

S32G3 Software Support Summary

by: NXP Semiconductors

Legal Disclaimers

Disclaimer related to a project description/roadmap

The information given hereunder is non-binding and preliminary and provided without legal commitment whatsoever. The information may be subject to changes and amendments. As with any project, inherent uncertainties can lead to the termination or delay of the project at any time. NXP does not accept any liability with regard to the project description given hereunder nor to any project realization. Any project commitment is subject to conclusion of a separate duly signed contract.

Disclaimer for timelines/schedules

The dates provided herein are non-binding and preliminary and provided without legal commitment whatsoever. The timeline, and the assumptions underlying that timeline, are subject to change at any time. NXP does not accept any liability with regard to the dates provided. Any dates or other information provided by NXP are binding only upon conclusion of a written contract signed by customer and NXP.



Contents

Contents 2

Chapter 1 Introducing the S32G3 Software 3

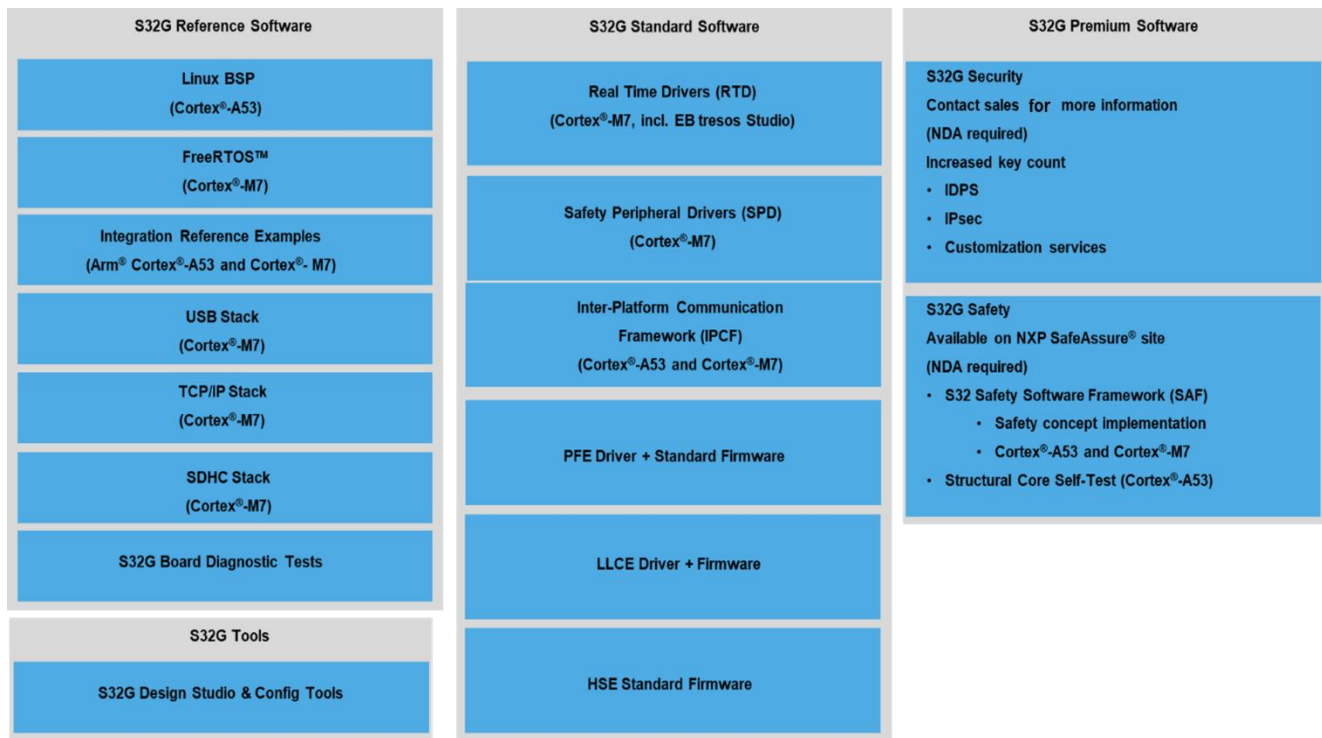
Chapter 2 S32G3 Reference Software 4

Chapter 3 S32G3 Standard Software 5

Chapter 1 Introducing the S32G3 Software

The S32G3 vehicle network processors are supported by a broad range of software enablement that is comprised of Reference Software, Standard Software and Premium Software, in addition to support from the S32 Design Studio IDE:

- Reference Software includes FreeRTOS™ support for the Arm® Cortex®-M7 cores and Linux® BSP support for the Cortex-A53 cores, as well as integration reference examples and board diagnostic tests.
- Standard Software includes Real Time Drivers for AUTOSAR® and non-AUTOSAR operating systems, Safety Peripheral Drivers, an Inter-Platform Communication Framework for communications between the Cortex-M7 and Cortex-A53 cores and hardware accelerator drivers and firmware.
- Premium Software includes Premium Security with expanded security capabilities and Premium Safety, which includes the S32 Safety Software Framework for functional safety implementations and Structural Core Self-Test (SCST) for the Cortex-A53 cores.



Chapter 2 S32G3 Reference Software

Table 1. S32G3 Reference Software Enablement Status

Additional Cortex-M7 Reference Software	Description	Status
FreeRTOS	FreeRTOS for integration with S32 Design Studio	Now
SDHC	SDHC stack non-AUTOSAR environment	Now
TCP/IP	TCP/IP stack for non-AUTOSAR environment	Now
USB	USB stack for non-AUTOSAR environment	Now

Table 2. S32G3 Integration Reference Examples Status

Integration Reference Software	Description	Status
GoldVIP	Vehicle Integration Platform reference software, includes CAN gateway, ETH gateway, IDPS, Xen-Hypervisor, OTA, Telemetry, etc...	Now
Other Integration reference examples	Lighting, Router	Now

Chapter 3 S32G3 Standard Software

Table 3. S32G3 RTD Software Enablement Status

Real Time Driver (RTD) Enablement	Description	AUTOSAR (M7) Status	Non-AUTOSAR (M7) Status
ADC	Driver, Analog-to-Digital Conversion	Now	Now
Base	Base Module, General AUTOSAR and Hardware Specific register files	Now	Now
CAN	Driver, Controller Area Network	Now	Now
CanIf	Support Stub, Controller Area Network Interface	Now	Now
CRC	Driver, Cyclic Redundancy Check	Now	Now
Crypto	Driver, Cryptographic Operations	Now	Now
CryIf	Support Stub, Crypto Interface	Now	Now
CSM	Support Stub, Crypto Service Manager	Now	Now
DEM	Support Stub, Diagnostic Event Manager	Now	Now
DET	Support Stub, Development Error Tracer	Now	Now
DIO	Driver, Digital Input Output	Now	Now
EcuC	Support Stub, ECU Configuration	Now	Now
EcuM	Support Stub, ECU State Manager	Now	Now
EEP	Driver, EEPROM	Now	Now
ETH	Driver, Ethernet	Now	Now
EthIf	Support Stub, Ethernet Interface	Now	Now
EthSwT	Driver, Ethernet Switch	Now	Now
EthTrcv	Driver, Ethernet Transceiver	Now	Now
FEE	Driver, Flash EEPROM Emulation	Now	Now
FLS	Driver, Flash	Now	Now
FR	Driver, FlexRay	Now	Now
FrIf	Support Stub, FlexRay Interface	Now	Now
GPT	Driver, General Purpose Timer	Now	Now
I2C	Driver, Inter-Integrated Circuit	Now	Now
ICU	Driver, Input Capture Unit	Now	Now
LIN	Driver, Local Interconnect Network	Now	Now
LinIf	Support Stub, Local Interconnect Network Interface	Now	Now
MCL	Driver, Microcontroller Library	Now	Now
MCU	Driver, Microcontroller Unit	Now	Now
MemIf	Support Stub, Memory Interface	Now	Now
OCOTP	Driver, On-Chip One Time Programmable Controller	Now	Now
OCU	Driver, Output Control Unit	Now	Now
OS	Support Stub, Operating System	Now	Now
PLATFORM	Driver, Platform	Now	Now
PMIC	Driver, Power Management Integrated Circuit	Now	Now
PORT	Driver, Port	Now	Now
PWM	Driver, Pulse Width Modulation	Now	Now
QDEC	Driver, Quadrature Decoder	Now	Now

Resource	Resource Module, Required by all other modules to select MCU derivative	Now	Now
RM	Driver, Resource Manager	Now	Now
RTE	Support Stub, only for Schedule Manager	Now	Now
SERDES	Driver, SerDes subsystem, SGMII and PCIe functionality	Now	Now
SPI	Driver, Serial Peripheral Interface	Now	Now
Thermal	Driver, Thermal Management	Now	Now
UART	Driver, UART Driver	Now	Now
WDG	Driver, Watchdog	Now	Now
WdgIf	Support Stub, Watchdog Interface	Now	Now
WDG_VR5510	Driver, Watchdog for VR5510	Now	Now

Table 4. S32G3 PFE Software Enablement Status

PFE SW Feature	Linux (A53) Status	AUTOSAR (M7) Status	Non-AUTOSAR (M7) Status
Datapath Endpoint -Traffic distribution from/to host system with HW pre-classification of RX packets	Now	Now	Q4 2023
MAC RGMII	Now	Now	Q4 2023
MAC SGMII¹	Now	Now	Q4 2023
Multi-instance Datapath Endpoint -Ability to run multiple driver instances within separate environments (CPUs/VMs) sharing the PFE-provided connectivity. Master-Slave concept	Now	Now	Q4 2023
FCI/libFCI	Now	Now	Q4 2023
IPv4/IPv6 Router -L3/L4 traffic router within Fast Path domain (TCP/UDP)	Now	Now	Q4 2023
IPv4/IPv6 Multicast Router -L3/L4 traffic router with multicast support (TCP/UDP)	Not Supported	Not Supported	Not Supported
L2 Switching - VLAN Aware Switch -Ethernet switch within Fast Path domain.	Now	Now	Q4 2023
Flexible Router -Fast-path traffic router allowing an arbitrary combination of packet properties including packet payload values to be used to make routing decisions.	Now	Now	Q4 2023
Ingress QoS Management API -Configuration of ingress traffic prioritization and congestion prevention. Access to statistics.	Now	Now	Q4 2023

Egress QoS Management API -Configuration of egress traffic aggregation and prioritization	Now	Now	Q4 2023
IPsec Offload -Transparent ESP Tunnel mode with HSE assistance	Demo Now	Not Supported	Not Supported
IDPS integration²	Now	Not Supported	Not Supported
Traffic/Runtime Statistics	Now	Now	Q4 2023
MDIO support	Now	Now	Q4 2023
IEEE 1588 Timestamping	Now	Now	Q4 2023
Runtime Errors Reporting -Firmware State Monitoring -HW Watchdogs Monitoring -Bus Parity Errors Monitoring -Error Interrupts Monitoring -Safety Events Reporting and Handling	Now	Now	Q4 2023
IGMP -EMAC Multicast group membership	Not Supported	Not Supported	Not Supported
HIF/AUX interface	Now	Now	Q4 2023
Multi-client HIF³	Now	Now	Q4 2023
HIF no copy support	Not Supported	Now	Q4 2023
MACsec integration	Not Supported	Not Supported	Not Supported
CMM – Contrack Monitor Module for dynamic connection tracking	Demo Now	NA	NA
Flexible Filter -Classify ingress traffic according to a set of custom classification rules	Now	Now	Q4 2023
Mirroring -Selective mirroring and RSPAN	Now	Now	Q4 2023
Suspend to RAM	Now (Master) Q2 2023 (Slave)	Not Supported	Not Supported
Jumbo Frames	Now	Not Supported	Not Supported

1. SGMII autoneg supported between 2.5G/1G/100M. For RGMII autoneg supported is 1G/100M/10M.
2. Available via Argus Cyber Security
3. MCAL - Multiple AUTOSAR Controllers through single HIF channel accessing multiple eMACs is supported

Table 5. S32G3 LLCE Software Enablement Status

LLCE Software Feature	Linux (A53) Status	AUTOSAR (M7) Status	Non-AUTOSAR (M7) Status
LLCE CAN	Now	Now	Now
LLCE LIN	Not Supported	Now	Now
LLCE FlexRay	Not Supported	Now	Now
LLCE LPSPi	Not Supported	Now	Now
LLCE Logging	Now	Now	Now
LLCE Advanced Features*	Q4 2023	Now	Now
LLCE headless mode	Not Supported	Now	Now
Advanced Features*			
CAN2CAN	Q4 2023	Now	Now
Multi-host	Q4 2023	Now	Now

CAN2ETH	Not Supported	Now	Now
ETH2CAN	Not Supported	Now	Now

Table 6. S32G3 HSE (Hardware Security Engine) Software Enablement Status

HSE Enablement	Status	Comment
Linux (A53)	Now	Crypto driver available
AUTOSAR (M7)	Now	Crypto driver available
Non-AUTOSAR (M7)	Now	Demo application provided as a baseline to enable customer development
Suspend To RAM (Linux)	Now	Starting with BSP33 without Secure-boot
OTFAD	Yes	App Note being developed
Secure Boot - Basic	Now	Not Supported in Linux
Secure Boot - Advanced	Now	Supported in Linux as well
Installing HSE firmware and SYS_IMG	Now	Supported in Linux as well
HSE programming during ECU production	Now	Recommended to convert HSE firmware from Pink to Blue in factory
Premium HSE software support	Not Supported	
Anti-rollback counter protection	Now	Requires VDD_EFUSE present at boot time
Message Unit (MU) support on A53 (Linux/QNX)	Now	Two independent drivers, kernel crypto and HSE UIO, available in Linux BSP, each using a different MU instance
PKCS #11 support (Linux)	Now	Enhanced support in progress
VKMS Vehicle Key Management System (AUTOSAR / Non-AUTOSAR / QNX)	Now	Contact NXP representative for further information

Table 7. S32G3 DRAM Software Enablement Status

DRAM Enablement	Status	Comment
Linux (A53)	Now	
AUTOSAR (M7)	Not Supported	
Non-AUTOSAR (M7)1	Now	Code generated by DDR tool can be used for customer development
Suspend To RAM (Linux)	Now	
LPDDR42	Now	
DDR3L2	Now	
Dual Channel	Now	
ECC	Now	
IO retention routine for customer application (DDR Tool)	Now	Code generated by DDR tool can be used for customer development

1. M7 code intended for DRAM initialization only, depending on preferred boot approach, M7 only parts (S32G234M) do not support DRAM. M7 code execution out of DRAM is not recommended.
2. Micron parts used on NXP hardware platforms

Table 8. S32G3 PCI Express (PCIe) Software Enablement Status

PCIe Enablement	Status	Comment
Linux (A53) only – Root Complex (RC)	Now	
Linux (A53) only – Endpoint (EP)	Now	
AUTOSAR (M7)	Now	
Non-AUTOSAR (M7)	Now	
GEN 1,2 & 3	Now	
x1, x2 lane	Now	
External / Internal SerDes clock	Now	See Hardware Developer’s Guide for recommended operating conditions
MSI	Now	Supports EP to RC, according to PCIe specification
Endpoint function (EPF) and controller (EPC) library	Now	Available as demo (pcitest)
Device resource access through sysfs	Not Supported	
Advanced Error Reporting (AER)	Now	Available as demo (pcitest)
Hot Plug	Now	Partial support, full support with BSP33

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, Freescale, the Freescale logo are the trademarks of NXP B.V. All other product or service names are the property of their respective owners. Arm, the Arm logo, and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved.

© 2023 NXP B.V

Document Number: S32GSWSS

Rev. 1

03/2023

