SOT1288

Plastic single-ended multi-chip package; 6 interconnections; 3 in-line leads

2 August 2016   Package information
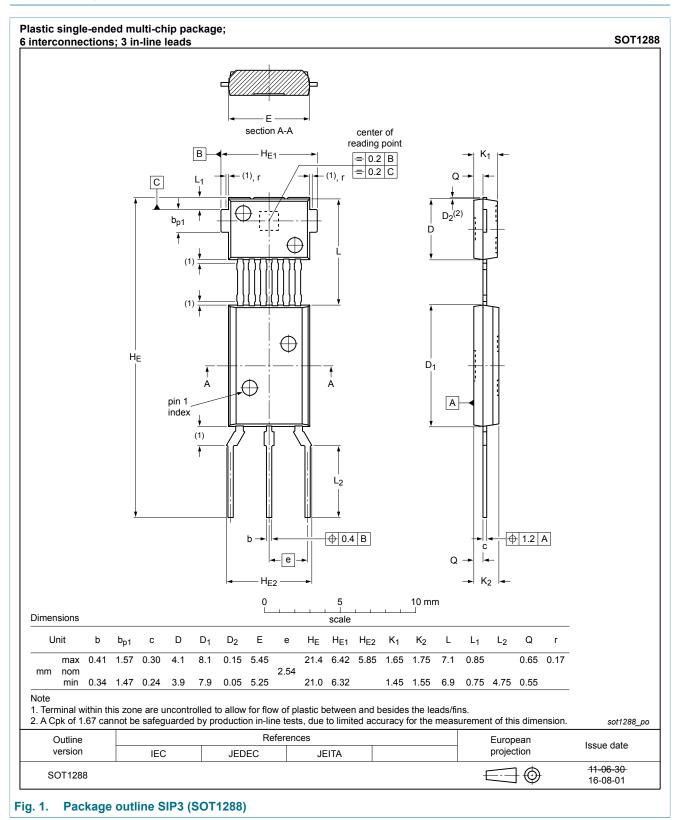
1. Package summary

Dimensions (mm)	21.4 x 6.42 x 1.75
Terminal position code	S (single)
Package type descriptive code	SIP3
Package outline version code	SOT1288
Manufacturer package code	SOT1288
Package type industry code	SIP3
Package outline version description	Plastic single-ended multi-chip package; 6 interconnections; 3 in-line leads
Package style descriptive code	SIP (single in-line package)
Package body material type	P
Handling precautions	IC26_CHAPTER_3_2000
Thermal design considerations	SC18_1999_CHAPTER_5_2
Mounting method type	T (through-hole mount)
Major version date	16-4-2012
Minor version date	11-5-2012
Security status	COMPANY PUBLIC
Modified date	11-5-2012
Issue date	2-8-2016
Web publication date	28-11-2012
Initial web publication date	17-4-2012
Customer specific indicator	N
Maturity	Product

Table 1. Package summary

Symbol	Parameter		Min	Typ	Nom	Max	Unit
D	package length		3.9	-	4	4.1	mm
E	package width		5.25	-	5.35	5.45	mm
e	nominal pitch		-	-	2.54	-	mm
n_2	actual quantity of termination		-	-	3	-	

2. Package outline

Plastic single-ended multi-chip package;
6 interconnections; 3 in-line leads **SOT1288**

		b	b_{p1}	c	D	D_1	D_2	E	e	H_E	H_{E1}	H_{E2}	K_1	K_2	L	L_1	L_2	Q	r
	Unit																		
mm	max	0.41	1.57	0.30	4.1	8.1	0.15	5.45		21.4	6.42	5.85	1.65	1.75	7.1	0.85		0.65	0.17
	nom								2.54										
	min	0.34	1.47	0.24	3.9	7.9	0.05	5.25		21.0	6.32		1.45	1.55	6.9	0.75	4.75	0.55	

Note

1. Terminal within this zone are uncontrolled to allow for flow of plastic between and besides the leads/fins.
2. A Cpk of 1.67 cannot be safeguarded by production in-line tests, due to limited accuracy for the measurement of this dimension.

sot1288_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1288						~~11-06-30~~ 16-08-01

Fig. 1. Package outline SIP3 (SOT1288)

3. Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

4. Contents