AN5415

Estimation of PWM duty cycle range for MC33HB200x at different slew rates

Rev. 2.0 — 2 October 2018 Application note

Document information

Information	Content
Keywords	pulse width modulation (PWM), field-effect transistor (FET), serial peripheral interface (SPI)
Abstract	This application note gives an estimation of PWM duty cycle accuracy that can be achieved using MC33HB2000, MC33HB2001 and MC33HB2002 at varying slew rate settings and voltage levels.

Revision history

Rev	Date	Description
1.0	20170419	• Initial version
2.0	20181002	• Updated document title, document abstract, Section 1, Section 3, Section 5, Section 7 to accommodate MC33HB2002

1 Introduction

In all motor control applications, there are several trade-offs a system engineer performs to get the optimum performance of overall system. One of the important trade-offs is switching accuracy and efficiency versus noise. In some applications noise is more important and in others the switching efficiency takes priority over noise especially when the operating temperature is high. NXP's MC33HB200x family of H-bridge motor drivers provides eight selectable slew rates which can be changed while operating via SPI. The eight selectable slew rate settings via SPI give the system engineer flexibility and configurability in optimizing the system performance.

However, to utilize such flexibility best, one should know the limitations associated with a particular setting in terms of accuracy and operating duty cycle. This application note gives a good estimation of the upper and the lower limits of PWM duty cycle at which MC33HB2000, MC33HB2001 and MC33HB2002 can be operated. It helps system engineers to know the boundaries and select appropriate slew rate for an application.

2 Factors effecting PWM duty cycle accuracy

PWM duty cycle accuracy can be critical for applications requiring precise control to maintain the overall stability of a system. There are several factors which impact the overall PWM accuracy in H#bridge motor drivers. In MC33HB2000 and MC33HB2001, the factors effecting the PWM duty cycle accuracy are as follows.

1. Slew rate (SR) - major impact
2. Dead time between switching high-side and low-side FETs to prevent shoot-through - major impact: depends on slew setting
3. OUTx turn-on and turn-off delay time (t_{DON}, t_{DOFF}) - medium impact and if turn-on and turn-off delays are not equal can become major impact
4. Junction temperature (T_J) - medium impact
5. Battery voltage (V_{PWR}) - medium to minor as it may impact the slew rate and thus the switching time to affect the accuracy

In most cases, selecting the highest slew rate provides the best PWM duty cycle accuracy. Moreover, using the highest slew rate also makes the switching more efficient by reducing switching losses. However, highest slew rate may generate more noise. Depending on the type of system, one may need to perform a trade-off between noise, PWM duty cycle accuracy and switching efficiency. In such cases, the system engineer has to select an intermediate slew setting which is optimum for switching accuracy, efficiency and noise. Nonetheless, to enable such decisions one must know the boundaries and limitations for each setting and how they drift with voltage and temperature. A typical timing diagram showing the input and output timing parameters while switching is shown in Figure 1.

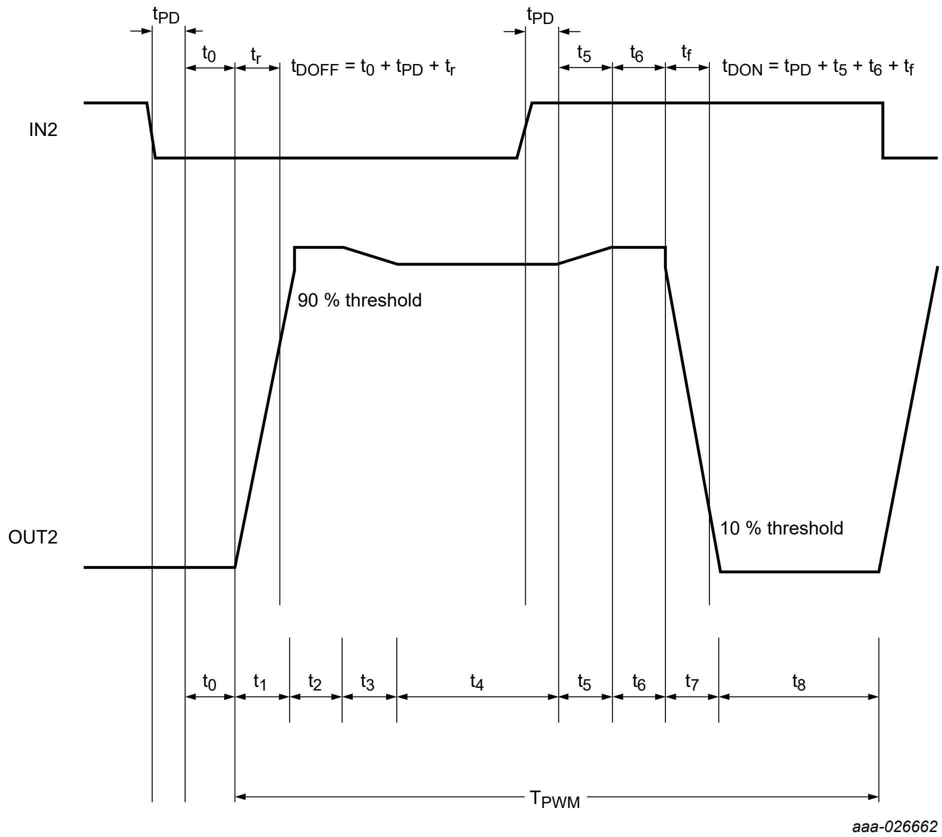


Figure 1. Timing parameters associated with input and output while switching

The description of each timing parameter is as follows.

Table 1. Description of timing parameters

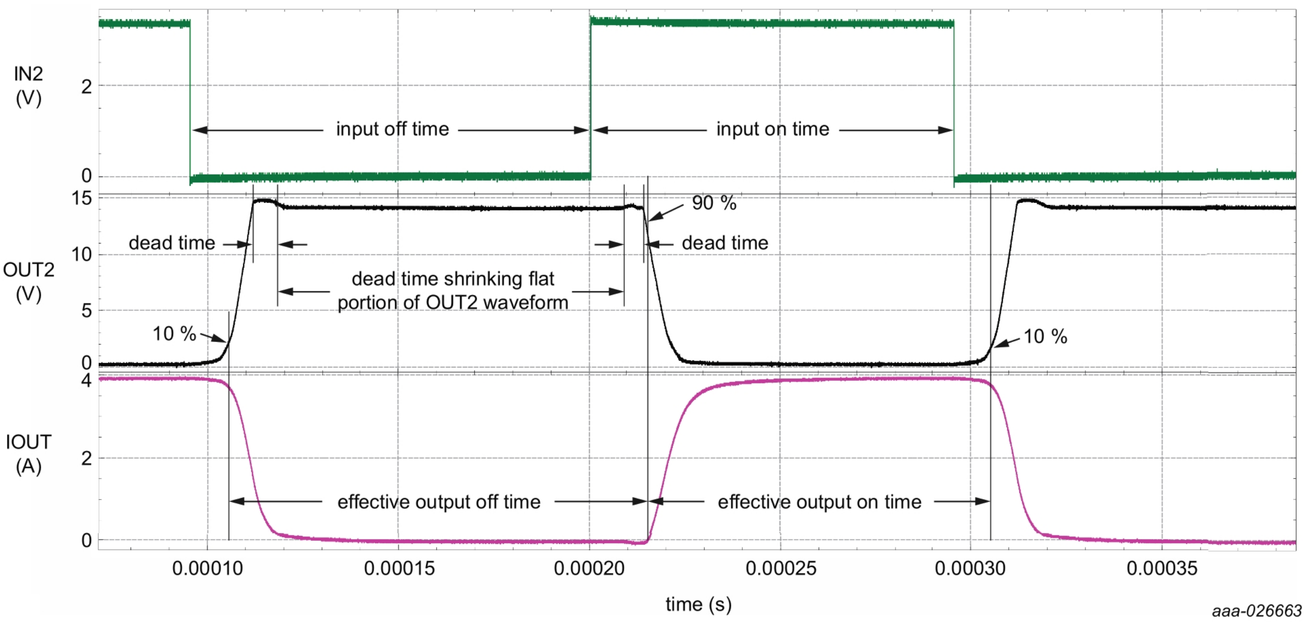
Timing parameter	Description	Impact on PWM duty cycle accuracy/ comments
t_{PD}	propagation delay between input switching and out initiating switching (logic delay)	no impact
t_0	time during which low-side FET prepares to switch	slew dependent; medium to major impact; can have major impact for very low or high duty cycle
t_r	0 % to 90 % of the total voltage swing on the rising edge of OUTx voltage	slew dependent; major impact
t_1	0 % to 100 % of the total voltage swing on the rising edge of OUTx voltage	slew dependent; major impact
t_2, t_6	dead time between switching high-side and low-side FETs	slew dependent; major impact
t_3	time to complete the switching from low-side to high-side after dead time	slew dependent; medium to major impact; can have major impact for very low or high duty cycle

Timing parameter	Description	Impact on PWM duty cycle accuracy/ comments
t_4	time during which high-side FET remains on	slew dependent; it represents the major part of duty cycle; higher the percentage of this parameter when compared to timing parameters associated with switching, more the accuracy
t_5	time during which high-side FET prepares to switch	slew dependent; medium to major impact; can have major impact for very low or high duty cycle
t_7	100 % to 0 % of the total voltage swing on the falling edge of OUTx voltage	slew dependent; major impact
t_f	100 % to 10 % of the total voltage swing on the falling edge of OUTx voltage	slew dependent; major impact
t_8	time during which low-side FET remains on	slew dependent; it represents the major part of duty cycle; higher the percentage of this parameter when compared to timing parameters associated with switching, more the accuracy

All of the above timing parameters influence the PWM duty cycle accuracy.
A combination of these parameters becomes the specifications defined in the data sheet. For example, OUTx turn-off delay time is $t_{DOFF} = t_0 + t_{PD} + t_r$. Similarly, OUTx turn#off delay time is $t_{DON} = t_{PD} + t_5 + t_6 + t_f$. Asymmetry in t_{DON} and t_{DOFF} contributes toward inaccuracy in PWM duty cycle and the inaccuracy may drift a bit based on PWM frequency, voltage and temperature. In this application note, we are going to look at the estimated boundaries of PWM duty cycle for each slew setting at different voltage levels and PWM frequencies.

3 Dead-time impact

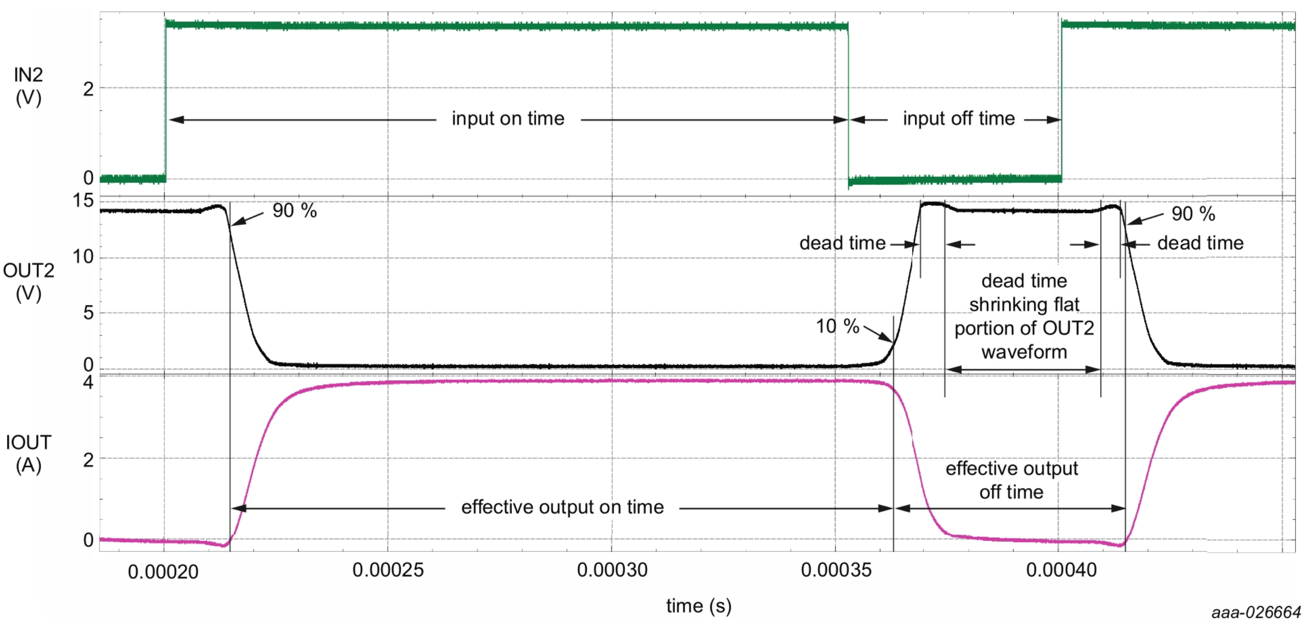
The MC33HB200x product family does not have fixed, pre-programmed dead time. The dead time between high-side and low-side FETs on the same half-bridge while switching is based on gate voltage detection of the FET. Due to the dependency of gate voltage on the slew rate, the dead time automatically adjusts itself for each slew setting to give the optimum cross-conduction protection. Dead time has major dependency on the slew rate as it scales up and down along with the slew rate. The dead time has a major impact on PWM duty cycle accuracy (especially at extreme duty cycle values). During the dead time the device is not delivering any power to the load. It is just an intermediate state between a switching event. As a result, the smaller the duty cycle requirement (on or off) the more error introduced by the dead time; as the dead time becomes a larger part of duty cycle. Figure 2 to Figure 4 demonstrate this phenomenon.



the signal is ON 50 % of the time and OFF 50 % of the time

5000 Hz at 2 V/µs

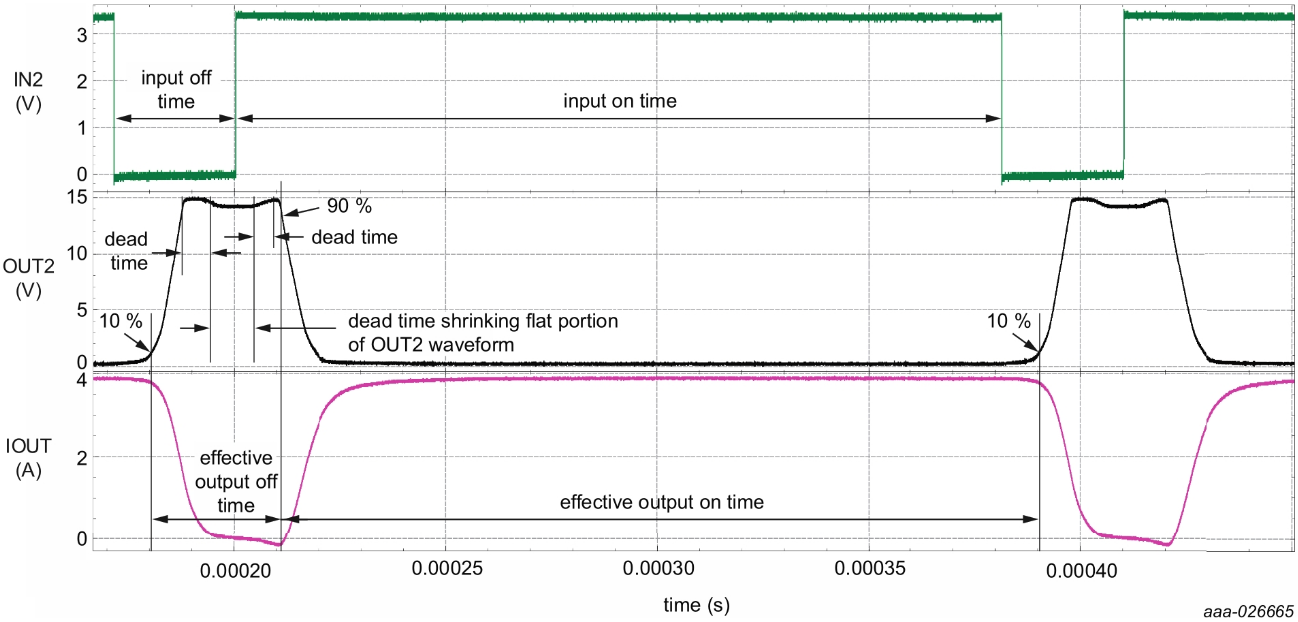
Figure 2. OUT2 duty cycle closely matching the commanded duty cycle by IN2



the signal is ON 70 % of the time and OFF 30 % of the time

5000 Hz at 2 V/µs

Figure 3. Introduction of error in OUT2 duty cycle when compared to IN2



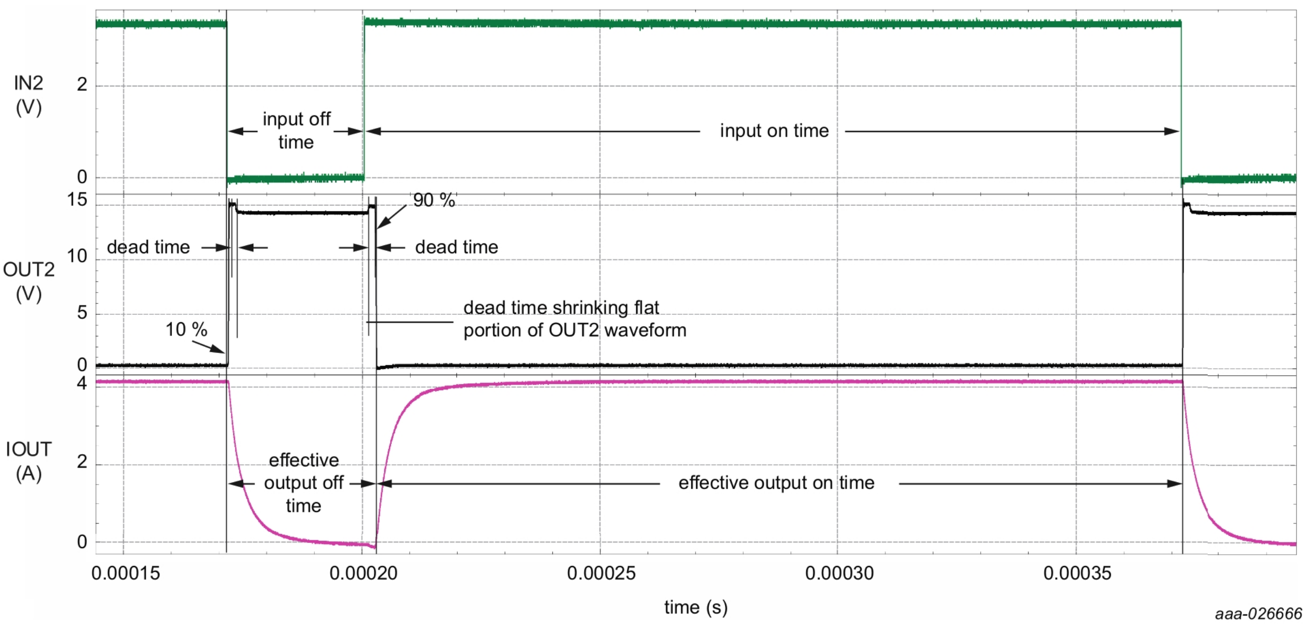
the signal is ON 90 % of the time and OFF 10 % of the time

5000 Hz at 2 V/μs

Figure 4. Increasing error in OUT2 duty cycle when compared to IN2

Duty cycle definition for motor control: Selecting an effective duty cycle can be subjective and may change from one application to another. For brushed DC motor control, one may consider an effective duty cycle based on the current flowing through the load. Based on the start of current flowing through the load to the point when current starts dropping can be considered as an effective on-duty cycle and the remaining time in that period of the PWM cycle is the off-duty cycle.

Based on this assumption, the effective off-duty cycle has been shown in Figure 2 to Figure 4, which in terms of output voltage, corresponds to about 10 % threshold on the rising edge to 90 % threshold on the falling edge. The above readings were taken with 2 V/μs slew setting with PWM signal at 5000 Hz. It is clear from the above figures that as the duty cycle approaches toward extreme values, the error in duty cycle on OUTx with respect to input keeps increasing. However, this error can be reduced if a higher slew setting than 2 V/μs was selected. The duty cycle error happens due to timing parameters described in Table 1. Figure 5 shows the reduced error in duty cycle at the highest slew setting with the same input duty cycle (90 %) as shown in Figure 4.



the signal is ON 90 % of the time and OFF 10 % of the time

5000 Hz at highest slew setting

Figure 5. Reduced error in OUT2 duty cycle when compared to IN2

4 Slew rate impact

Slew rate has direct or indirect impact on all the parameters defined in Table 1 except for propagation delay (t_{PD}). However, slew rate changes with temperature as well as the battery voltage. The temperature variation can be compensated for by taking the minimum value into consideration at 14 V which is specified in the data sheet. Although, the data sheet specifies the slew rate at 14 V, for other battery voltage levels, there may be slight shift in the slew rate which can be modeled empirically as follows.

Table 2. Experimentally determined slew rates at different battery voltages

Battery voltage [V]	Rise/fall time [µs]	Slew [V/µs]
6	4.74	1.27
7	5.04	1.39
8	5.44	1.47
10	6.14	1.63
12	6.94	1.73
14	7.44	1.88
18	8.54	2.11
24	9.44	2.54

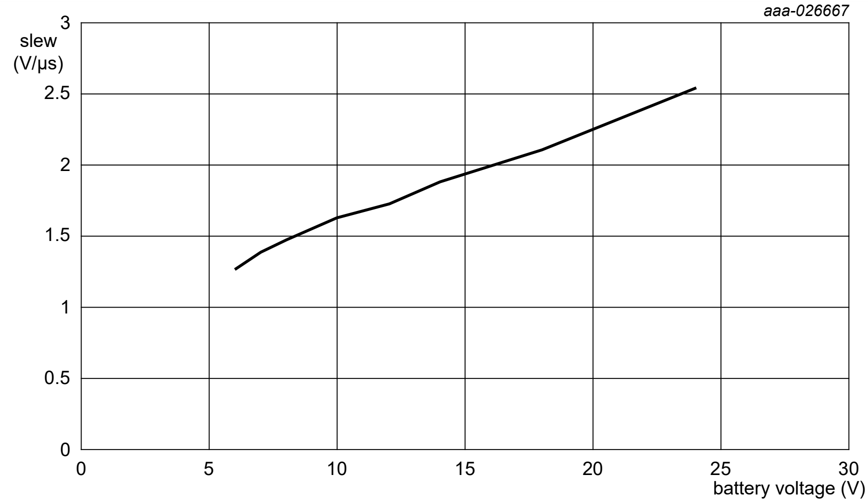


Figure 6. Experimental slew rate versus battery voltage

If the slew rate value for one voltage (in this case 14 V) is known, one may determine the slew rate for any battery voltage.

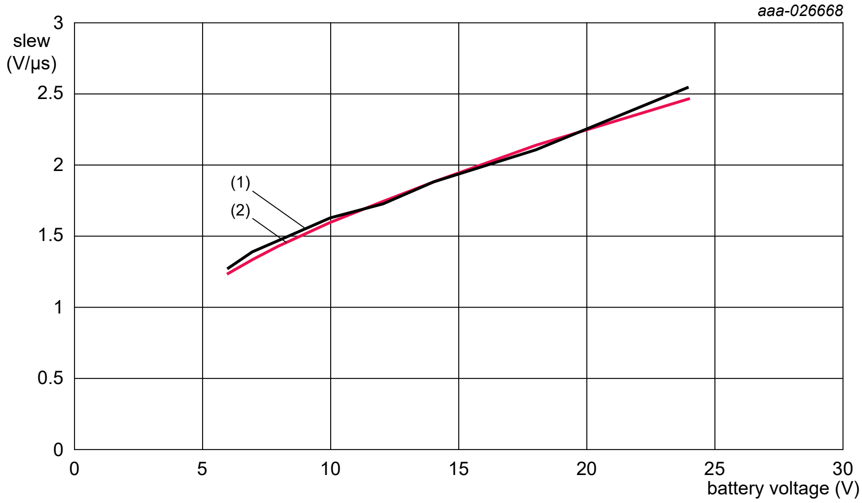
Table 3. Theoretically determined slew rates at different battery voltages

Battery voltage [V]	Rise/fall time [µs]	Slew [V/µs]
6	4.87	1.23
7	5.26	1.33
8	5.62	1.42
10	6.29	1.59
12	6.89	1.74
14	7.44	1.88
18	8.44	2.13
24	9.74	2.46

Based on the data gathered from limited devices, theoretically, the slew rate with battery voltage at x can be modeled as follows when slew rate at 14 V is known.

$$\text{slew rate at x Volt} = \frac{\sqrt{x}}{\sqrt{14}} \times \text{slew rate at 14 Volt} \tag{1}$$

Figure 7 shows the comparison of experimentally determined slew rate and theoretically estimated slew rate using Equation 1. It is clear from Figure 7 that the estimation is close. Moreover, the theoretically estimated slew rate value is slightly lower than the experimentally determined one. Hence, using theoretical value would give the worst case for slew time and result in the worst case error in the duty cycle.



1. Experimental slew rate
2. Calculated slew rate

Figure 7. Theoretical slew rate versus experimental slew rate at different battery voltages

5 Duty cycle range for various PWM frequencies at all the slew settings

The model in Equation 1 verifies that we can actually use the mathematical model for estimation for operation at different voltage levels. In order to get the worst case, one should consider the worst case slew rate defined in the specification, which in this case is the minimum value. Based on Equation 1, considering the worst case slew rate and the timing parameters explained in Table 1, Table 4 to Table 8 give an estimation of duty cycle range at different PWM frequencies for all the slew rate settings.

Table 4. Theoretically determined duty cycle range at 1 kHz PWM frequency

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 1 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
6 V	bypass	1.713	2.963	bypass	0.363	1.613	bypass	0.2	99.8
	16	2.905	5.530	16	1.555	4.180	16	0.6	99.4
	8	4.460	8.210	8	3.110	6.860	8	1.1	98.9
	4	7.569	12.194	4	6.219	10.844	4	1.9	98.1
	2	13.788	22.663	2	12.438	21.313	2	3.7	96.3
	1	26.227	43.727	1	24.877	42.377	1	7.4	92.6
	0.5	51.104	86.229	0.5	49.754	84.879	0.5	14.8	85.2
	0.25	117.442	186.567	0.25	116.092	185.217	0.25	33.1	66.9
14 V	bypass	1.904	3.154	bypass	0.554	1.804	bypass	0.3	99.7
	16	3.725	6.350	16	2.375	5.000	16	0.8	99.2
	8	6.100	9.850	8	4.750	8.500	8	1.5	98.5
	4	10.850	15.475	4	9.500	14.125	4	2.6	97.4
	2	20.350	29.225	2	19.000	27.875	2	5.2	94.8
	1	39.350	56.850	1	38.000	55.500	1	10.3	89.7
	0.5	77.350	112.475	0.5	76.000	111.125	0.5	20.6	79.4
	0.25	178.683	247.808	0.25	177.333	246.458	0.25	46.6	53.4
18 V	bypass	1.978	3.228	bypass	0.628	1.878	bypass	0.3	99.7
	16	4.043	6.668	16	2.693	5.318	16	0.9	99.1
	8	6.736	10.486	8	5.386	9.136	8	1.6	98.4
	4	12.122	16.747	4	10.772	15.397	4	2.9	97.1
	2	22.894	31.769	2	21.544	30.419	2	5.7	94.3
	1	44.438	61.938	1	43.088	60.588	1	11.4	88.6
	0.5	87.526	122.651	0.5	86.176	121.301	0.5	22.8	77.2
	0.25	202.427	271.552	0.25	201.077	270.202	0.25	100.0	100.0

[1] t_{PD} can be eliminated as it does not have dependency on slew setting.

Table 5. Theoretically determined duty cycle range at 5 kHz PWM frequency

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 5 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
6 V	bypass	1.713	2.963	bypass	0.363	1.613	bypass	1.1	98.9
	16	2.905	5.530	16	1.555	4.180	16	3.2	96.8
	8	4.460	8.210	8	3.110	6.860	8	5.5	94.5
	4	7.569	12.194	4	6.219	10.844	4	9.4	90.6
	2	13.788	22.663	2	12.438	21.313	2	18.6	81.4
	1	26.227	43.727	1	24.877	42.377	1	37.0	63.0
	0.5	51.104	86.229	0.5	49.754	84.879	0.5	100.0	100.0
	0.25	117.442	186.567	0.25	116.092	185.217	0.25	100.0	100.0
14 V	bypass	1.904	3.154	bypass	0.554	1.804	bypass	1.3	98.7
	16	3.725	6.350	16	2.375	5.000	16	4.1	95.9
	8	6.100	9.850	8	4.750	8.500	8	7.3	92.7
	4	10.850	15.475	4	9.500	14.125	4	13.0	87.0
	2	20.350	29.225	2	19.000	27.875	2	25.8	74.2
	1	39.350	56.850	1	38.000	55.500	1	100.0	100.0
	0.5	77.350	112.475	0.5	76.000	111.125	0.5	100.0	100.0
	0.25	178.683	247.808	0.25	177.333	246.458	0.25	100.0	100.0
18 V	bypass	1.978	3.228	bypass	0.628	1.878	bypass	1.4	98.6
	16	4.043	6.668	16	2.693	5.318	16	4.4	95.6
	8	6.736	10.486	8	5.386	9.136	8	8.0	92.0
	4	12.122	16.747	4	10.772	15.397	4	14.4	85.6
	2	22.894	31.769	2	21.544	30.419	2	28.6	71.4
	1	44.438	61.938	1	43.088	60.588	1	100.0	100.0
	0.5	87.526	122.651	0.5	86.176	121.301	0.5	100.0	100.0
	0.25	202.427	271.552	0.25	201.077	270.202	0.25	100.0	100.0

[1] t_{PD} can be eliminated as it does not have dependency on slew setting.

Table 6. Theoretically determined duty cycle range at 10 kHz PWM frequency

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 10 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
6 V	bypass	1.713	2.963	bypass	0.363	1.613	bypass	2.2	97.8

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 10 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
	16	2.905	5.530	16	1.555	4.180	16	6.3	93.7
	8	4.460	8.210	8	3.110	6.860	8	11.0	89.0
	4	7.569	12.194	4	6.219	10.844	4	18.8	81.2
	2	13.788	22.663	2	12.438	21.313	2	37.1	62.9
	1	26.227	43.727	1	24.877	42.377	1	100.0	100.0
	0.5	51.104	86.229	0.5	49.754	84.879	0.5	100.0	100.0
	0.25	117.442	186.567	0.25	116.092	185.217	0.25	100.0	100.0
14 V	bypass	1.904	3.154	bypass	0.554	1.804	bypass	2.6	97.4
	16	3.725	6.350	16	2.375	5.000	16	8.1	91.9
	8	6.100	9.850	8	4.750	8.500	8	14.6	85.4
	4	10.850	15.475	4	9.500	14.125	4	26.0	74.0
	2	20.350	29.225	2	19.000	27.875	2	100.0	100.0
	1	39.350	56.850	1	38.000	55.500	1	100.0	100.0
	0.5	77.350	112.475	0.5	76.000	111.125	0.5	100.0	100.0
	0.25	178.683	247.808	0.25	177.333	246.458	0.25	100.0	100.0
18 V	bypass	1.978	3.228	bypass	0.628	1.878	bypass	2.8	97.2
	16	4.043	6.668	16	2.693	5.318	16	8.8	91.2
	8	6.736	10.486	8	5.386	9.136	8	16.0	84.0
	4	12.122	16.747	4	10.772	15.397	4	28.8	71.2
	2	22.894	31.769	2	21.544	30.419	2	100.0	100.0
	1	44.438	61.938	1	43.088	60.588	1	100.0	100.0
	0.5	87.526	122.651	0.5	86.176	121.301	0.5	100.0	100.0
	0.25	202.427	271.552	0.25	201.077	270.202	0.25	100.0	100.0

[1] t_{PD} can be eliminated as it does not have dependency on slew setting.

Table 7. Theoretically determined duty cycle range at 15 kHz PWM frequency

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 15 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
6 V	bypass	1.713	2.963	bypass	0.363	1.613	bypass	3.3	96.7
	16	2.905	5.530	16	1.555	4.180	16	9.5	90.5
	8	4.460	8.210	8	3.110	6.860	8	16.4	83.6

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 15 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
	4	7.569	12.194	4	6.219	10.844	4	28.2	71.8
	2	13.788	22.663	2	12.438	21.313	2	100.0	100.0
	1	26.227	43.727	1	24.877	42.377	1	100.0	100.0
	0.5	51.104	86.229	0.5	49.754	84.879	0.5	100.0	100.0
	0.25	117.442	186.567	0.25	116.092	185.217	0.25	100.0	100.0
14 V	bypass	1.904	3.154	bypass	0.554	1.804	bypass	3.9	96.1
	16	3.725	6.350	16	2.375	5.000	16	12.2	87.8
	8	6.100	9.850	8	4.750	8.500	8	21.9	78.1
	4	10.850	15.475	4	9.500	14.125	4	39.0	61.0
	2	20.350	29.225	2	19.000	27.875	2	100.0	100.0
	1	39.350	56.850	1	38.000	55.500	1	100.0	100.0
	0.5	77.350	112.475	0.5	76.000	111.125	0.5	100.0	100.0
	0.25	178.683	247.808	0.25	177.333	246.458	0.25	100.0	100.0
18 V	bypass	1.978	3.228	bypass	0.628	1.878	bypass	4.1	95.9
	16	4.043	6.668	16	2.693	5.318	16	13.2	86.8
	8	6.736	10.486	8	5.386	9.136	8	24.0	76.0
	4	12.122	16.747	4	10.772	15.397	4	43.2	56.8
	2	22.894	31.769	2	21.544	30.419	2	100.0	100.0
	1	44.438	61.938	1	43.088	60.588	1	100.0	100.0
	0.5	87.526	122.651	0.5	86.176	121.301	0.5	100.0	100.0
	0.25	202.427	271.552	0.25	201.077	270.202	0.25	100.0	100.0

[1] t_{PD} can be eliminated as it does not have dependency on slew setting.

Table 8. Theoretically determined duty cycle range at 20 kHz PWM frequency

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 20 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
6 V	bypass	1.713	2.963	bypass	0.363	1.613	bypass	4.3	95.7
	16	2.905	5.530	16	1.555	4.180	16	12.6	87.4
	8	4.460	8.210	8	3.110	6.860	8	21.9	78.1
	4	7.569	12.194	4	6.219	10.844	4	37.5	62.5
	2	13.788	22.663	2	12.438	21.313	2	100.0	100.0

V_{PWR}	Calculated t_{DOFF} and t_{DON} with propagation delay included			Calculated $t_{DOFF} - t_{PD}$ and $t_{DON} - t_{PD}$[1]			Calculated the duty cycle range PWM frequency		
	Calculated value			Calculated value			DC range at 20 kHz		
	SR (V/µs)	t_{DOFF} (µs)	t_{DON} (µs)	SR (V/µs)	$t_{DOFF} - t_{PD}$ (µs)	$t_{DON} - t_{PD}$ (µs)	SR (V/µs)	DC min (%)	DC max (%)
	1	26.227	43.727	1	24.877	42.377	1	100.0	100.0
	0.5	51.104	86.229	0.5	49.754	84.879	0.5	100.0	100.0
	0.25	117.442	186.567	0.25	116.092	185.217	0.25	100.0	100.0
14 V	bypass	1.904	3.154	bypass	0.554	1.804	bypass	5.2	94.8
	16	3.725	6.350	16	2.375	5.000	16	16.2	83.8
	8	6.100	9.850	8	4.750	8.500	8	29.2	70.9
	4	10.850	15.475	4	9.500	14.125	4	100.0	100.0
	2	20.350	29.225	2	19.000	27.875	2	100.0	100.0
	1	39.350	56.850	1	38.000	55.500	1	100.0	100.0
	0.5	77.350	112.475	0.5	76.000	111.125	0.5	100.0	100.0
	0.25	178.683	247.808	0.25	177.333	246.458	0.25	100.0	100.0
18 V	bypass	1.978	3.228	bypass	0.628	1.878	bypass	5.5	94.5
	16	4.043	6.668	16	2.693	5.318	16	17.6	82.4
	8	6.736	10.486	8	5.386	9.136	8	31.9	68.1
	4	12.122	16.747	4	10.772	15.397	4	100.0	100.0
	2	22.894	31.769	2	21.544	30.419	2	100.0	100.0
	1	44.438	61.938	1	43.088	60.588	1	100.0	100.0
	0.5	87.526	122.651	0.5	86.176	121.301	0.5	100.0	100.0
	0.25	202.427	271.552	0.25	201.077	270.202	0.25	100.0	100.0

[1] t_{PD} can be eliminated as it does not have dependency on slew setting.

The above modeled data gives a guideline to system engineers to make their decision solely based on duty cycle accuracy and range of operating duty cycle for any application. However, this information should only be used as a guideline as this model has been created using extensive empirical data taken on limited units. Nonetheless, this should give a fair approximation of how a typical device of the MC33HB200x family performs for PWM duty cycle accuracy. Moreover, this application note does not take the noise and switching efficiency into consideration. The slew rate selection guideline presented is solely based on duty cycle accuracy. In some applications, noise and switching efficiency could have more priority over duty cycle accuracy which may require a different analysis.

6 Conclusion

From the above data and information, it is clear that the duty cycle accuracy is greater at fast slew rate settings when compared to slow slew settings. This fact is because all the parameters which have an impact on duty cycle accuracy except t_{PD} (shown in Table 1) are directly or indirectly slew dependent. Moreover, fast slew rate selection also result in better switching efficiency than slow slew rate configuration. However, inductive loads may result in higher noise at fast slew rate settings when compared to slower slew rate settings. Both thermal efficiency and noise are beyond the scope of this document. Hence, while selecting a slew setting for an application, numerous factors should be considered. A diligent choice should be made based on system requirements and design priorities.

7 References

Support page	Description	URL
MC33HB2000	product summary page	http://www.nxp.com/HB2000
MC33HB2001	product summary page	http://www.nxp.com/HB2001
MC33HB2002	product summary page	http://www.nxp.com/HB2002

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Date of release: 2 October 2018
Document identifier: AN5415