NXP Semiconductors
Application Notes

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S32G3 Power Estimations

by: NXP Semiconductors

1. Introduction

This application note supports the Power Estimation on S32G3. It describes the basic components and lists the steps to configure and estimate the power consumption on different voltage rails of S32G3.

This document helps enable embedded system designers to gain insights and design energy-efficient automotive gateway applications. It helps the system developer to estimate and design an optimal power supply scheme for their application use case.

The document leverages power consumption data from the device datasheet and additional real measurements or design estimates depending on availability. These estimates are provided “as is” and are not guaranteed within a specified precision. Power consumption depends on electrical parameters, silicon process variations, environmental conditions, and use cases running on the processor during operation. Actual power consumption should be verified in the real and complete system. You must always cross-verify the latest numbers from the device datasheet.

Contents

2. Common terms used

Static consumption – This is the minimum consumption when the device is powered. It is always present irrespective of any activity.

Dynamic consumption – This depends on the activity of the module and must be added to the static consumption to derive total consumption

S32G3HDG – Refers to the S32G3 Hardware design guideline document

IO – Input-output pads of the S32G3 silicon, refer to the IOMUX sheet in S32G3 Reference Manual

3. Attachments with the document

S32G3_PowerEstimator – This sheet provides an estimation of load on various power rails of the PMIC. The details on its usage are covered in section S32G3-PMIC power budgeting.

S32G3_IOpower_estimator – This sheets helps in configuring the IO activity and in estimating the dynamic current for the different IO supply rails. The details on its usage are covered in section S32G3 IO power estimation.

4. S32G3 power tree

The S32G3 device has multiple supply pins for the core, I/O, fuses, and, analog supplies. All such pins must be connected to the proper supply voltage for proper operation. NXP recommends using VR5510 and PPF53BDAMMA1ES PMIC in companion mode for S32G3 power requirements. The S32G3HDG provides further details on power connection recommendations.

The recommended power tree using S32G3, VR5510, and, PPF53BDAMMA1ES is shown below.

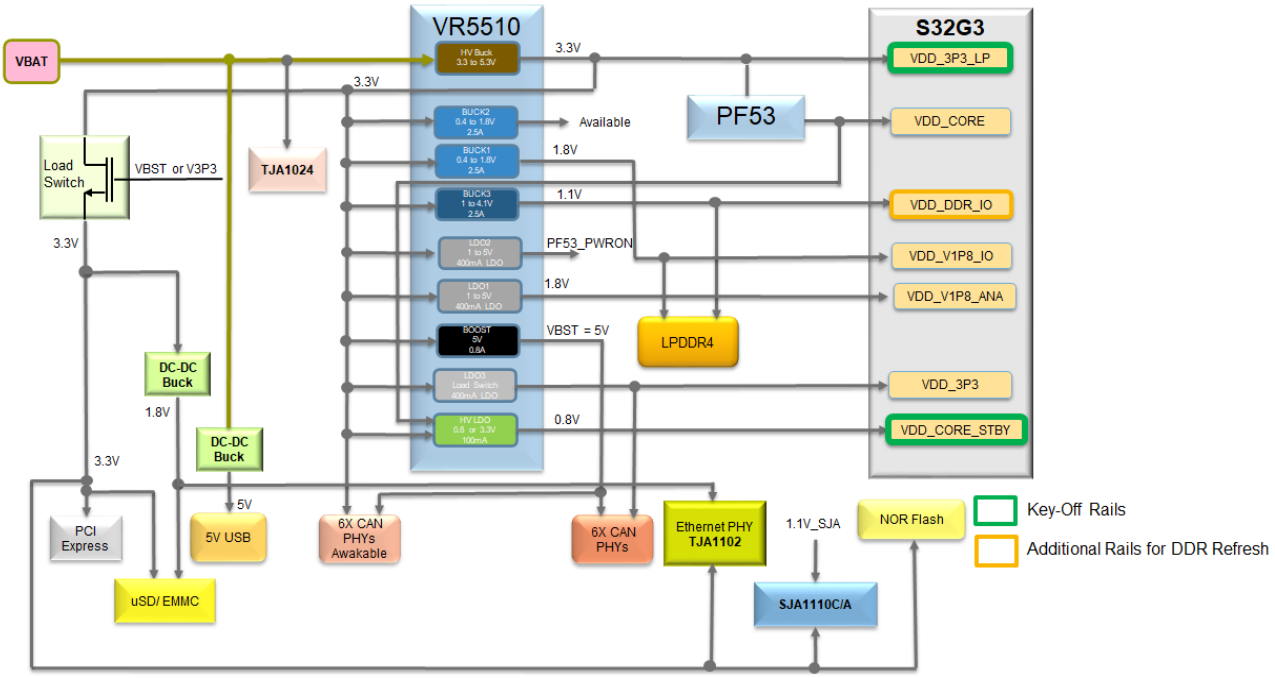

Figure 1. **Power tree**

When designing an application, the power requirements of the application need to be derived to ensure the functional as well as thermal feasibility of the application. The below sections provides help to the system designer to work out an optimal power topology for their application.

5. S32G3-PMIC power budgeting

Power consumption on 0.8 V rail is the major difference between S32G3 and S32G2. As such an additional regulator (PF5300) is recommended to provide the 0.8 V supply to the S32G3. The PMIC solution of VR5510+PF5300 is capable of meeting S32G3 power requirements. The different power rails are capable of handling different loads and must be used appropriately.

The S32G3_PowerEstimator (see attached) is intended for a quick sanity check of power scheming of S32G3 based applications and to provide an idea of the load on various PMIC power rails. Below are further details on S32G3_PowerEstimator usage.

The '*S32G3 Silicon Power*' sheet in S32G3_PowerEstimator is filled with inputs from the device datasheet and is used as a reference in the '*S32G3 Power budget example*' sheet. Since the sheet contains static values from the datasheet, it is not intended to be modified and hence is configured as a protected sheet. The sheet groups the S32G3 supply pins as per the applicable voltage. The sheet only uses max values since these are the ones that need to be taken care of when designing a system.

The '*S32G3 Power budget example*' sheet is user configurable and can be used to estimate the load on various power rails of the PMIC. The sheet groups power supplies as per PMIC output rails as the constraint on available power comes from the PMIC side. The application designer needs to configure the 'Conditions' column from the available drop-down menu wherever applicable. The 'Power Max'

column accordingly gets updated with the corresponding data referenced from the *S32G3 Silicon Power* sheet.

The *'S32G3 Power Budget example*' sheet can also be observed to see if some of the power rails of the PMIC can be used for supplying power to components other than the S32G3. This sheet already shows examples of adding LPDDR4, QSPI flash, and USB PHY on the PMIC power rails. Power consumption of the additional external components can be accommodated through the ‘Additional components’ rows. The designer must sum up the consumption of external components and provide this as an input in the relevant row. Each of the ‘total’ rows should be reviewed to confirm that the power limits of the PMIC voltage rail outputs are not breached.

Low power mode requirements must also be kept in mind when using this sheet to design the power tree of the system. Refer to S32G3HDG for further details.

In case a user is not using the recommended PMIC solution with S32G3, they can still use this sheet to estimate load and predict any overload condition. The limits on each of the power rails should be updated as per the power solution used.

Example Power Budgeting for S32G3 with VR5510

PMIC Power Rail	Components	Voltage	Power Max (mW)	Conditions (user selection using dropdown available in select cases)
PF5300 : VDD_0V8 typ_max: 15A Power_max: 12W	VDD, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR	0.8	8620.00	S32G399A, Sum of VDD, VDD_STBY, VDD_VP_PCIE0/1, VDD_LV_PLL, VDD_LV_PLL_DDR0, VDD_LV_PLL_AUR
BUCK1: VDD_IO_1V8 max: 2500mA Power_max_LDO2 = 4.5W	VDD_IO_QSPI	1.8	58	200MHz, clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle
	VDD_QSPI		252.00	MX25 VCC Read While Write, 200MHz 8IO DTR
	VDD_LPDDR4		25.00	All-bank REFRESH burst current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tRFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled
	Additional Components		0.00	Depending on application requirement, the supply rail may be connected to additional components.
	Total:		**335.00**	**The cell color changes to red if max power specs violated.**
BUCK2: 1V1 max: 2500mA Power_max_LDO2 = 4.5W		1.1		Available for application usage
BUCK3: VDD_1V1 typ_max: 2.5A Power_max_BUCK3: 2.75W	VDD_IO_DDR	1.1	625.00	LPDDR4, 3200 MT/s, 100% links, 16 data lines switching, 60 Ohm transmit termination driving a 60 Ohm load
	VDD_LPDDR4		420.00	Operating burst READ current, One bank is active; BL = 16 or 32; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled
	Additional Components		0.00	Depending on application requirement, the supply rail may be connected to additional components.
	Total:		**1045.00**	**The cell color changes to red if max power specs violated.**
LDO1: VDD_ANA_1V8 max: 400mA Power_max_LDO1 = 0.72W	IDD_EFUSE_PGM	1.8	252	Efuse programming current, should not be added to dynamic consumption as this would be one off exercise with most of other peripherals in stop mode
	VDD_PXOSC, VDD_HV_PLL_AUR, VDD_HV_ PLL_DDR0, VDD_ADC, VREFH_ADC0/1, VDD_FIRC, VDD_VREF, VDD_HV_PLL, VDD_EFUSE(Read)		135	Does not include the IDD_EFUSE_PGM numbers which would be required instantaneously only when most other current consumption would be absent.
	VDD_IO_PCIE0/1		152.00	PCIe0/1, All circuits enabled, Gen3 8Gbps, 2 lanes
	VDD_IO_GMAC		81	RGMII 125MHz, 100% clock rate, 50% data rate, 1/2 data switching per cycle, per IP instance
	VDD_IO_AUR		164	5Gbps on 4 lanes, 50% Activity Rate, 1/2 data switching per cycle
	VDD_IO_USB		59.00	modem - 8 outputs @60MHz, 50% data rate, 1/2 data switching per cycle
	VDD_ULPI_PHY		58.00	high-speed transceiver, continuous transmission
	Additional Components		0.00	Depending on application requirement, the supply rail may be connected to additional components.
	Total:		**649**	**The cell color changes to red if max power specs violated.**
LDO2: 1V8 max: 400mA Power_max_LDO2 = 0.72W	PF53_PWRON	1.8	0	The PWRON signal should not have any noteworthy consumption
				Available for application use
LDO3: VDD_IO_3V3 max: 400mA Power_max_LDO3 : 1.32W		3.3		Use case specific
Vpre: VDD_3V3	VDD_STBY_IO	3.3	0.11	Ta = 25C, VDD_IO_STBY = 3.0V, typical silicon, all pull up/down disabled
	VDD_3V3_STBY_BRD			Typically depends on IO usage
HVLDO: VDD_STBY_0V8 max: 100mA	VDD_STBY	0.8	0.058	Ta = 25C, typical silicon, all pull up/down disabled

Figure 2. **S32G3 power budget example**

6. S32G3 IO power estimation

The S32G3_IOpower_calculator (xlsx attached) can be used to estimate dynamic IO current for the different IO rails. This can then be added to the static power specifications as provided in the device datasheet to estimate the total power on any of the IO rails. There are changes in the static I/O power (refer to the device datasheet) but the dynamic I/O power is same on both the S32G3 and S32G2 devices.

The ‘Overview’ sheet provides a summary of different specified or calculated current parameters and also specifies the IO power estimator use case.

The ‘*1.8 V*’, ‘*3.3 V*’, and ‘*3.3 VSTB*’ sheets details all the IOs available in respective voltage domains. The green fields in these sheets are modifiable and require you to fill in the inputs as per the activity expected on these IOs. Enabling an IO turns the row blue in the sheet. The dynamic consumption estimate of an IO is calculated based on the activity filled in a row. The total current consumption and total power consumption of all IOs in a VDD domain is calculated and populated at the bottom right of the sheet.

Port	Function	Module	Description	Direction	Pad Type	I/O Power Segment	I/O voltage [V]	Enabled	Frequency [MHz]	Activity	SRE	Cload_total [pF]	CeffIO [pF]	Dynamic [mA]
PF_03	GPIO[83]	SIUL_CC	General Purpose I/O 83	I/O	18GPIO	VDD_IO_CLKOUT	1.8				0	15.5		
PF_03	CLKOUT0	Misc	Clock Output 1	O			1.8				0	15.5		
PF_04	GPIO[84]	SIUL_CC	General Purpose I/O 84	I/O	18GPIO	VDD_IO_CLKOUT	1.8				0	15.5		
PF_04	CLKOUT1	Misc	Clock Output 2	O			1.8				0	15.5		
PF_05	GPIO[85]	SIUL_CC	General Purpose I/O 85	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_05	QSPI_DATA_A_O[0]	QuadSPI	QuadSPI A Data 0	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_06	GPIO[86]	SIUL_CC	General Purpose I/O 86	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_06	QSPI_DATA_A_O[1]	QuadSPI	QuadSPI A Data 1	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_07	GPIO[87]	SIUL_CC	General Purpose I/O 87	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_07	QSPI_DATA_A_O[2]	QuadSPI	QuadSPI A Data 2	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_08	GPIO[88]	SIUL_CC	General Purpose I/O 88	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_08	QSPI_DATA_A_O[3]	QuadSPI	QuadSPI A Data 3	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_09	GPIO[89]	SIUL_CC	General Purpose I/O 89	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_09	QSPI_DATA_A_O[4]	QuadSPI	QuadSPI A Data 4	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_10	GPIO[90]	SIUL_CC	General Purpose I/O 90	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_10	QSPI_DATA_A_O[5]	QuadSPI	QuadSPI A Data 5	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_11	GPIO[91]	SIUL_CC	General Purpose I/O 91	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_11	QSPI_DATA_A_O[6]	QuadSPI	QuadSPI A Data 6	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_12	GPIO[92]	SIUL_CC	General Purpose I/O 92	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_12	QSPI_DATA_A_O[7]	QuadSPI	QuadSPI A Data 7	O			1.8	Y	200	25%	0	15.5	13.6	2.6
PF_13	GPIO[93]	SIUL_CC	General Purpose I/O 93	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PF_13	QSPI_DQS_A_O	QuadSPI	Quad SPI A Data Strobe	O			1.8				0	15.5		
PF_14	GPIO[94]	SIUL_CC	General Purpose I/O 94	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PG_00	GPIO[96]	SIUL_CC	General Purpose I/O 96	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PG_00	QSPI_CK_A	QuadSPI	QuadSPI Serial Clock Flash A +	O			1.8	Y	200	100%	0	15.5	13.6	10.5
PG_01	GPIO[97]	SIUL_CC	General Purpose I/O 97	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PG_01	QSPI_CK_A_b	QuadSPI	QuadSPI Serial Clock Flash A -	O			1.8				0	15.5		
PG_02	GPIO[98]	SIUL_CC	General Purpose I/O 98	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PG_02	QSPI_CK_2A	QuadSPI	QuadSPI Serial Clock 2 Flash A +	O			1.8				0	15.5		
PG_03	GPIO[99]	SIUL_CC	General Purpose I/O 99	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PG_03	QSPI_CK_2A_b	QuadSPI	QuadSPI Serial Clock 2 Flash A -	O			1.8				0	15.5		
PG_04	GPIO[100]	SIUL_CC	General Purpose I/O 100	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PG_04	QSPI_CS_A0	QuadSPI	QuadSPI A Chip Select 0	O			1.8	Y	200	2%	0	15.5	13.6	0.2
PG_05	GPIO[101]	SIUL_CC	General Purpose I/O 101	I/O	18GPIO	VDD_IO_QSPI	1.8				0	15.5		
PG_05	QSPI_CS_A1	QuadSPI	QuadSPI A Chip Select 1	O			1.8				0	15.5		

Figure 3. **IO power estimator fixed voltage snapshot**

Additionally some of the IOs can be configured for both 1.8 V and 3.3 V operations. These are grouped in ‘*dual(VDD_IO_SDHC)*’, ‘*dual(VDD_IO_GMAC0)*’, ‘*dual(VDD_IO_GMAC1)*’ and ‘ *dual (VDD_IO_USB)*’ sheets. These sheets are also used in a similar way to the fixed voltage sheets. However, these sheets need an additional input in the form of operational voltage which needs to be filled at the bottom left of the sheet. The total power consumption is accordingly calculated in the sheet.

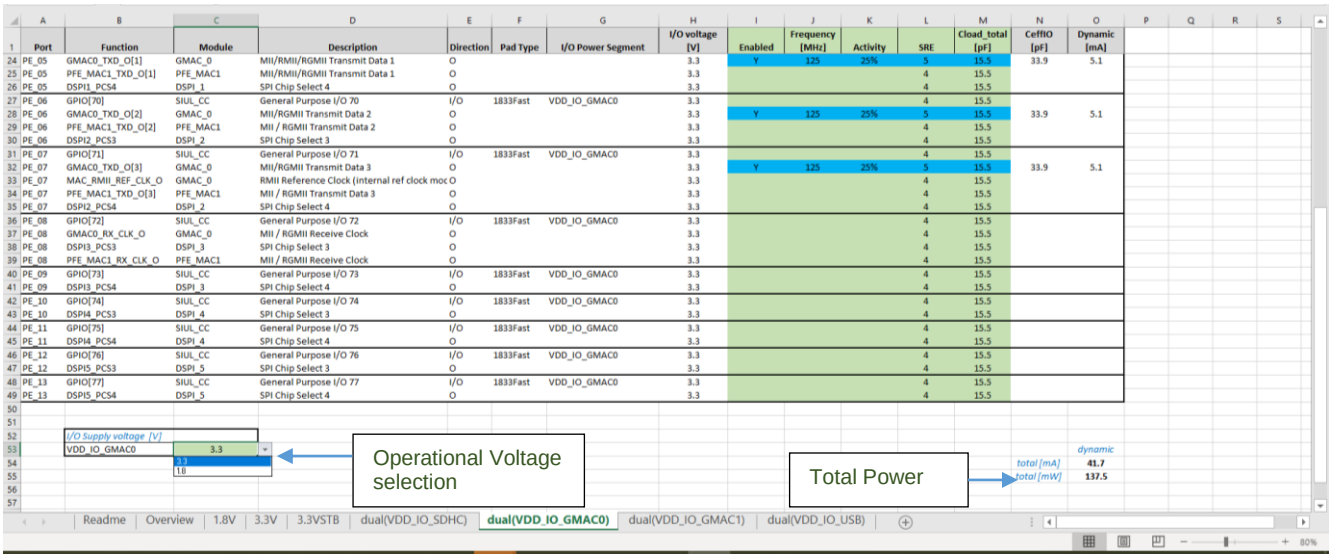

Figure 4. **Operational voltage selection in dual voltage sheets**

7. Additional considerations

7.1. Power impact for unused module

A system use case may not require each of the components powered by the 0.8 V supply. In such cases, the additional granularity may be required to find the reduced consumption on the respective power rail. The S23G3 does not offer power gating of modules, but there is the possibility to clock gate certain modules using the MC_ME. This means that the dynamic component of the power consumption for these modules would be saved when not using them. Below are the estimates for major modules on 0.8V rail based on module running at full speed with Tj as 125° C.

Table 1 Module power estimates

Core / Module	Dynamic Power (mW)
A53 Cluster (4 cores active – 1 GHz)	385
A53 Cluster (4 cores active – 1.3 GHz)	500
A53 Cluster (2 cores active – 1.3 GHz)	328
A53 Cluster (1 core active – 1.3GHz)	242
M7 Cluster (1 lock step instance)	51
DRAM Controller	473
PFE	165

Core / Module	Dynamic Power (mW)
LLCE	27
PCIe (per module)	82

It should be noted here that the figures provided in the above table are design estimates based on simulations only. As such these should only be used for guidance purpose and must not be treated as a specification. These values are for the VDD domain only and do not take into consideration any analog or I/O impact of the module. These should be calculated separately. The power consumption for cores take into account the core/cluster only and do not account for the corresponding savings in traffic across the bus fabric etc.

7.2. Power impact for reduced operation frequency

The impact of operational frequency on dynamic power should be assumed to be linear for further estimation. For example, if one Cortex-A53® core running at 1.3 GHz is estimated to consume ~90 mW then the same cluster when run at 650 MHz would consume ~45 mW.

7.3. Power profile with temperature

The power consumption of a module can be broadly divided into dynamic and static consumption. The dynamic component remains stable across temperature, however the static consumption varies with temperature. The graph below shows the leakage power (static component) on the 0.8 V VDD power domain across temperature for a device taken from the worst case leakage corner of the process. The graph is derived from limited bench experiments and hence should be taken only for guidance and should not be treated as a specification. The power shown in the below graph is for the 0.8 V VDD domain only and does not take into consideration any analog or I/O leakage power.

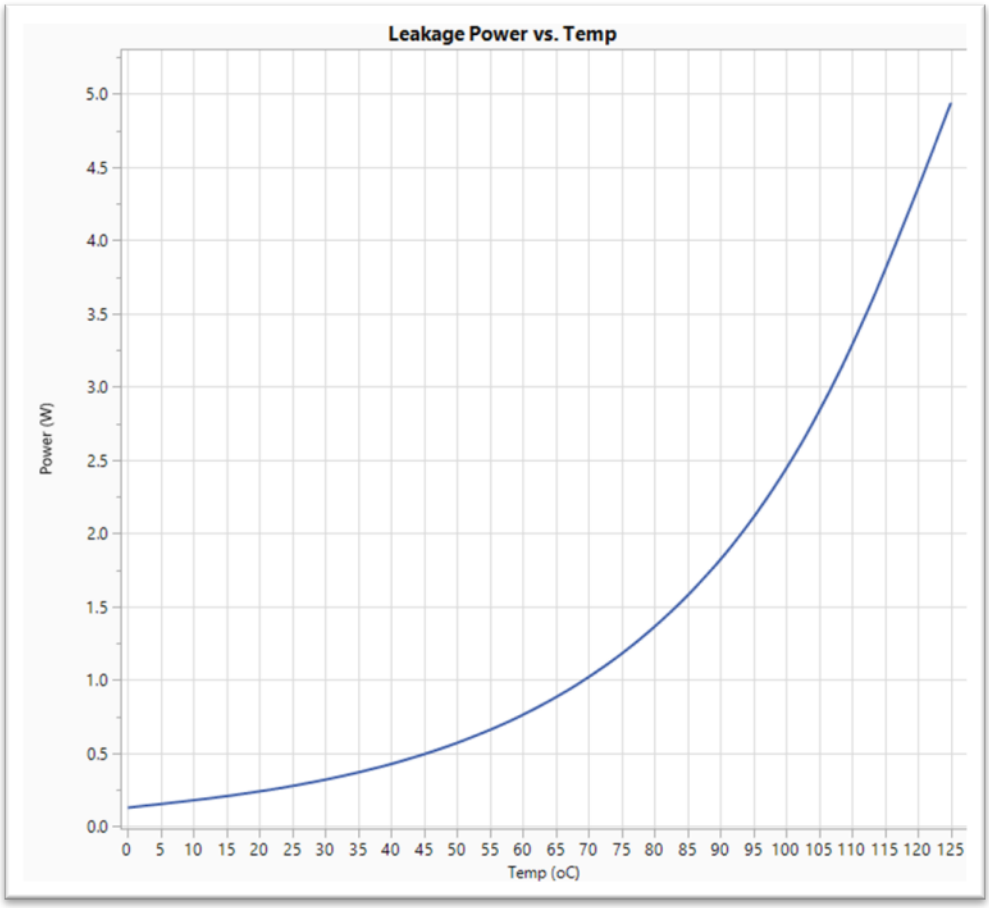

Figure 5. **0.8 V Leakage power vs temperature**

8. References

S32G3 Hardware Design Guidelines (S32G3HDG)

S32G3 Reference Manual

S32G3 Datasheet

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