AN13272

Power Management Solution for CV22/CV25

Rev. 1 — 6 August 2021 Product application note

Document information

Information	Content
Keywords	ASIL-B, ASIL-D, Power Management IC (PMIC), Ambarella CV22/CV25, PF8x00, ADAS, Infotaintment, Total Power Tree
Abstract	The PF8x00 family represents NXP’s current line of high-integration/high performance Power Management ICs (PMICs). They are widely used in ADAS, infotainment and other complex automotive applications. As a one chip power solution, the PF8x00 can be used to attach to Ambarella's CV22/25. NXP also provides a total power solution for CV22/25 power requirements with a highly functional safety level.

Revision History

Table 1. Revision history

Revision	Date	Description
AN13272 v.1	20210806	Initial Release
Modifications	NA	

1 Introduction

The PF8x00 family represents NXP's current line of high-integration/high-performance Power Management ICs (PMICs). PF8x00 devices are widely used in ADAS, Infotainment and other complex Automotive applications. As a single-chip power solution, PF8x00 devices meet all Ambarella CV22/CV25 power rail and functional safety requirements. The PF8x00 PMIC has been chosen to supply CV22/CV25 on the Ambarella Reference Design.

This application note describes how PF8x devices can be used to supply an Ambarella CV22/CV25 SoC. Besides the single-chip power solution, the application note introduces the Total Power Tree solution for CV22/CV25 systems, which includes the MCU and peripherals. The Total Power Tree solution achieves all the power requirements of CV22/CV25 system, including the functional safety and Low-Power Wake Up function.

The document also describes functional safety and power designs that help achieve ASIL-D(B) system levels using NXP's 3rd Generation Functional Safety PMICs.

The goal of this application note is to help customers quickly and efficiently design power networks for CV22/CV25 systems, especially for DMS, AEB, FCW and other Computer Vision Systems in Automotive applications.

2 Ambarella CV22/25 SoC and NXP PMIC Overview

Ambarella's AEC-Q100 qualified CV22/CV25 SoC combines image processing, 8MP30 video encoding, and CV flow computer vision processing in a single, low-power design that targets ADAS, electronic mirror, surround view, and drive recorder solutions.

Figure 1 shows the system structure of the CV22/CV25 AQ SoC:

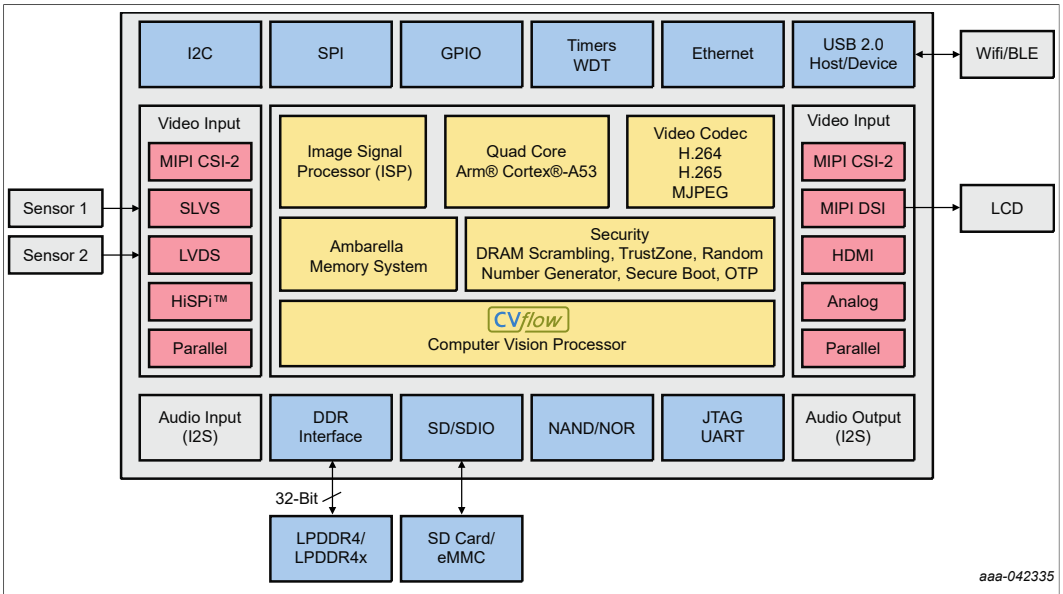

Figure 1. CV22/CV25 AQ System Block Diagram

The PF8x00 family offers highly integrated PMICs designed for high-performance processor-based systems. Each device includes seven high-efficiency bucks and four LDOs to supply power to the processor, memory, and miscellaneous peripherals. Each buck regulator has a 2.5 A stable current capability and the BUCKs can work in multi-phase mode to supply up to 10 A current to the system. Each LDO regulator can output

400 mA current with low drop-out voltage and can be set to work as one Load switch. An always-on LDO (VSNVS) has a10 mA current capability to supply the RTC. The voltage and power-up and power-down sequence of PF8x00 power channels can be set by One-Time-Programming (OTP), thereby allowing customers to power their system without additional software development.

The PF8x00 family includes the PF8100 and the PF8200. The PF8100 can be used to supply the CV22/CV25 AQ, which has no functional safety design requirements. The PF8200 is used to supply the CV22FS in order to support ASIL-B systems. Figure 2 shows a block diagram of a PF8x00 family device.

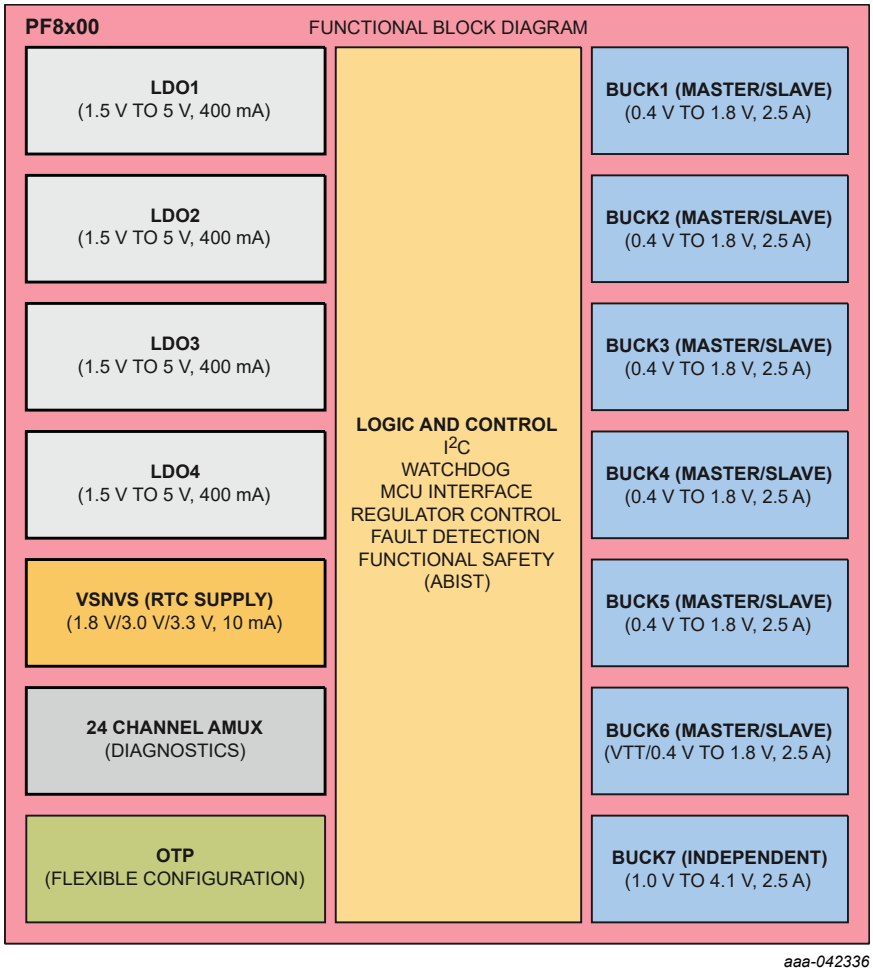

Figure 2. PF8x00 Family Device Function Block Diagram

Because the input voltage range of the PF8x00 is 2.5 V–5.5 V, a front power converter is needed to supply the device from a 12 V or 24 V vehicle battery. To meet that requirement, NXP offers the FS56 and FS85 as high-voltage PMICs that can be connected directly to 12 V or 24 V batteries. Furthermore, FS56 and FS85 devices can also provide power to the MCU and other system peripherals. In addition, the devices can provide high functional safety features if the customer requires it.

Figure 4 show a block diagram for the FS56 and FS85 family devices.

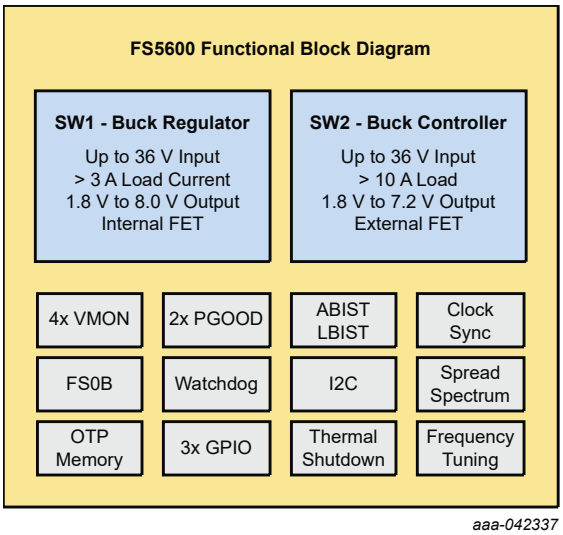

Figure 3. FS5600 Family PMIC Function Block Diagram

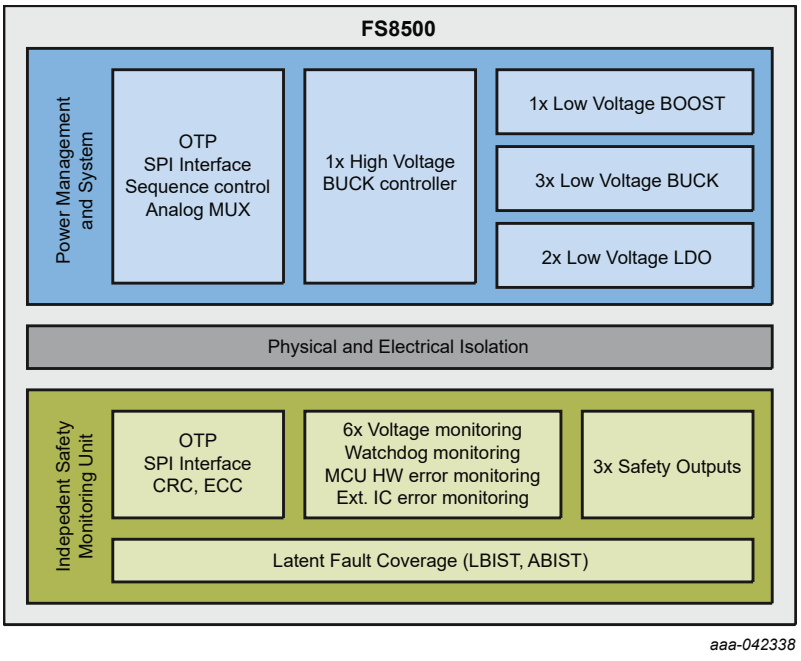

Figure 4. FS8500 Family PMIC Function Block Diagram

3 Power Solution for CV22/25

3.1 One chip power solution for CV22/CV25

PF8x00 family PMIC is capable of independently suppling all CV22/CV25 power rails, including the DDR and other memory power requirements. Section 3.1 shows a one-chip power solution with a PF8100 supplying a CV22/CV25 SoC. In this solution, the PF8100 input (SYS_5V) is 5 V. All power rails and some I/O function are described in the diagram.

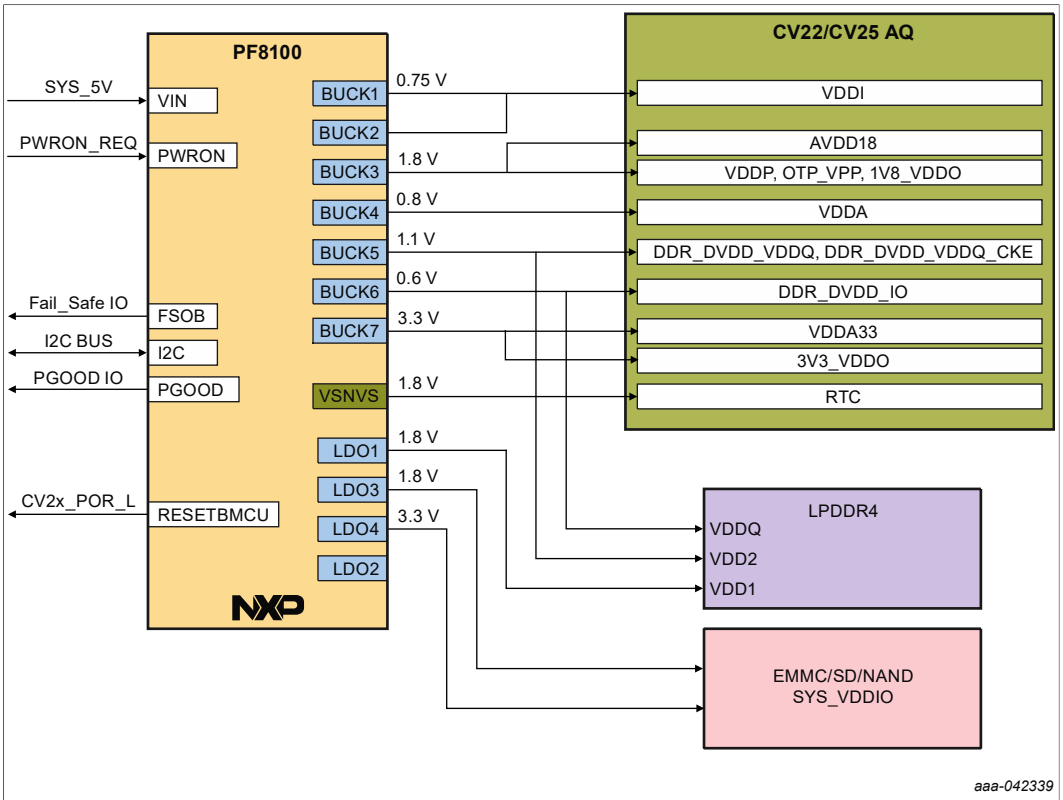

Figure 5. PF8100 One chip power solution for CV22/CV25

Table 2 shows the design parameters of a PF8100 attached to a CV22/CV25.

Table 2. PF8100–CV22/CV25 design parameters

CV22/CV25 Power rails	Voltage(V)	Max Load(mA)	PF8100 output	Current Capability(A)	Power Up Delay
VDDI	0.75	4400	BUCK1	5	0
			BUCK2		
VDDP, OTP_ VPP,1V8_VDDO	1.8	100	BUCK3	2.5	30 ms
VDDA18					
VDDA	0.8	120	BUCK4	2.5	0
DDR_DVDD_VDDQ	1.1	800	BUCK5	2.5	30 ms
DDR_DVDD_IO	0.6	1000	BUCK6	2.5	30 ms
AVDD33	3.3	100	BUCK7	2.5	60 ms
3V3_VDDO					
VDD1 of LPDDR4	1.8	-	LDO1	0.4	30 ms
EMMC/SD	1.8	-	LDO3	0.4	60 ms
SYS_VDDIO	3.3	10	LDO4	0.4	60 ms
RTC	1.8	0.003	VSNVS	0.01	Always on when VIN>UVDET

- For the CV22/CV25 power solution, the PF8100 output voltage and the power-up and power-down sequence for the CV22/CV25 are defined in OTP. If VIN of the PF8100 is higher than UVDET, the power rails start up following the defined power-up sequence, as long as PWRON is pulled up. After all the power rails have started up, PGOOD and RESETBMCU on the PF8100 are released and the CV22/CV25 SoC system boots up. During system operation, the PF8100 can still be controlled through I^2C, depending on system requirements.
- The CV22/CV25 ripple requirements are as follows: VDDI requires a maxim 4% ripple, and the other channels require a maxim 3% ripple. Based on the recommended hardware design, all PF8100 BUCKs can provide power output within 1% of the peak-to-peak ripple value in PWM mode.
- NXP provides several dedicated OTP versions of the PF8100 that meets the CV22/CV25 power-up and power-down sequence requirements by default. The PF8100 power-up and power-down sequence is shown in Figure 6.

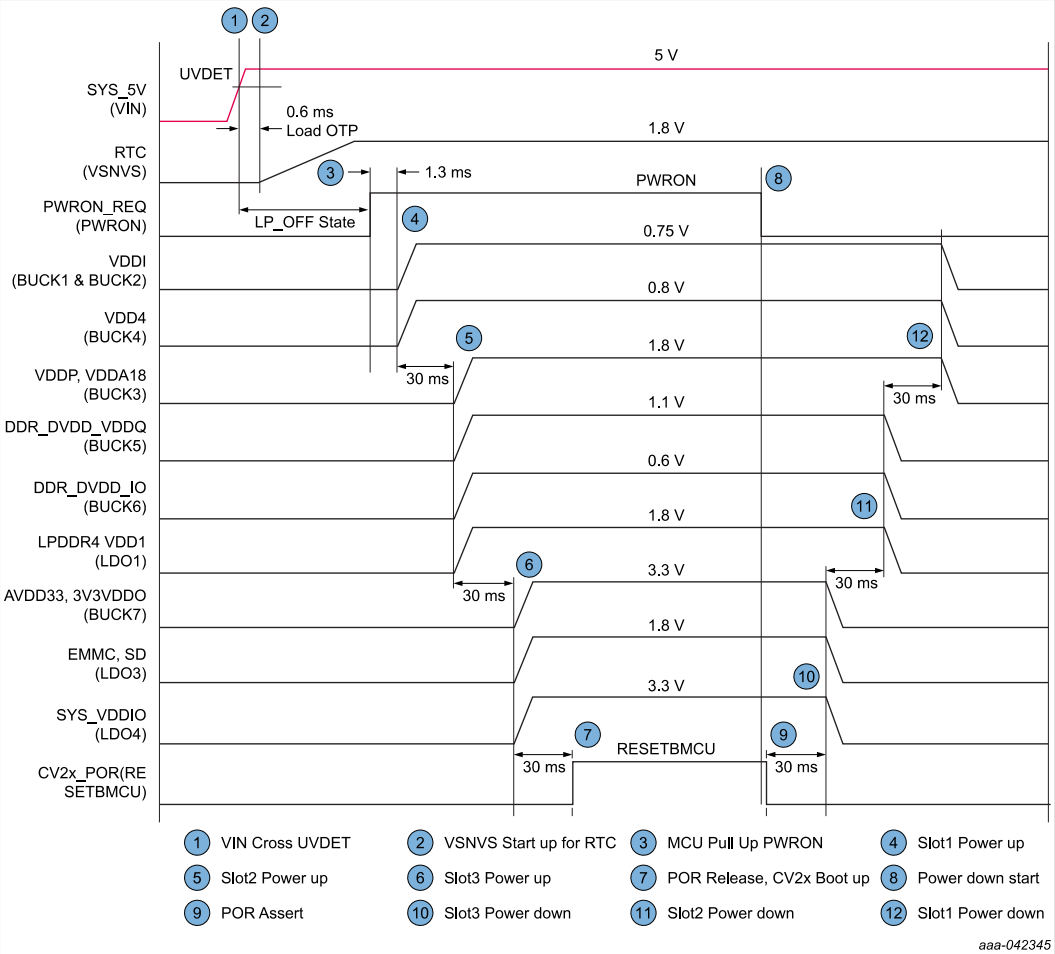

Figure 6. Power up and Power down sequence of PF8100 for CV22/CV25

- PF8100 has good thermal performance with an ambient operation temperature from −40 °C to 105°C. Assuming no additional readiating designs are involved, the PF8100 has no thermal issues when powering the CV22/CV25 SoC.

3.2 Board power solution for CV22/25 based system

NXP offers complete board-level power solutions for CV22/CV25 designs with a variety of system requirements. Figure 7 shows a typical solution for a 12 V battery system.

In this example, the FS56 provides power inputs to the PF8100 and other peripherals. The current capability of FS56 SW2 is greater than 10 A. SW1 provides 1.8 V–8.0 V, 3 A high efficiency power for the MCU and other peripherals. ENs on the FS56 can be connected to the ignition signal or the CAN Phy wake-up signal, based on the customer's real use cases.

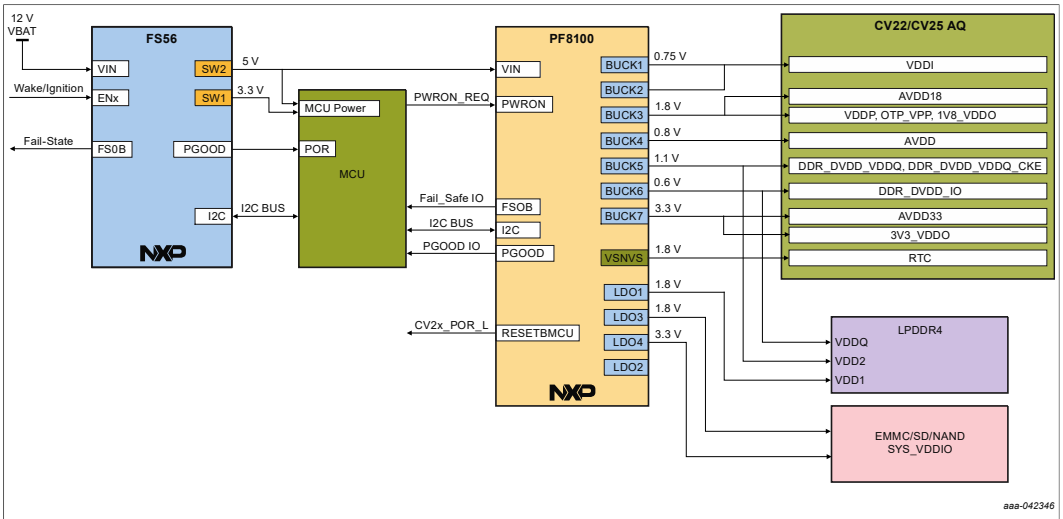

Figure 7. FS56+PF8100 Board solution for CV22/CV25

For 24 V and 12 V battery compatible systems, the power solution can be designed as shown in Figure 8. In addition, the FS85 is capable of supporting ASIL-D systems and is suitable for powering and securing safety MCU's which require ASIL-D(B) level compliance.

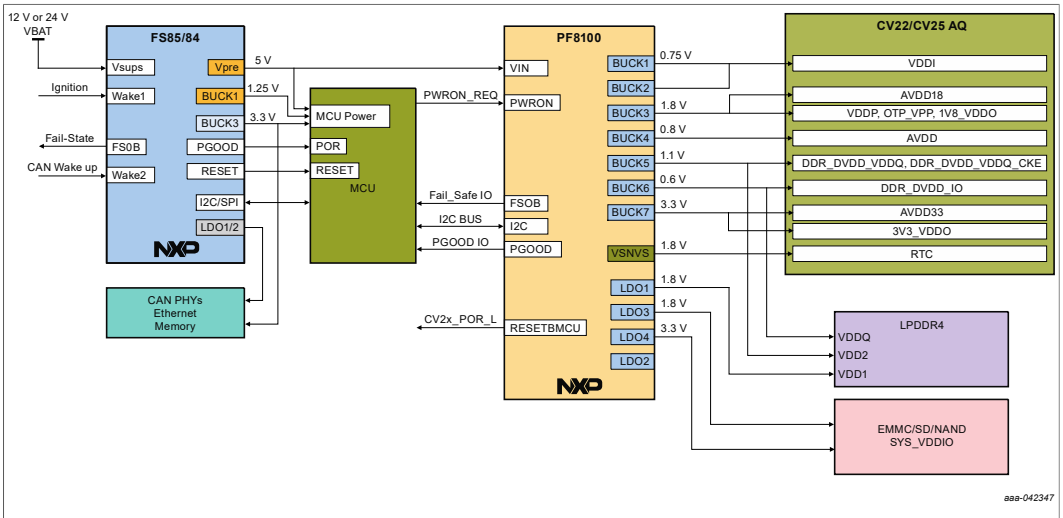

Figure 8. FS85/84+PF8100 Board solution for CV22/CV25

For customers who need power rail board solutions for other functions (for example, cameras), NXP offers the PF502x and PF52 family of devices, which work in conjunction with the PF8x00 to synchronize the power-up\down sequence and to manage faults. For more details on Multi-NXP PMIC power solutions, contact NXP local technical support.

4 Functional Safety Design

The FS56, FS85, and PF8x00 family of PMICs represent NXP's 3rd Generation Functional safety PMICs. Regardless of the process or the architectural design, the product lifecycle meets ISO26262 requirements. Customers can use NXP PMICs directly to achieve system level power functional safety and nearly all the safety mechanisms are implemented by hardware inside the device.

To meet Vision System's functional safety requirements for commercial and passanger vehicle ADAS or DMS designs, Ambarella provides their first ASIL-B processor, the CV22FS. The CV22F offers a wide variety of built-in functional safety features designed for use in ASIL-B Vision Systems.

The PF8200 and PF8100 are pin-to-pin compatible and have the same power electrification parameters. The difference between the two is that, the PF8200 is suitable for ASIL-B systems and is designed to follow the System Element out of Context (SEooC) ISO26262 standard to help designers more easily achieve ASIL-B compliance. The FS85, on the other hand, is designed for ASIL-D target systems. It can be used to supply and monitor functional safety MCUs to help the system reach ASIL-D compliance.

The functional safety power design for CV22FS is shown in Figure 9. For additional functional safety details, contact NXP local technical support.

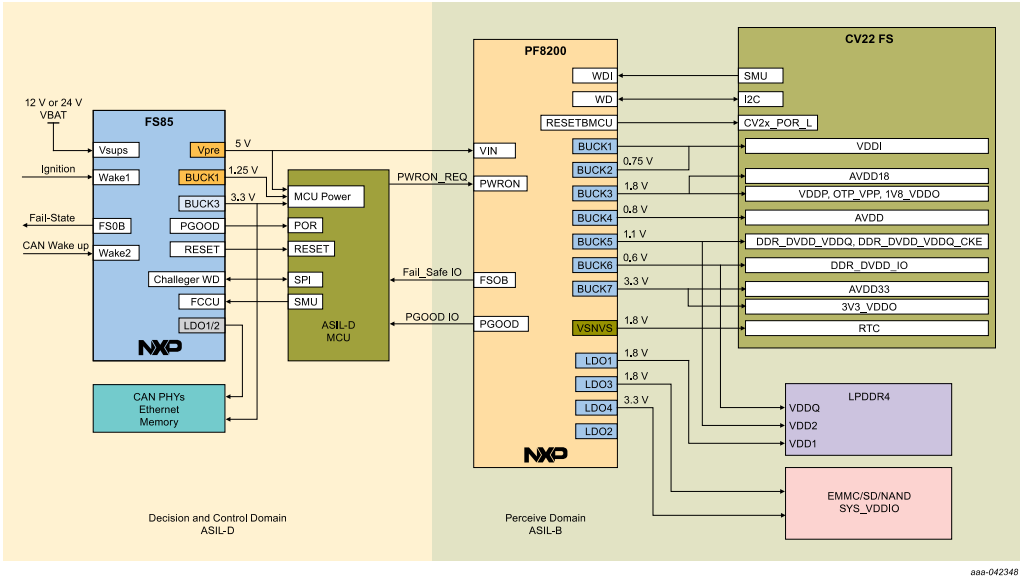

Figure 9. Functional safety power solution for CV22FS system

In this solution, all the power rails have their own real-time monitor. The Single Point Fault Metric (SPFM) of the Voltage Monitor can reach above 99% for an ASIL-D domain and above 97% for an ASIL-B domain. Inside the PMIC, BIST circuitry, redundancy band-gaps and oscillators are designed to make the Latent Fault Metric (LFM) of the Voltage Monitor function achieve about 90% for an ASIL-D domain and about 60% for an ASL-B domain. Probabilistic Metric For Hardware Failure(PMHF) of all the power deivces is much lower than ASIL-D requirements, which helps systems reserve more buffer for the System PMHF.

At the same time, NXP PMICs provide WD and hardware monitor functions for MCU and system diagnosis. These safety mechanism can be used at a system level to facilitate the safety design of the MCU and CV22/25. Several safety output IOs can be used to indicate failure and switch the system into a safe state. More details about the Functional safety design can be found in the FMEDA and Safety Manuels of NXP PMICs.

5 Schematic and BOM

The PF8100 is incorporated in the CV25 reference design board, so customers can get the reference design files from Ambarella directly. This section shows the recommended schematic for a PF82 used in a CV22/25 design. The BOM list associated with the schematic is included in Table 3.

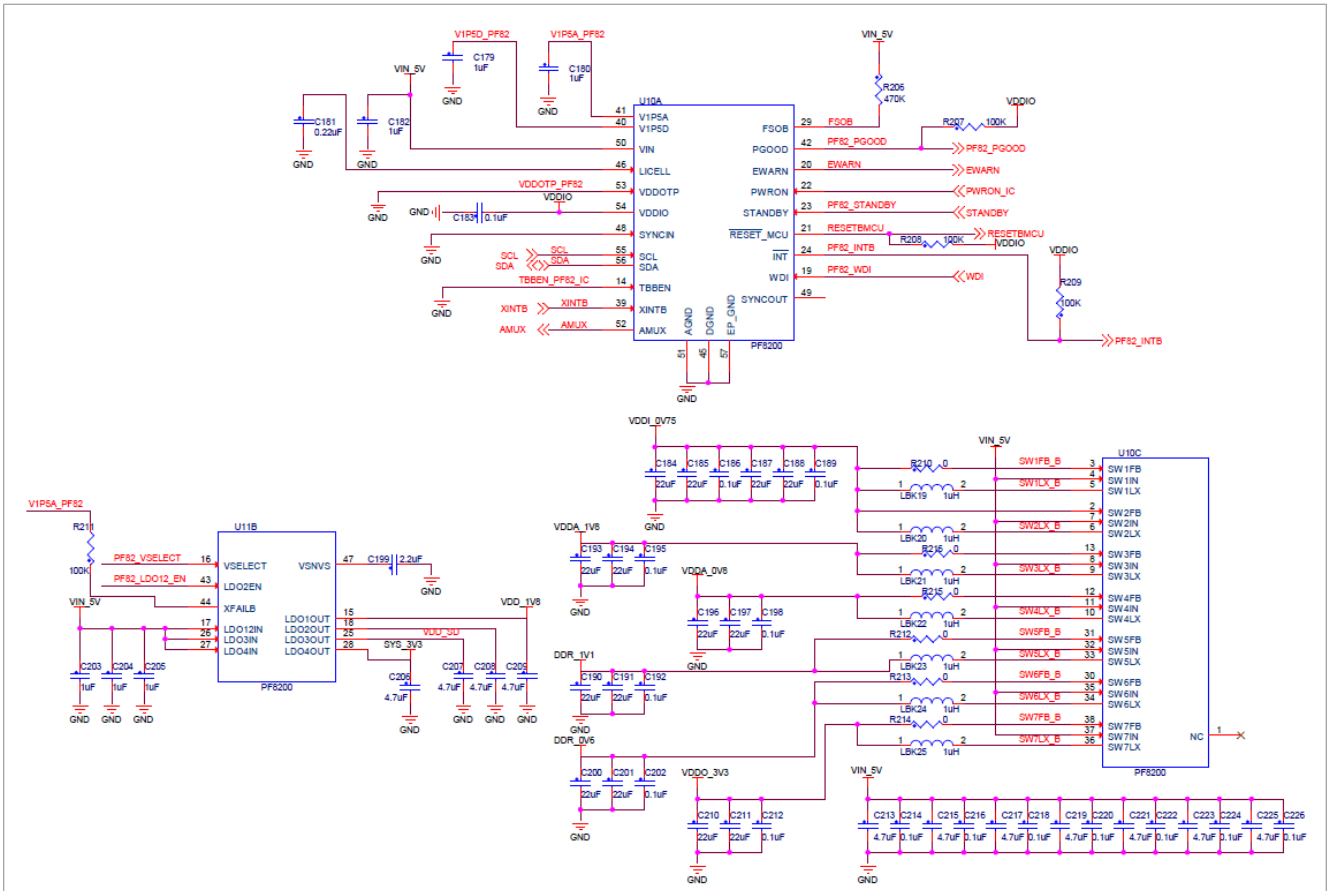

Figure 10. PF8100-CV25 reference design schematic

Table 3. BOM

Item	Quantity	Value	Package Size	Part Number	Company
1	6	1uF	0402	GCM155C71A105KE38D	MURATA
2	1	0.22uF	0402	GRT155C81E224KE01	MURATA
3	15	0.1uF	0402	GCM155R71C104KA55D	MURATA
4	14	22uF	0805	GRT21BC81A226ME13	MURATA
5	1	2.2uF	0402	GRT155C71A225KE13	MURATA
6	11	4.7uF	0603	GRT188C81E475KE13	MURATA
7	7	1uH	1210	TFM252012ALMA1R0MTAA	TDK
8	1	470K	0603	CR0603-FX-4703ELF	BOURNS
9	3	100K	0603	ERJ-2RKF1003X	PANASONIC

Table 3. BOM...*continued*

10	1	100K	0603	CRCW0402100KJNED	VISHAY INTERTECHNOLOGY
11	6	0	0402	ERJ-3GEY0R00V	PANASONIC
12	1	PF8200	QFN 8*8	MC33PF8200A0ES	NXP SEMICONDUCTORS

6 Reference Resource

In accordance with the NXP/Ambarella partnership, NXP offers fixed PF8100 OTP versions specfically for use with an attached CV22/25 device. PF8100 parts with the fixed OTP can be ordered directly from the NXP customer site. Customers can design their schematic using the existing OTP version. The mass production OTP version PF8100 for CV22/CV25 can be found below. For more details on the dedicated OTP version of the PF8100, contact NXP or Ambarella.

Table 4. PF8100 OTP Version for CV22/CV25

Part Number	Attach Processor	DDR	Comments
SC33PF8100JHES	CV22	LPDDR4	LDO2=1.5V
SC33PF8100F6ES	CV25/22(QM)	LPDDR4	VSNVS 3.3V/LDO2 3.3V
SC33PF8100G9ES	CV25/22(QM)	LPDDR4	VSNVS 1.8V/LDO2 3.15V

PF8100/PF8200 resource can be downloaded in the links below:

Table 5. PF8100/PF8200 resource links

Document and tool information	Link
Datasheet for PF8100/PF8200	Datasheet
Hardware Design Guide	AN12286
PF8200 / PF8201 Functional Safety Manual	UM11200 (Need NDA)
OTP Burn Board User Manuel	UM11162
OTP Board introduction	Overview
FlexGUI for PF8100/8200	Flex GUI
User Manuel for PF8100/PF8200 EVM	UM11160
PF8100/PF8200 EVM introduction	Overview
Embedded Software Driver	Overview

FS56 information can be found at the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/automotive-dual-buck-regulator-and-controller-with-voltage-monitors-and-watchdog-timer:FS5600

FS85 information can be found at the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-for-s32-microcontrollers-fit-for-asil-d:FS8500

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