NXP Semiconductors
Application Note

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Rev. 0, 01/2018

LS1012A silicon changes from revision 1.0 to revision 2.0

1 About this document

This document is intended for customers using LS1012A processor revision 1.0 based designs and need to migrate their designs to revision 2.0.

2 System and Processor version

This table provides a cross-reference to match the LS1012A revision level to the system version register (SVR). Software that uses the SVR, must take into account the changes in these values with LS1012A revision 1.0

Contents

Table 1. Revision Level to Part Marking Cross-Reference

Part	Revision	System Version Register Value	Note
LS1012A	1.0	0x8704_0110	Without Encryption
LS1012AE	1.0	0x8704_0010	With Encryption
LS1012A	2.0	0x8704_0120	Without Encryption
LS1012AE	2.0	0x8704_0020	With Encryption

Software needs to accommodate SVR update.

3 Errata fixed in LS1012A revision 2.0

This section describes the errata fixed in LS1012A revision 2.0

Table 2. Errata fixed in LS1012A revision 2.0

Errata	Title	SW Impact	HW Impact
Ethernet A-010336	SGMII operation requires common clock between PHY/ link partner and LS1012A	No	Yes For details, refer SGMII clocking scheme change
Ethnernet A-010904	2.5 SGMII is not supported.	No	No
Ethernet A-010897	Jumbo frame not supported.	No	No

NOTE

For complete list of LS1012A errata, refer LS1012ACE document.

Errata fixes have no impact on software implementation.

4 SGMII clocking scheme change

LS1012A revision 1.0 requires common clock for LS1012A and its link partner for proper operation of SGMII (10/100/1000/2500 Mbps). Refer erratum Ethernet A-010336.

Ethernet A-010336 is fixed in LS1012A revision 2.0.

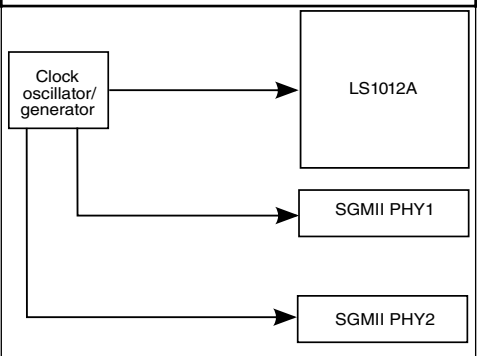
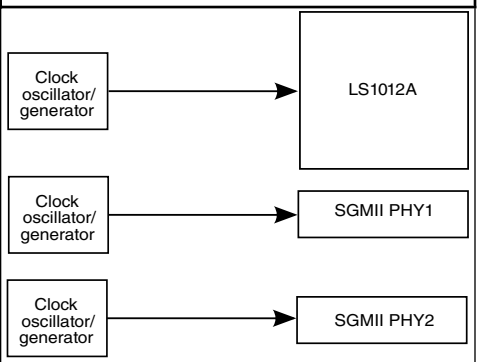
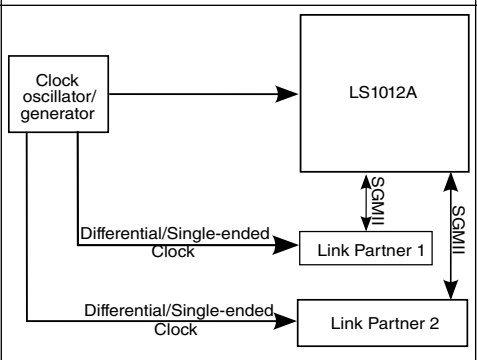
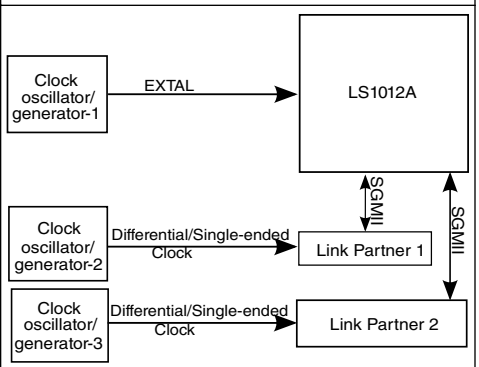
Changes in clocking requirement are shown below:

Table 3. MAC to PHY and MAC to MAC clocking scheme

Clocking scheme	Schemes supported by revision 1.0 and revision 2.0	Additional schemes supported by revision 2.0
MAC to PHY clocking scheme		

Table continues on the next page...

Table 3. MAC to PHY and MAC to MAC clocking scheme (continued)

Clocking scheme	Schemes supported by revision 1.0 and revision 2.0	Additional schemes supported by revision 2.0
		
MAC to MAC clocking scheme		

5 Functional changes in revision 2.0 from revision 1.0

This section describes the major functional changes applicable to LS1012A revision 2.0 from LS1012A revision 1.0.

5.1 RESET_REQ_B additionally multiplexed to CLK_OUT

This section describes additional multiplexing of RESET_REQ_B with CLK_OUT.

In LS1012A revision 1.0, RESET_REQ_B is multiplexed with QSPI_A_DAT3 signal hence limiting 4 bit QSPI mode with RESET_REQ_B.

In LS1012A revision 2.0, RESET_REQ_B is additionally multiplexed with CLK_OUT signal thus providing flexibility to support 4 bit QSPI along with RESET_REQ_B.

RCW Bit	Field Name	Revision 1.0	Revision 2.0
382	Reserved	Reserved. Must be set to 0.	Options:
383	CLK_OUT_BASE This field configures the functionality of the CLK_OUT pin.	Options: 0 GPIO1[31] 1 CLK_OUT	00 GPIO1[31] 01 CLK_OUT 10 RESET_REQ_B

RCW Bit	Field Name	Revision 1.0	Revision 2.0
			11 Reserved Note:Select RESET_REQ_B through either RCW[382:383] or RCW[QSPI_IIC2]. Selection of RESET_REQ_B in both RCW fields simultaneously is prohibited.

Impact:

Higher QSPI bandwidth is available with RESET_REQ_B.

5.2 Dependence of RESET_REQ_B selection on the ITS fuse

In revision 1.0, when ITS=1, RESET_REQ_B get mapped on QSPI_A_DATA3 pin. Hence LS1012A device cannot support 4-bit QSPI in secure mode.

The LS1012A revision 2.0 supports 4-bit QSPI in secure mode. In secure mode (ITS=1), user can choose to have RESET_REQ_B signal on CLK_OUT or choose to not pinout RESET_REQ_B.

Impact

LS1012A revision 2.0 can be configured in secure mode without RESET_REQ_B.

5.3 GPIO1[13] availability

In LS1012A revision 1.0, GPIO1[13] is not available with RESET_REQ_B. If RCW[QSPI_IIC2]=11, then the pin IIC2_SCL is always tristated.

In LS1012A revision 2.0, GPIO1[13] is available with RESET_REQ_B. If RCW[QSPI_IIC2]=11, then the pin IIC2_SCL is configured as GPIO1[13]. If backwards compatibility with revision 1.0 is required when using RCW[QSPI_IIC2]=11, then please ensure that GPIO1[13] is configured to be tristated.

RCW Bit	Field Name	Revision1.0	Revision2.0
424-425	QSPI_IIC2 Selects between GPIO's, IIC2, QSPI_DAT[2:3] and RESET_REQ_B	Options: 00 GPIO1[13], GPIO1[14] 01 IIC2_SCL, IIC2_SDA 10 QSPI_A_DATA2, QSPI_A_DATA3 11 Reserved, RESET_REQ_B	Options: 00 GPIO1[13], GPIO1[14] 01 IIC2_SCL, IIC2_SDA 10 QSPI_A_DATA2, QSPI_A_DATA3 11 GPIO1[13], RESET_REQ_B Note:Select RESET_REQ_B through either RCW[382:383] or RCW[QSPI_IIC2] Selection of RESET_REQ_B in both RCW fields simultaneously is prohibited.

Impact:

GPIO1[13] is available when RCW[QSPI_IIC2]= 11.

6 Additional Part of 1000MHz CPU core frequency

LS1012A revision 2.0 is available with additional core frequency of 1000MHz.

Table 4. Supported CPU frequency for LS1012A revision 1.0 and 2.0

	LS1012A revision 1.0	LS1012A revision 2.0
CPU Frequency supported	H = 800 MHz E = 600 MHz	K = 1000 MHz H = 800 MHz E = 600 MHz

7 DC power supply tolerance changes

Tolerance for DC power supply ($S1V_{DD}$, USB_SDV_{DD}, USB_SV_{DD}) is changed in revision 2.0.

Table below details the changes:

Table 5. Recommended operating condition changes between revision 1.0 and revision 2.0

Characteristic	Symbol	Recommended Value in revision 1.0	Recommended Value in revision 2.0	Unit
SerDes transceiver core and receiver power supply	$S1V_{DD}$	0.9 ± 30 mV	0.9 +50/-30 mV	V
USB PHY Transceiver supply voltage	USB_SDV_{DD}	0.9 ± 30 mV	0.9 +50/-30 mV	V
USB PHY Transceiver supply voltage	USB_SV_{DD}	0.9 ± 30 mV	0.9 +50/-30 mV	V

Impact

Tolerance for $S1V_{DD}$, USB_SDV_{DD}, USB_SV_{DD} has been increased on positive side.

8 Power up sequencing change

Table 6. Changes in USB supplies ramp up timing

Supply	Revision 1.0	Revision 2.0
Maximum time allowed for all USB supplies to ramp-up with respect to each other	10ms	95ms

9 Revision history

This table summarizes changes to this document.

Table 7. Document revision history

Revision number	Date	Change
0	01/2018	Initial public release

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