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Revisions			
Rev	Description	Date	Approved
B1	All unnamed nets have been named. Release to Production.	16-JAN-17	Didier Pagnoux
B2	Update R83 due to PN obsolescence	16-MAY-17	Didier Pagnoux

FRDMFS6522LAEVB

		Analog Sensor Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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ICAP Classification: CP: IUD: X PUBL:			
Designer: Didier Pagnoux	Drawing Title: FRDMFS6522LAEVB		
Drawn by: Didier Pagnoux	Page Title: TITLE, TOC & REV		
Approved: Didier Pagnoux	Size C	Document Number SCH-29303 PDF: SPF-29303	Rev B2
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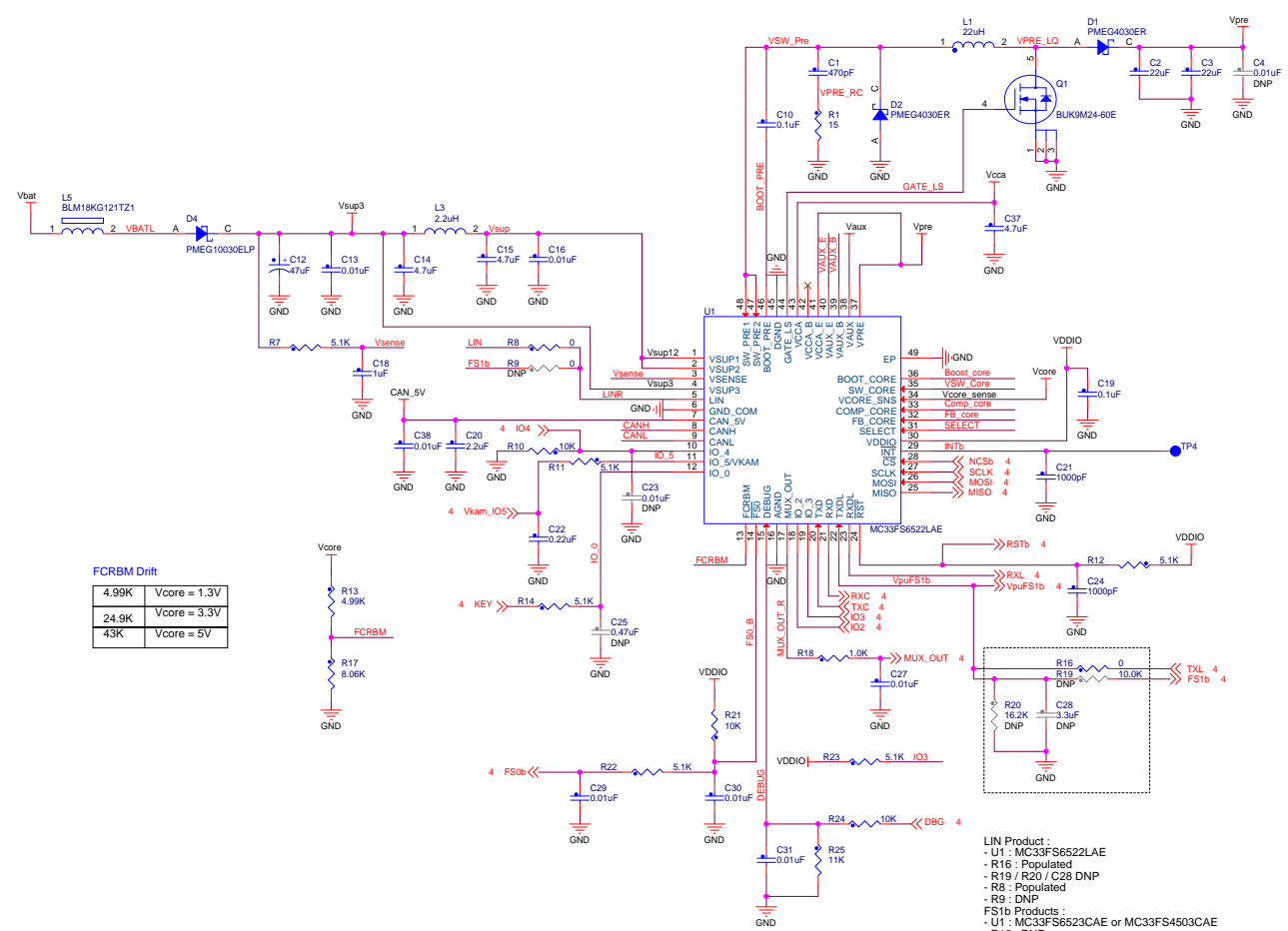
Configuration :

- DFS Enabled
- VDDIO connected to Vcca by default (MCU as an option)
- LIN option by default (FS1b not available)
- FS0b on VDDIO
- Vcore regulator set to 1.3V
- Vcca regulator set to 3.3V
- Vcca regulator using Internal PMOS (VCCA_E connected to Vpre)
- Vaux regulator set to 5V
- Vpre regulator configured in Buck or Boost mode

Note: PCB Layout is common to several MC33FSxxxx (U1) part numbers.
For this reason, the schematic gives some variant depending on the MC33FSxxxx installed on the board.

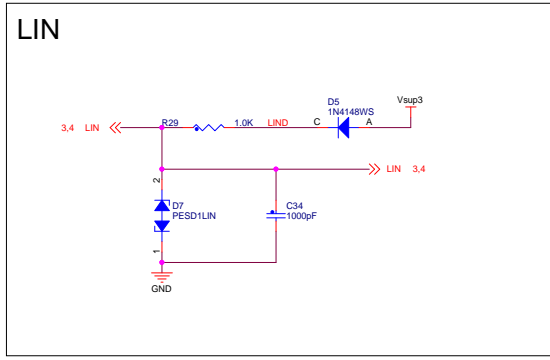
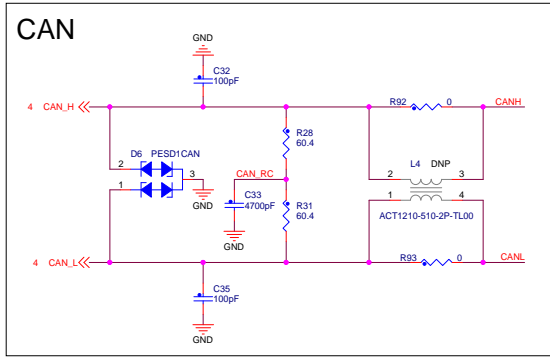
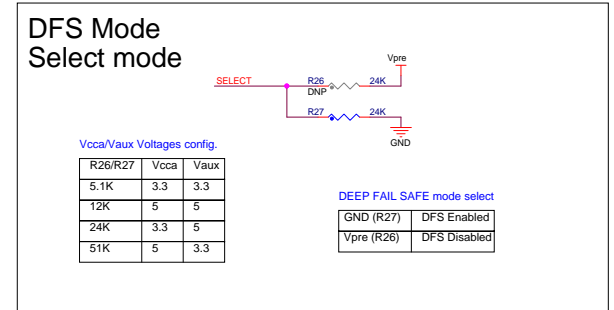
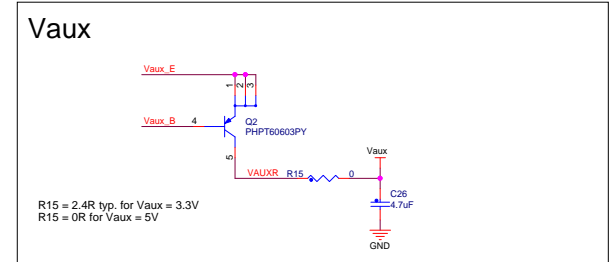
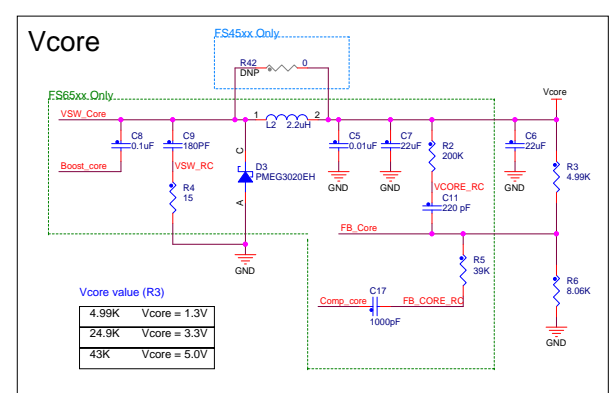


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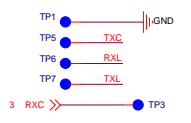
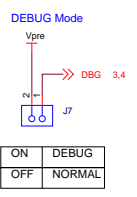
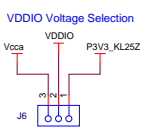
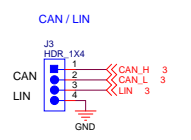
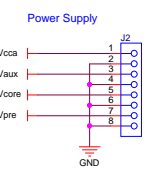
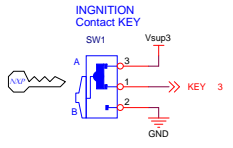
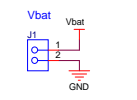


FCRBM Drift

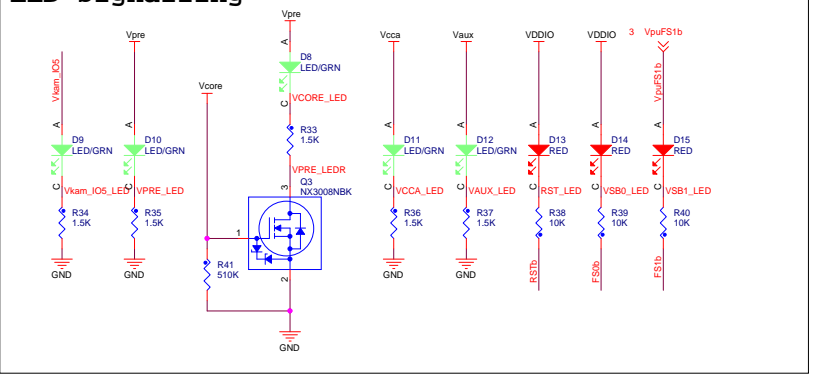
4.99K	Vcore = 1.3V
24.9K	Vcore = 3.3V
43K	Vcore = 5V



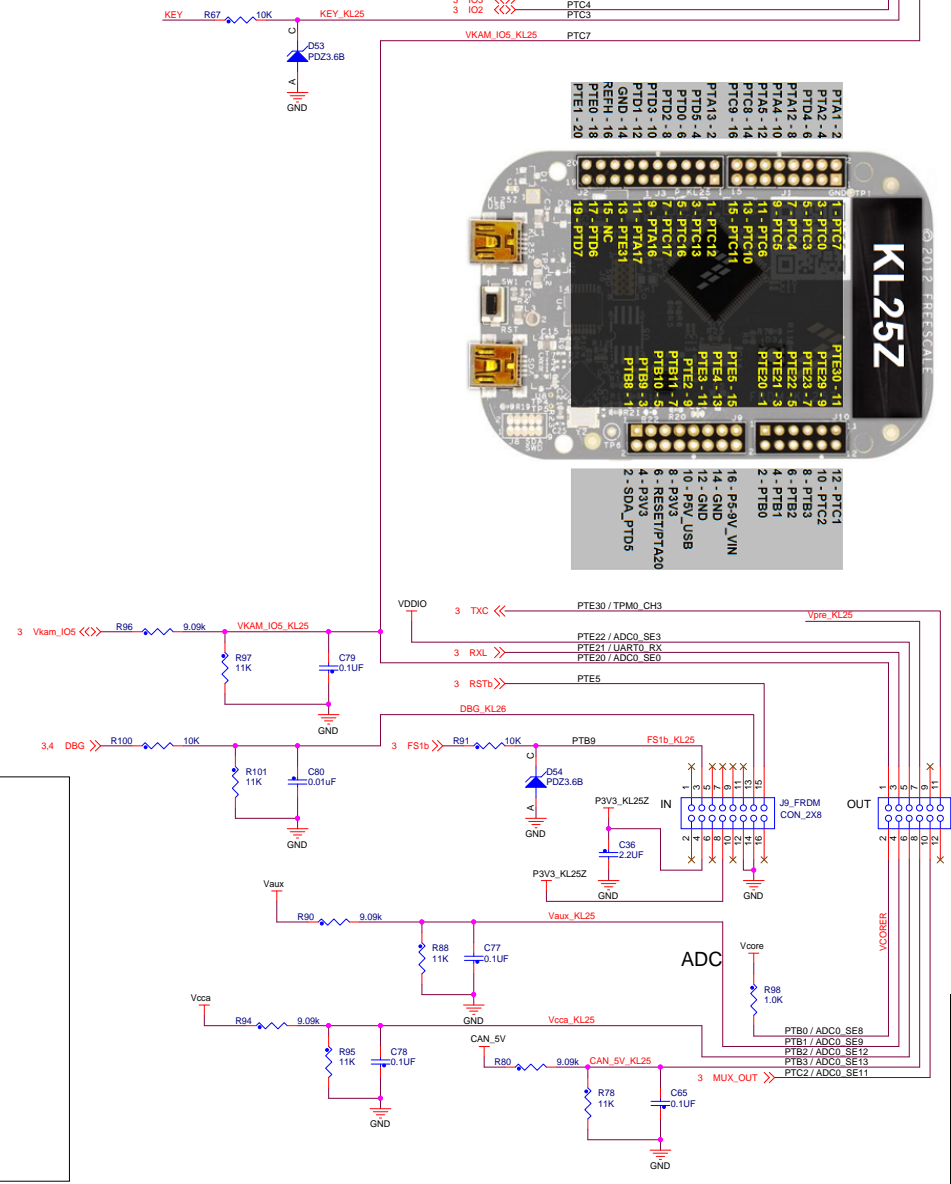
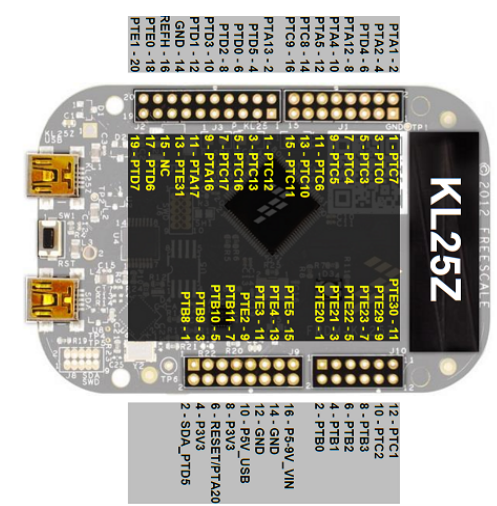
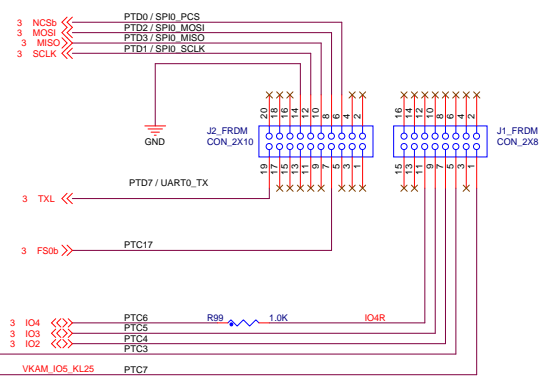
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LED Signalling



SPI



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