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Revisions			
Rev	Description	Date	Approved
X1	First Draft	2-FEB-21	Lucie Hernandez
A	Original Release	25-FEB-21	Lucie Hernandez

KITFS6507LAEEVM

		Analog Sensor Product Group	
		8501 Williams Cannon Drive West Austin, TX 78725-8598	
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Designer: F. Mias	Drawing Title: KITFS6507LAEEVM	ICAP Classification: CP:	IND: X PUR:
Drawn by: F. Mias	Page Title: TITLE, TOC & REV		
Approved: L. Hernandez	Size C	Document Number SCH-4820 PDF: SPF-4820	Rev A
Date: Friday, March 12, 2021	Sheet 1 of 4		

JUMPER TABLE

REF DES	JUMPER(DEFAULT)	PAGE NAME
J2,J12	1-2 3-4	03 - FS6507
J7,J26,J18,J9,J1,J27,J10,J3, J43,J11,J28,J16,J6,J21,J5, J25,J32,J35,J14,J15,J39	1-2	03 - FS6507
J38,J22	2-3	03 - FS6507
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DNP TABLE

REF DES	ASSY OPT	PAGE NAME
R108,TP8,C24,TP4,TP6,J41,C58, TP2,C55,J42,C26,R7,C11,C63, Q3,C59,R69,C92,C10,TP10,C54, R98,R107,C14	DNP	03 - FS6507
R91	DNP	04 - INTERFACE

SWITCH TABLE

REF DES	SWITCH	PAGE NAME
SW1	1: OFF 2:OFF 3:OFF 4:OFF	03 - FS6507
SW5	1: OFF 2:ON 3:OFF 4:OFF	03 - FS6507
SW3	1:OFF 2:OFF 3:OFF 4:OFF 5:OFF 6	04 - INTERFACE
SW6	1:OFF 2:OFF 3:OFF 4:OFF	04 - INTERFACE

Notes :

This Schematic is intended to support FS45XX and FS65XX family.

All the families will be supported on the same PCB.

As a consequence, the variation at schematic level are managed with components maked as "DNP"

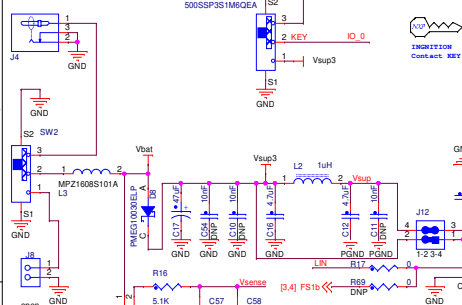
Board configured for MC33FS6507LAE

(Vcore DC/DC 2.2A - FS0b (no FS1b) - LDT - CAN & LIN)

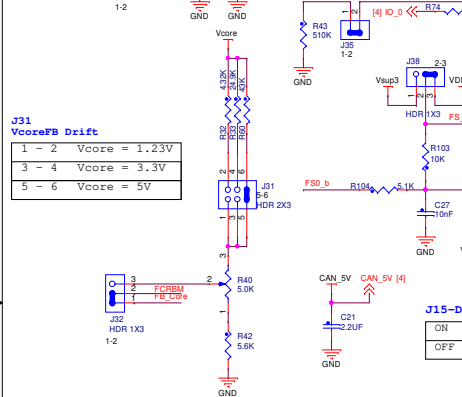


EAP Classification: CP: IUC: X PUBL			
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Page Title: NOTES			
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Vbat Jack



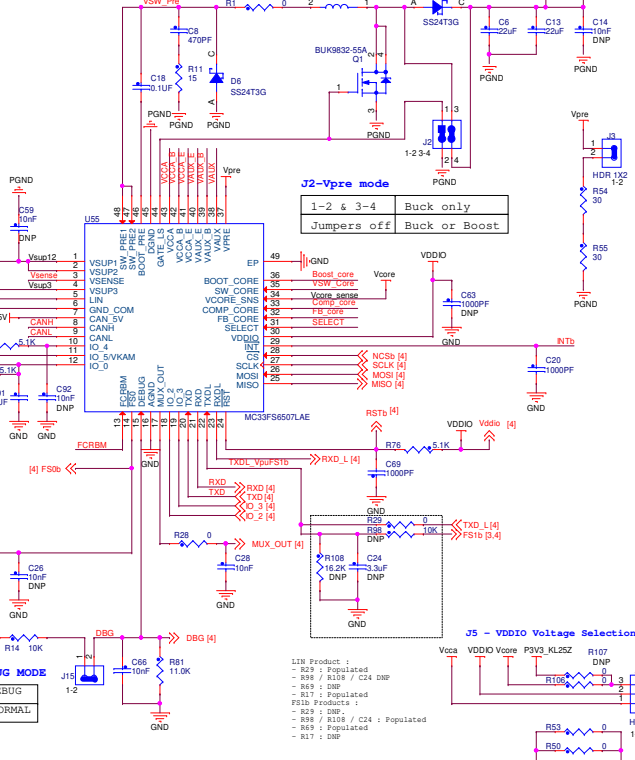
Vbat



J31

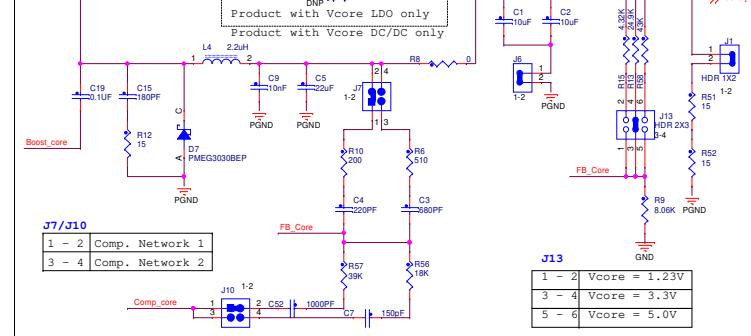
VcoreFB Drift

1 - 2	Vcore = 1.23V
3 - 4	Vcore = 3.3V
5 - 6	Vcore = 5V

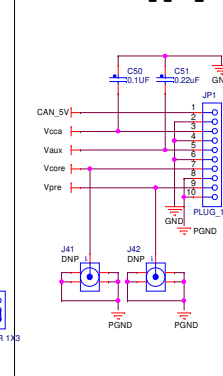


LIN Product :
 - R29 : Populated
 - R98 / R108 / C24 : DNP
 - R69 : DNP
 - R217 : Populated
 FS18 Products :
 - R29 : DNP
 - R98 / R108 / C24 : Populated
 - R69 : Populated
 - R17 : DNP

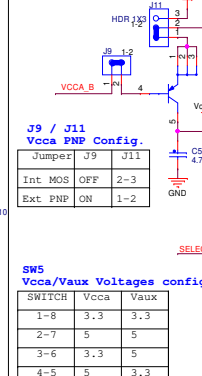
Vcore



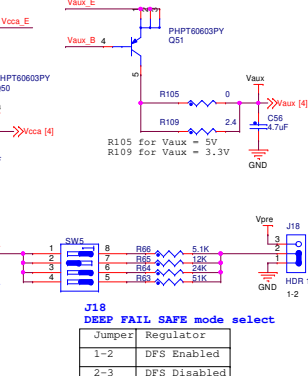
Power Supply



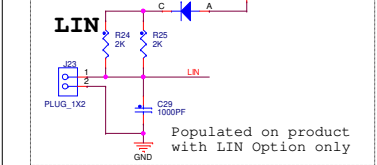
Vcca



Vaux

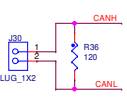


LIN

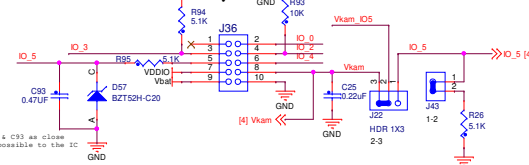


Populated on product with LIN Option only

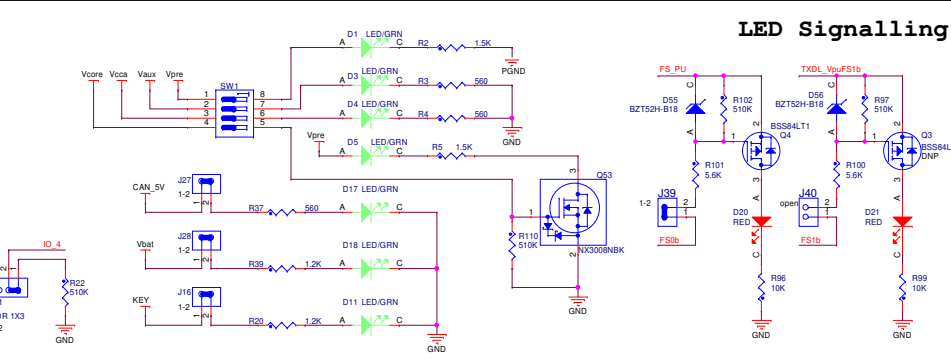
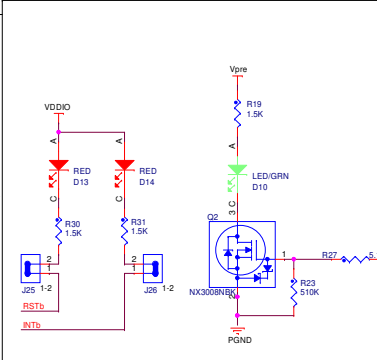
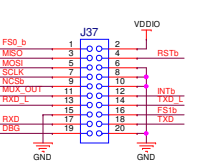
CAN



I/O



DEBUG

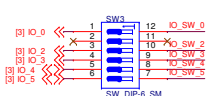


Test Points

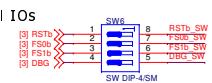
TP3 ● Vpre	TP11 ● Vcore	TP24 ● CANH
TP2 ● DNP	TP10 ● DNP	TP25 ● CANL
TP9 ● Vcca	TP7 ● Vaux	TP21 ● LIN
TP8 ● DNP	TP6 ● DNP	TP28 ● MUX_OUT
TP5 ● CAN_5V	TP16 ● Vaux3	TP30 ● FS0b
TP4 ● DNP	TP17 ● DNP	TP29 ● FS1b
TP12 ● DNP	TP22 ● DNP	TP28 ● RStb
TP31 ● DNP	TP14 ● DNP	TP15 ● VSW_Vcore
TP13 ● DNP	TP1 ● DNP	TP23 ● FCRBM
		TP19 ● SELECT

ICAP Classification: CP, IUC, X, PUB
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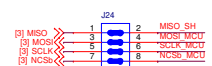
IOs



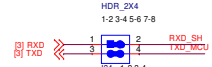
Special IOs



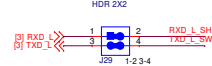
SPI



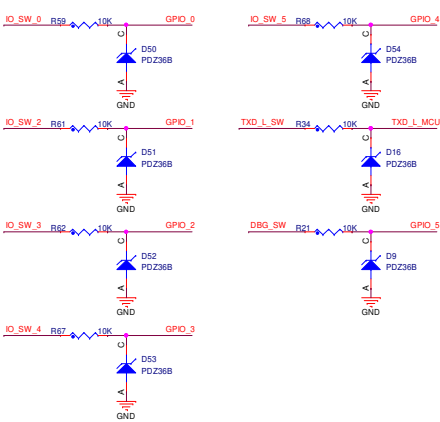
CAN



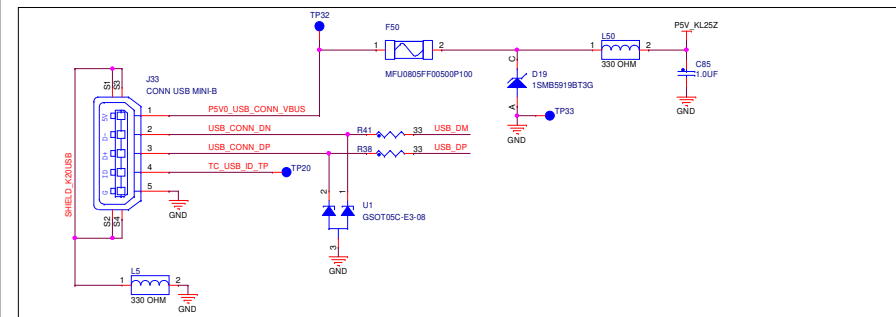
LIN



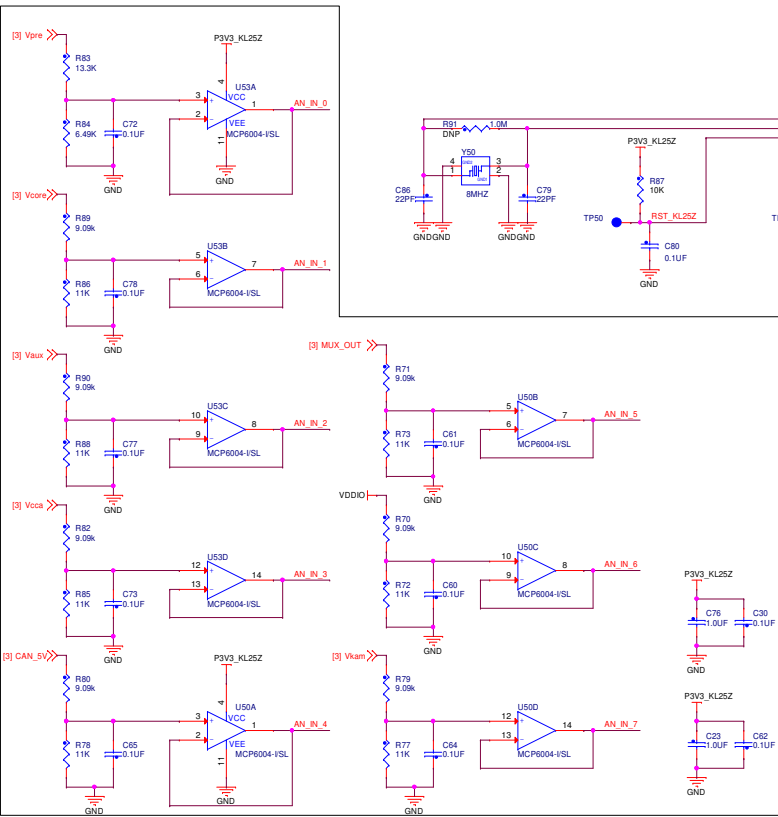
Digital IOs



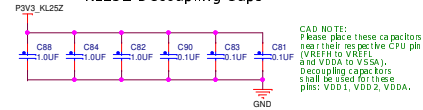
KL25Z USB CONNECTOR



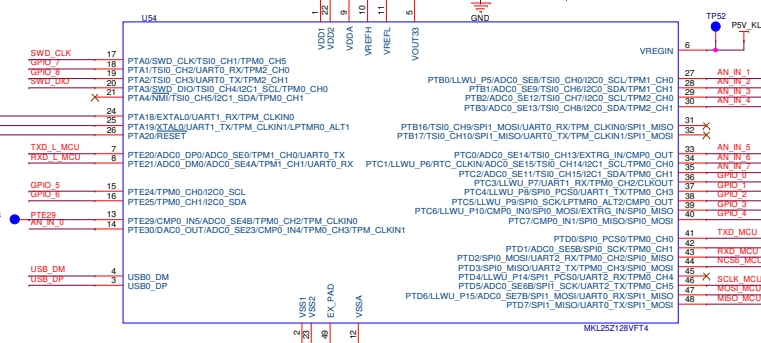
Analog Inputs



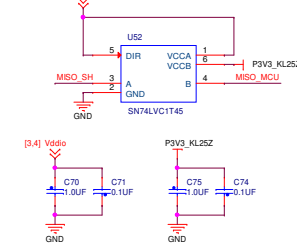
KL25Z Decoupling Caps



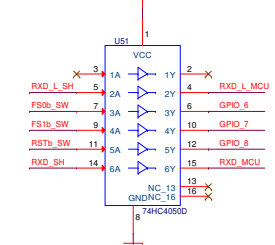
CAD NOTE: Please place these capacitors next to the positive CPU pin (VREFIN or VREF) and VDDA to VSSA. Decoupling capacitors shall be used for these pins: VDD1, VDD2, VDDA.



FAST HIGH_to_LOW Level Shifter



HIGH_to_LOW Level Shifter



SWD CONNECTOR

