


Table of Contents	
1	TITLE, TOC & REV
2	NOTES
3	FS4500
4	INTERFACE

		Revisions	
Rev	Description	Date	Approved
A	Original Release	04-OCT-16	Didier Pagnoux

XFRDMFS4503CAEVB

		Analog Sensor Product Group 6501 William Cannon Drive West Austin, TX 78735-6598	
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Designer: Didier Pagnoux		ICAP Classification: CP: IJG: X PUBI:	
Drawing Title: XFRDMFS4503CAEVB		Page Title: TITLE, TOC & REV	
Drawn by: Didier Pagnoux		Size C Document Number SCH:29434 PDF: SPF-29434	
Approved: Didier Pagnoux		Date: Thursday, October 06, 2016	
		Rev A	
		Sheet 1 of 4	

Configuration :

- DFS Enabled
- VDDIO connected to Vcca by default (MCU as an option)
- FS1b option by default
- FS0b on VDDIO
- Vcore regulator set to 1.3V
- Vcca regulator set to 3.3V
- Vcca regulator using Internal PMOS (VCCA_E connected to Vpre)
- Vaux regulator set to 5V
- Vpre regulator configured in Buck or Boost mode

Note: PCB Layout is common to several MC33FSxxxx (U1) part numbers.

For this reason, the schematic gives some variant depending on the MC33FSxxxx installed on the board.



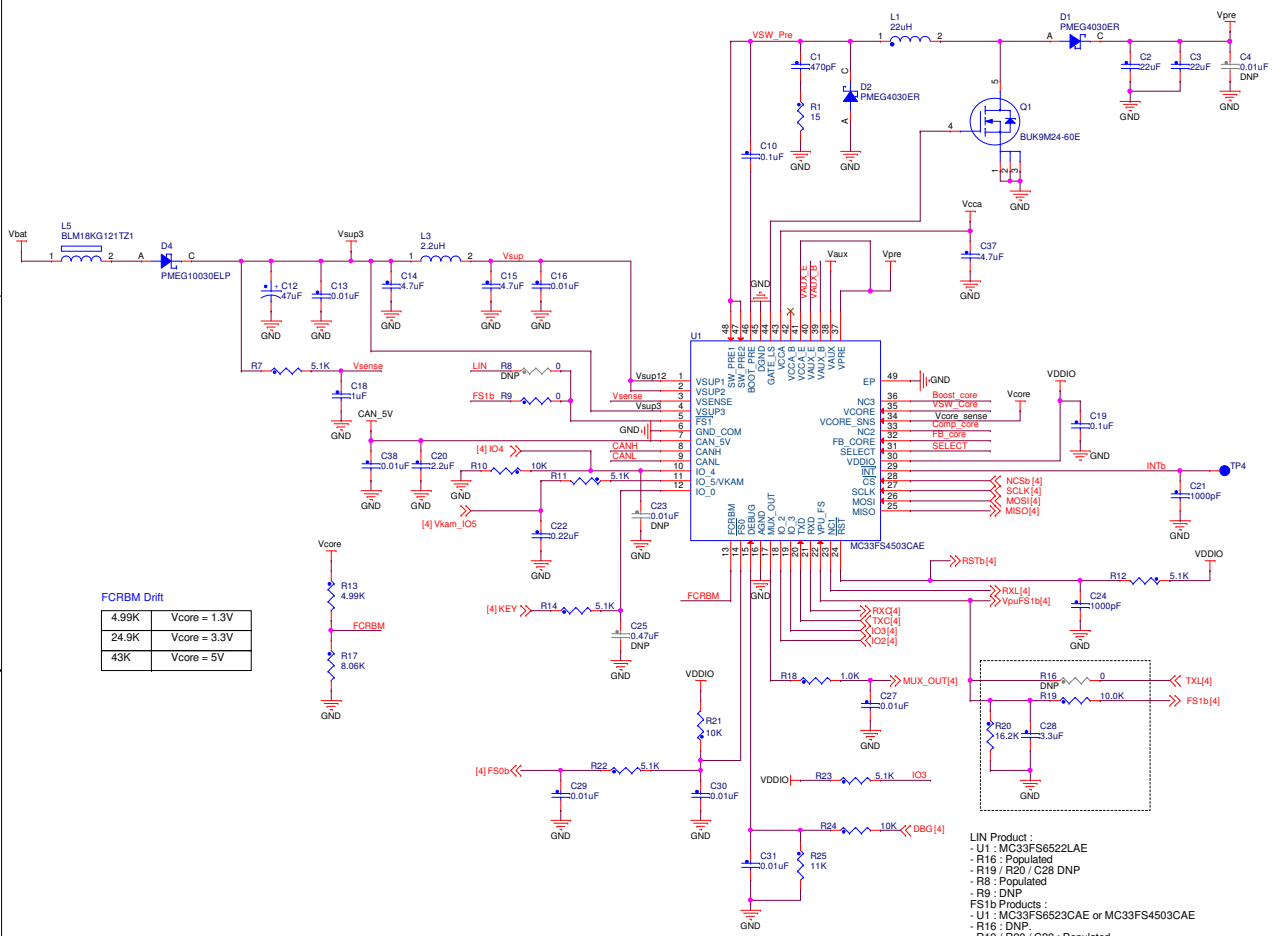
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Drawing Title: **XFRDMFS4503CAEVB**

Page Title: **NOTES**

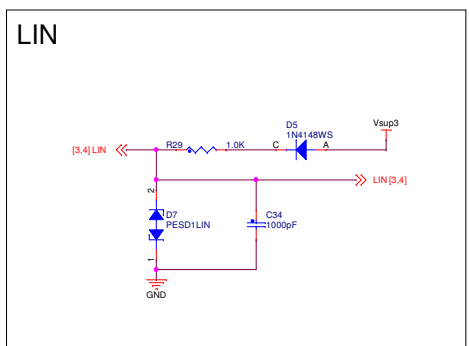
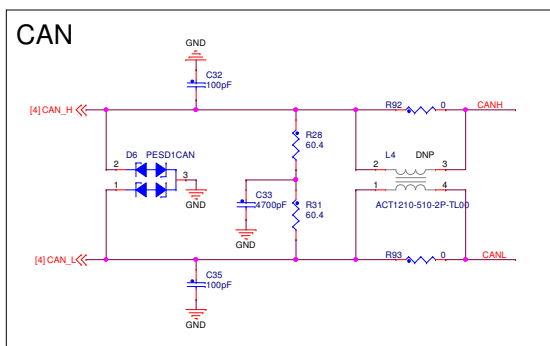
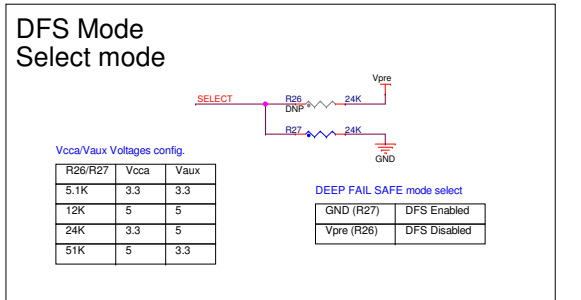
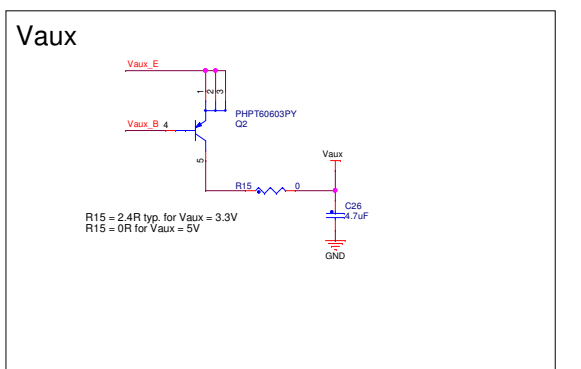
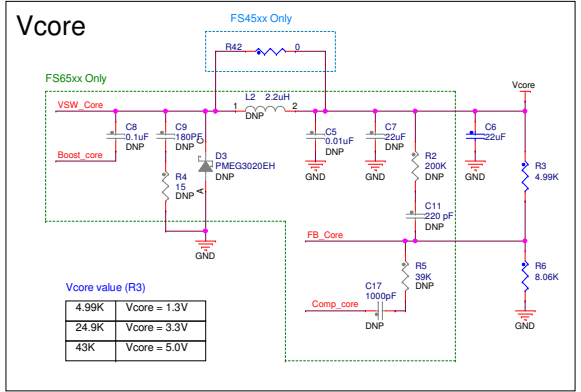
Size C	Document Number SCH-29434 PDF: SPF-29434	Rev A
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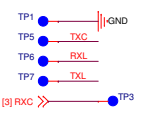
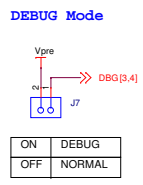
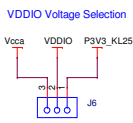
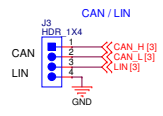
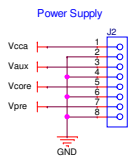
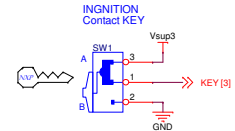
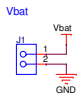
Date: Thursday, October 06, 2016	Sheet 2 of 4
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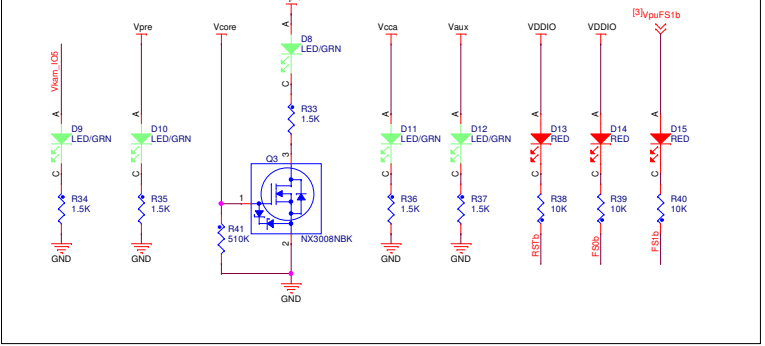
FCRBM Drift

4.99K	Vcore = 1.3V
24.9K	Vcore = 3.3V
43K	Vcore = 5V

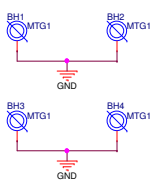
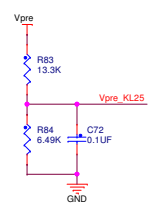
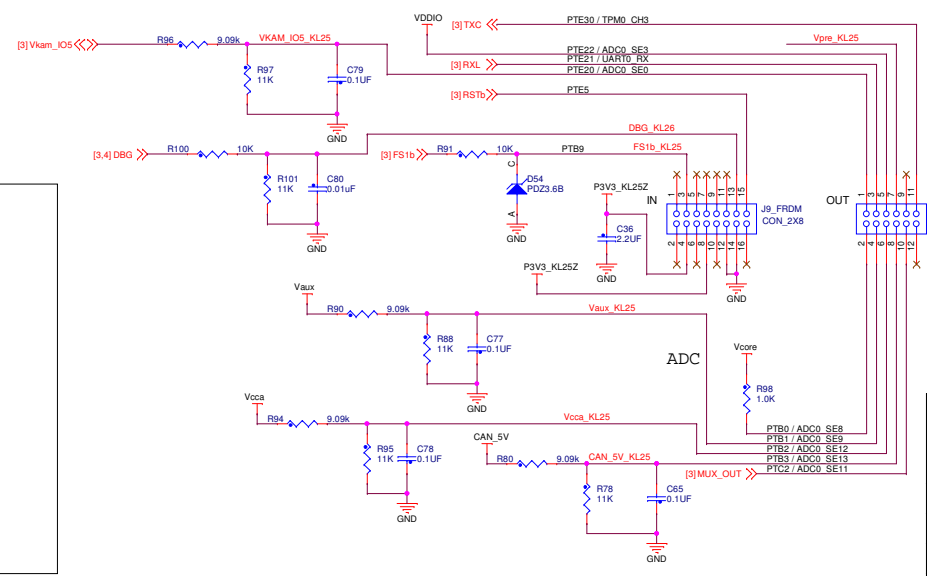
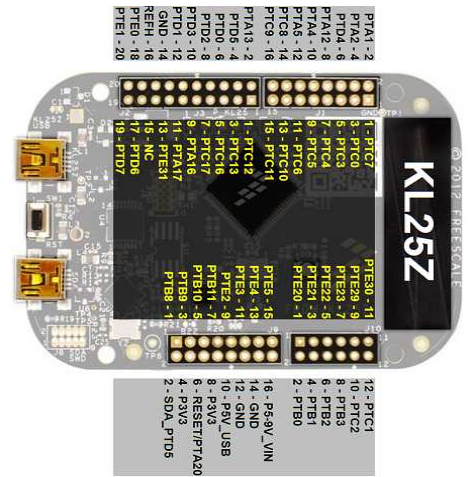
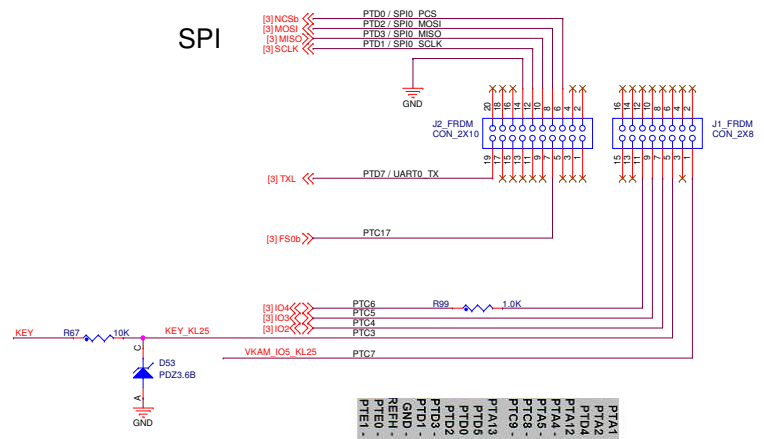





LED Signalling



SPI





ICAP Classification: CP: IUC: X PUB:	
Drawing Title: XFRDMFS4503CAEVB	
Page Title: INTERFACE	
Size C	Document Number SCH-29434 PDF: SPF-29434
Date: Thursday, October 06, 2016	Sheet 4 of 4