JN-RM-2078

JN5189 modules development reference manual

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1.1	20180307	Added picture of the JN5189-001-M16 module
1.2	20180618	Typo corrections
1.3	20190124	Design in checklist tab update DCDC R2 comment. Solder resist area for extra test pin.
1.4	201911216	Updated for mass market release

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

This manual describes the hardware for the reference designs for modules based around the NXP JN5189 wireless microcontroller. The NXP JN5189 modules are small, low-power and cost-effective evaluation and development board or application prototyping and demonstration of the JN5189 device.

The JN5189 is an ultra-low-power, highly integrated single-chip device that enables Standard IEEE 802.15.4 RF connectivity for portable, extremely low-power embedded systems.

The JN5189 SoC integrates a radio transceiver operating in the 2.4 GHz ISM band supporting O-QPSK modulation, an ARM Cortex-M4 processor, up to 640 kB flash,152 kB SRAM and 128 kB ROM, 802.15.4 processor hardware and peripherals optimized to meet the requirements of the target applications.

The design considerations presented in this manual are equally valid for bespoke solutions where the JN5189 device is placed directly onto the product PCB.

Three modules models are available:

- JN5189-001-M10
- JN5189-001-M13
- JN5189-001-M16

The models available are described in Table 1.

In order to complete a successful PCB design by your own the hardware guidelines described in this reference manual must be followed as strictly as possible. Further information on the JN5189 characteristics are available in the “JN5189 IEEE802.15.4 Wireless Microcontroller” datasheet.

The JN5189-001-M10 module has been fitted to a mezzanine board (OM15077) for use on the JN5189 evaluation kits. The module is known as JN5189-001-**T**10.

1.1 Audience

This guide is intended for systems designers

1.2 Regulatory approvals

The JN5189-001-M10 and M13 are compliant with:

- RED 2014/53/EU
- CFR 47 FCC part 15

The high power JN5189-001-M16 is not approved for use in Europe. It is compliant with:

- CFR 47 FCC part 15

2. Reference Design

The reference design package includes the following information for each module variant:

- Reference manual: JN-RM-2078
- Schematics
- Layout
- Bill-of-Materials

Full design databases including schematics and layout source files are available on request.

The following table provides a summary of the JN5189 Module Reference Design that is available from the Wireless Connectivity area of the NXP web site.

Table 1. Modules references

Part number	Description	Content		Reference Manual
JN-RD-6054	JN5189 Module Reference Design Package	OM15069 Standard Power PCB Antenna	JN5189-001-M10	JN-RM-2078
		OM15069 Standard Power μFl connector	JN5189-001-M13	
		OM15072 High Power Antenna diversity (PCB antenna and μFl connector)	JN5189-001-M16	

Note: These reference designs are approved for the operating temperature range of −40 ºC to +125 ºC.

3. Block diagram

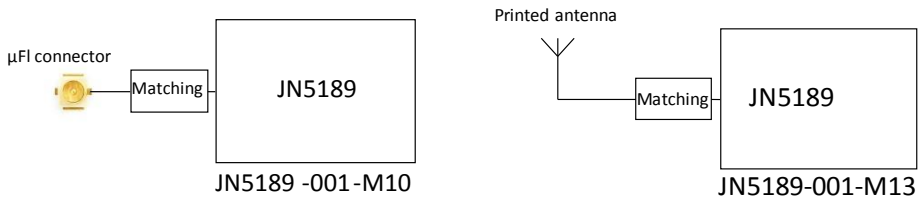


Fig 1. JN5189-001-M10 & M13 block diagrams

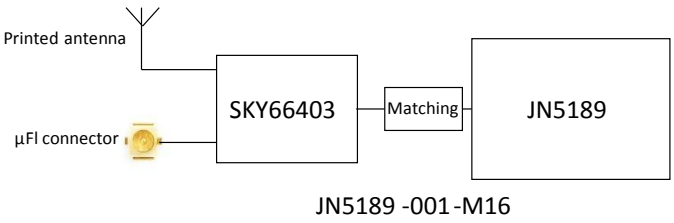


Fig 2. JN5189-001-M16 block diagram

4. Design considerations

To have successful wireless hardware development, the proper device footprint, RF layout, circuit matching, antenna design, and RF measurement capability are essential. RF circuit design, layout, and antenna design are specialties requiring investment in tools and experience. With available hardware reference designs from NXP, RF design considerations, and the guidelines contained in this application note, hardware engineers can successfully design IEEE 802.15.4 radio boards with good performance levels. The following figures show the JN5189 M10 & M13 reference modules. They contain the JN5189 device and all necessary I/O connections.

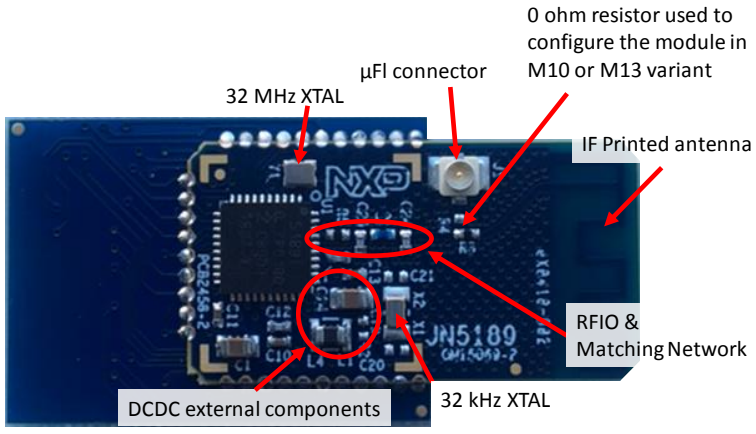


Fig 3. JN5189-001-M10 & M13

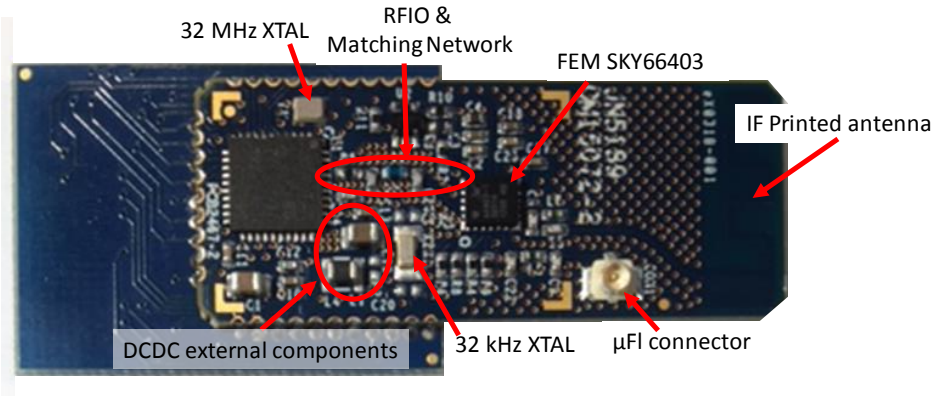


Fig 4. JN5189-001-M16

The device footprint and layout are critical, and the RF performance is affected by the design implementation. For these reasons, use of the NXP recommended RF hardware reference designs are important for successful board performance. Additionally, the reference platforms have been optimized for radio performance. Even small changes in the location of components can mistune the circuit. If the recommended footprint and design are followed exactly in the RF region of the board, sensitivity, output power, harmonic and spurious radiation, and range will have a high likelihood of first time success.

The following subsections describe important considerations when implementing a wireless hardware design starting with the device footprint, PCB stack-up, RF circuit implementation, and antenna selection. The following figure shows an example of a typical layout with the critical RF section which must be copied exactly for optimal radio performance. The less critical layout area can be modified without reducing radio performance.

NOTE

Exact dimensions are not given in this document, but can be found in the manufacturing files for the JN5189 modules

4.1 JN5189 device footprint

The performance of the wireless link is largely influenced by the device's footprint. As a result, a great deal of care has been put into creating a footprint so that receiver sensitivity and output power are optimized to enable board matching and minimal component count. NXP highly recommends copying the die flag exactly as it is shown in the following figure; this includes via locations as well. Deviation from these parameters can cause performance degradation.

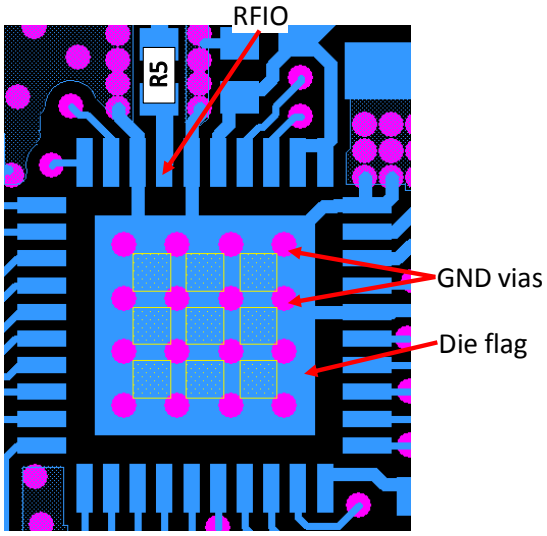


Fig 5. Critical Layout of die flag area

Figure 5 shows the critical areas of the device die flag. These are the following:

- Ground vias and locations
- RF output and ground traces
- Die flag shape

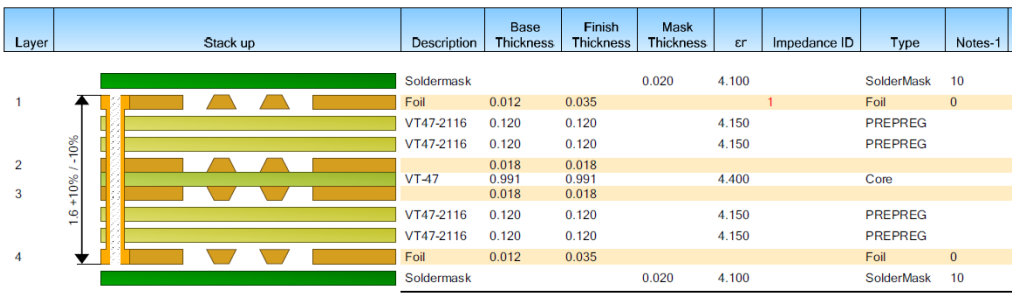
4.2 PCB Stack-Up

Complexity is the main factor that will determine whether the design of an application board can be two-layer, four-layer, or more. From an RF point of view a 4 layers PCB is preferred to a two layers PCB. Nevertheless, in a very simple application it should be possible to use a 2 layers PCB.

The recommended board stack-up for either a four-layer or two-layer board design is as follows:

- 4-layer stack-up:
  - Top: RF routing of transmission lines
  - L2: RF reference ground
  - L3: DC power
  - Bottom: signal routing
- Two-layer stack-up:
  - Top: RF routing of transmission lines, signals, and ground
  - Bottom: RF reference ground, signal routing, and general ground

The JN5789-001-M10 and JN5189-001-M13 (OM15069) and JN5189-001-M16 (OM15062) modules are built on a standard 4–layer printed circuit board (PCB) with the individual layers organized as shown in Figure 6.



Layer	Stack up	Description	Base Thickness	Finish Thickness	Mask Thickness	εr	Impedance ID	Type	Notes-1
		Soldermask			0.020	4.100		SolderMask	10
1		Foil	0.012	0.035			1	Foil	0
		VT47-2116	0.120	0.120		4.150		PREPREG	
		VT47-2116	0.120	0.120		4.150		PREPREG	
2			0.018	0.018					
		VT-47	0.991	0.991		4.400		Core	
3			0.018	0.018					
		VT47-2116	0.120	0.120		4.150		PREPREG	
		VT47-2116	0.120	0.120		4.150		PREPREG	
4		Foil	0.012	0.035				Foil	0
		Soldermask			0.020	4.100		SolderMask	10

Fig 6. PCB stack-up

Note: The NXP PCB layouts assume use of the layers defined above. If a different PCB stack-up is used, then NXP does not guarantee performance.

NXP strongly recommends the use of the above stack-up.

As shown in Figure 6, regarding transmission lines, it is important to copy not just the physical layout of the circuit, but also the PCB stack-up. Any small change in the thickness of the dielectric substrate under the transmission line will have a significant change in impedance; all this information can be found on the fabrication notes for each board design. As an illustration, consider a 50-ohm microstrip trace that is 18 mils

wide over 10 mils of FR4. If that thickness of FR4 is changed from 10 to 6 mils, the impedance will only be about 36 ohms.

In any case the width of the RF lines must be re-calculated according to the PCB characteristics in order to ensure a 50-ohm characteristic impedance.

When the top layer dielectric becomes too thin, the layers will not act as a true transmission line, even though all the dimensions are correct. There is not universal industry agreement on which thickness at which this occurs, but NXP prefers to use a top layer dielectric thickness of no less than 8-10 mils.

There is also a limit to the ability of PCB fabricators to control the minimum width of a PCB trace and the minimum thickness of a dielectric layer. +/- 1 mil will have less impact on an 18 mils wide trace and a 10 mil thick dielectric layer, than it will on a much narrower trace and thinner top layer.

This can be an especially insidious problem. The design will appear to be optimized with the limited quantity of prototype and initial production boards, in which the bare PCB's were all fabricated in the same lot. However, when the product goes into mass production there can be variations in PCB fabrication from lot-to-lot which can degrade performance.

The use of a correct substrate like the FR4 with a dielectric constant of 4.4 will assist you in achieving a good RF design.

While no special measures are required for the board design, it is recommended that Class 1 tolerances be used.

4.3 RF circuit topology and matching

NXP always recommends that designers start by copying the existing NXP reference design. This applies to both the circuit portion (schematic) of the design, and the PCB layout. For all RF designs, particularly for designs at frequencies as high as 2.4 GHz, the PCB traces are a part of the design itself. Even a very short trace has a small amount of parasitic impedance (usually inductive), which has to be compensated for in the remainder of the circuit.

What may seem like a minor change to the layout, or what would certainly be a minor change at a lower frequency of operation, can actually be a significant change at 2.4 GHz. For example, we may consider that a metal trace on a PCB such as the JN5189-001M1x modules is approximately 0.8 nH per mm. At lower frequencies, this would have no impact, but at 2.4 GHz this would have a significant impact in any matching circuits.

The circuits used on the NXP reference designs are all tuned and optimized on the actual layout of the reference design, such that the final component values take into account the effects of the circuit board traces, and other parasitic effects introduced by the PCB. This includes such issues as parasitic capacitance between components, traces, and/or board copper layers, inductance of traces and ground vias, the non-ideal effects of components, and nearby physical objects.

The layout of the RF portions of JN5189 based modules is critical. It is important that the reference designs are strictly adhered to, otherwise the following may occur:

- Reduction in RF output
- Excessive spurious RF outputs leading to RF compliance issues
- Unacceptable power slope across the full channel range
- Poor range
- Reduced Rx sensitivity

4.4 Transmission lines

Transmission lines have several shapes such as microstrip, coplanar waveguide, and strip-line. For 802.15.4 applications built on FR4 substrates, the types of transmission lines typically take the form of microstrip or coplanar waveguide (CPW). These two structures are defined by the dielectric constant of the board material, trace width, and the board thickness between the trace and the ground.

Additionally, for CPW, the transmission line is defined by the gap between the trace and the top edge ground plane. These parameters are used to define the characteristic impedance of the transmission line (trace) that is used to convey the RF energy between the radio and the antenna.

JN5189 has a single ended RF output with 3 component matching network composed of a shunt capacitor, a series inductor then another shunt capacitor. In addition, a 0 ohm resistor has been placed between the RFIO port of the chip and the first shunt capacitor. These elements transform the device impedance to 50 ohms. The value of these components may vary depending on your specific board layout. The recommended RF matching network is shown in Figure 7.

Avoid routing traces near or parallel to RF transmission lines or crystal signals. Maintaining a continuous ground under an RF trace is critical to maintaining the characteristic impedance of that trace. Avoid any routing on the ground layer that will result in disrupting the ground under the RF traces.

Keep the RF trace as short as possible.

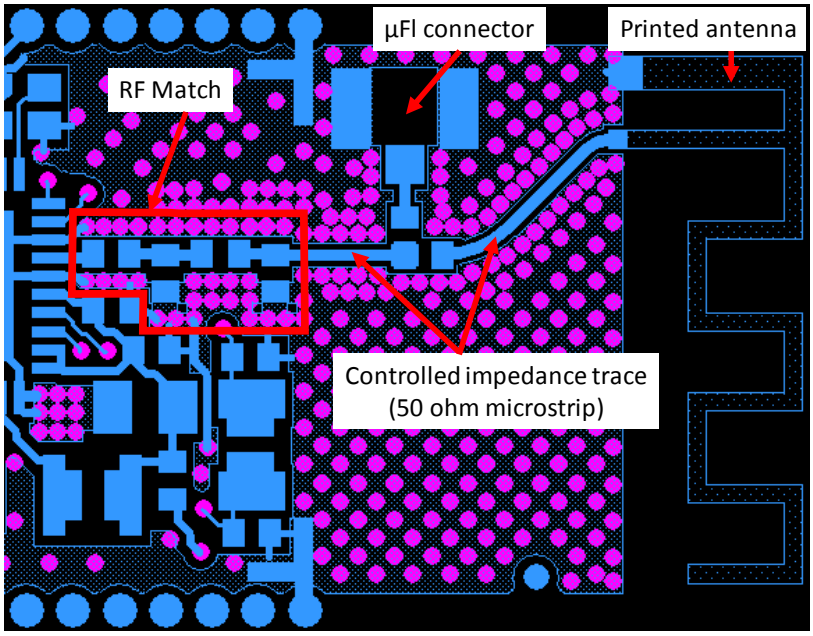


Fig 7. RF Matching Network

4.5 Components

All electronic components have parasitic characteristics that cause the part to act in a non-ideal way. Typically, these effects become worse as the frequency of operation is increased.

For most component suppliers, this quality is expressed by the Self Resonant Frequency (SRF) specification. For example, a capacitor has parasitic inductance introduced by the metal leads of the components. As frequency increases, at some point the impedance due to the parasitic inductance is greater than the impedance of the capacitor, and at that frequency and higher, the component no longer acts as a capacitor and now acts as an inductor. At the point at which the impedance from both inductive and capacitive components is the same, the part will resonate as a LC parallel resonant circuit, and this is called the Self Resonant frequency. Figure 8 shows some typical response curve.

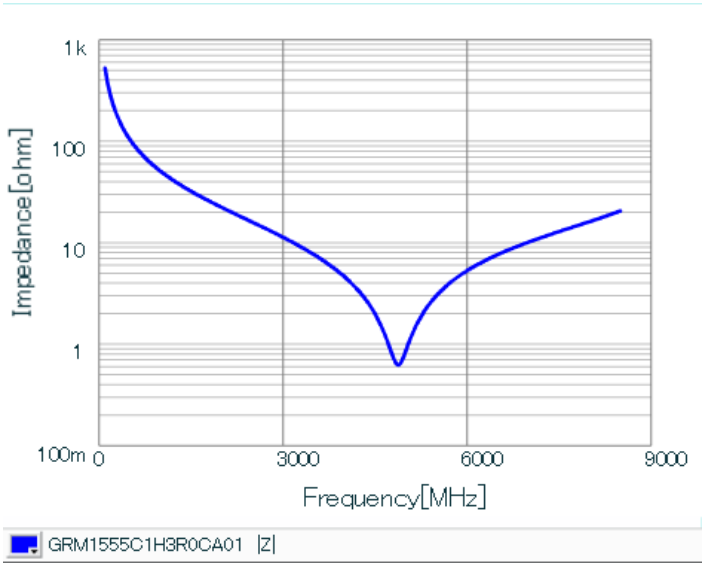


Fig 8. RF Plots for 3pF ceramic capacitor Murata GRM1555 type

The same is true of inductors. There is parasitic capacitance in an inductor, mainly due to capacitive coupling between the turns of wire. At some point in frequency, this capacitance will have a higher impedance than the inductance of the part. From this frequency and higher the part acts as a capacitor and not as an inductor.

The Bill of Materials (BOM) is available for all NXP reference designs. The BOM shows the specific vendors and part numbers used on NXP designs. It is certainly possible to substitute another vendor's parts, but it may impact the performance of the circuit, therefore, it may be necessary to use different component values when parts from another vendor are used.

If there is a performance issue on a new design, and part substitutions were made on that design, then it is strongly recommended that components identical to those used in the NXP reference design be placed on the new design for test purposes. Once the design is working properly with components that are identical to those used by NXP, then it will be possible to substitute components from other vendors one at a time, and test for any impact on circuit performance.

4.6 GND planes

It is recommended to use a solid (continuous) ground plane on Layer 2, assuming Layer 1 (top) is used for the RF components and transmission lines; avoid cut-outs or slots in that area.

Keep top ground continuous as possible. This also applies for the other layers.

Connect ground on the components layer to the ground plane beneath with a large quantity of vias.

Ground pours or fingers can act as antennas that unintentionally radiate. To avoid this, eliminate any finger that is not connected to the ground reference with a via; put a via in any trace that doesn't go anywhere.

4.7 Layers interconnections

Avoid vias in the RF traces.Typically for a 1.6mm thickness PCB material, a single via can add 1.2nH of inductance and 0.5pF of capacitance, depending upon the via dimensions and PCB dielectric material.

Provide multiple vias for high current and/or low impedance traces.

Connect carefully all the ground areas of any layer to the reference GND plane

4.8 DCDC components

Be sure that the smallest values capacitors C12 and C10 are placed close to the VBAT pin.

The impedance of the GND connection between C10/C12 and C19 must be as low as possible: connect them directly on the component layer (see the red path below)

The R2 footprint on DCDC reference design can be removed if there is constraint on the layout space as long as the DCDC is sued as depicted in the current JN5189 DS.

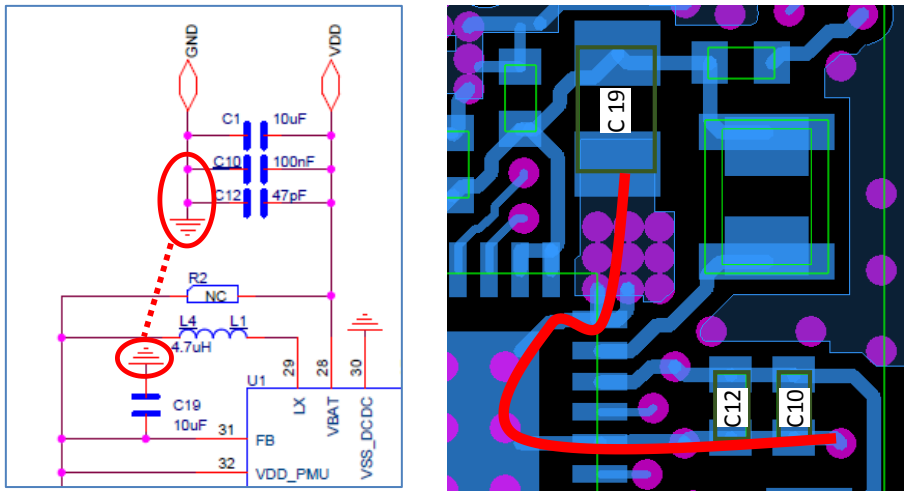


Fig 9. GND path between C10/C12 and C19

4.9 Reference Oscillator

The NXP JN5189 device contains the necessary on-chip components to build a 32-MHz reference oscillator with the addition of an external crystal resonator. There is no need to use external capacitors because the JN5189 includes a bank of switchable capacitors that can be tuned to adjust the load capacitance (C_L) that needs to be seen by the XTAL.

The reference crystal serves many purposes, including the provision of a reference for the 32-bit ARM processor, PHY controller, radio synthesizer and analogue peripherals. In addition, the crystal provides timing references for external I/O (e.g. on-chip UARTs) and timer counters. Thus, it is important that the crystal reference is specified and built correctly to ensure that the system functions properly.

The choice of crystal resonator is important for the following reasons:

Resonator tolerance: A number of parameters, ranging from on-chip timings to radio centre-frequency, are derived directly from the tolerance of the crystal. As indicated in the component list, we recommend that a total tolerance of less than ±25 ppm is used, as the maximum permissible offset specified in IEEE802.15.4 is ±40 ppm. Also, note that this tolerance should include both temperature and ageing effects imparted on the resonator.

Resonator load capacitance: The active oscillator components on the JN5189 devices are designed for a crystal resonator with load capacitance (C_L) of 6 pF. This is a standard load and resonators of this type are widely available.

Lay-out recommendations:

Route the connections from the 32 MHz XTAL to the chip oscillator pins with traces as short as possible. The layout of the oscillator circuit is such that tracks between components are as short as possible. This improves the performance of the oscillator by reducing stray capacitance which can introduce frequency errors.

The XTAL should be placed away from high frequency devices and traces in order to reduce the capacitive coupling between XTAL pins and PCB traces.

Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from the crystal connections as possible.

Caution: Adherence to NXP's recommendations will ensure that the module performs correctly. The substitution of components is not recommended, as this may lead to both oscillator start-up and frequency tolerance issues.

4.10 Decoupling

4.10.1 General considerations

Decouple the power supplies or regulated voltages as close as possible to the supply pin of the IC. The decoupling capacitors must be connected to a localized ground pad on the top layer that is connected to the main ground plane layer through multiple vias.

Ensure that each decoupling capacitor has its own via connection to ground. When possible use 2 vias to connect the capacitor to the ground layer.

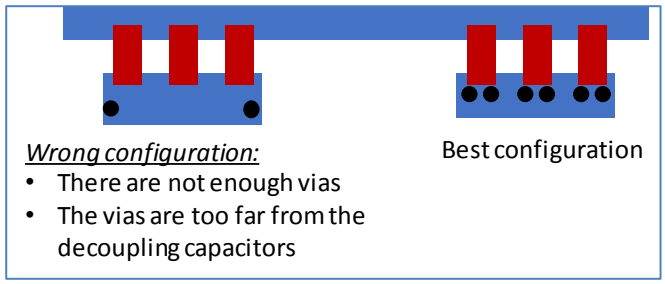


Fig 10. GND vias placement

The capacitor with a smaller capacitance must be placed nearer to the IC.

The decoupling capacitor must be placed between the main supply line and the supply pin as shown below:

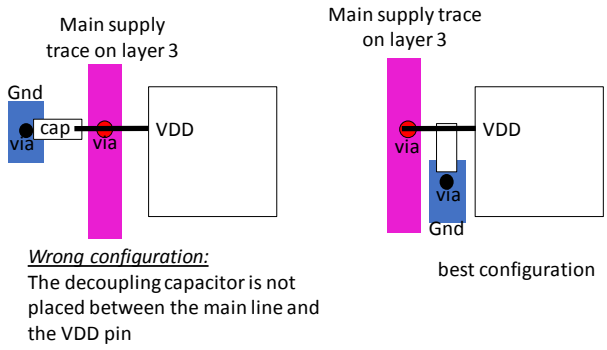


Fig 11. Decoupling capacitors placement

4.10.2 VDD(RADIO), FB, VDD_PMU, VDDE and VBAT decoupling

Copy as much as possible the placement of the decoupling capacitors of all the supply pins as shown below.

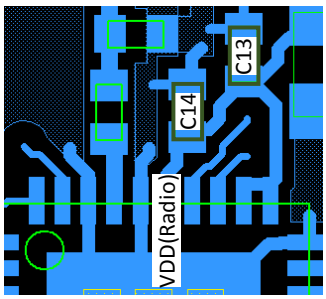


Fig 12. VDD(Radio) decoupling

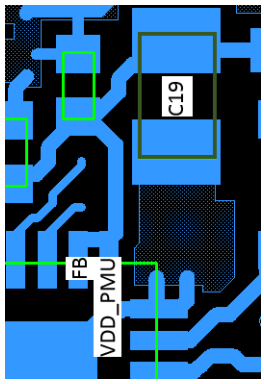


Fig 13. FB and VDD_PMU decoupling

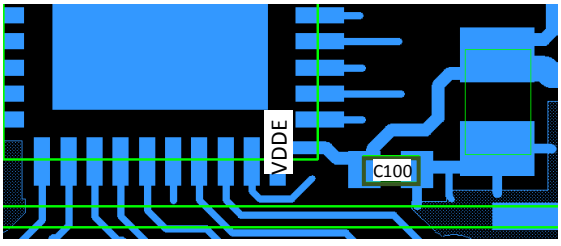


Fig 14. VDDE decoupling

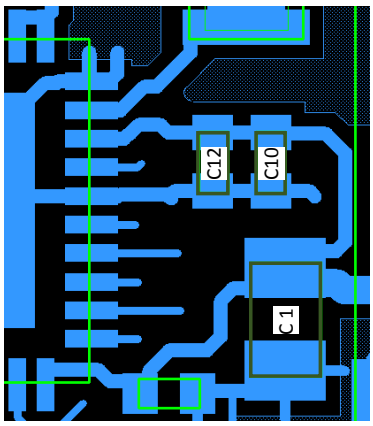


Fig 15. VBAT decoupling

4.11 Traces Isolation

When PCB traces are in close proximity, they can talk to each other through the capacitor created by these traces.
In order to minimize the effect of this parasitic coupling, identify the most sensitive traces or areas (RF trace, oscillator, power lines, ...) and separate them from any signal that is likely to couple with them through parasitics.
Separation between 2 lines can be achieved by increasing the distance from one to the other.

4.12 GPIOs

The GPIOs traces are generally long lines that can cover long distances. They can carry undesirable signals that are likely to radiate in any direction. It is recommended to avoid routing these signals

4.13 Screening can

The JN5189 doesn't radiate high spurs and it is very robust to EMC interferers so there is in principle no need for a screening can (or shielding can). Nevertheless, a footprint for a can has been added on the NXP modules and NXP recommends adding this footprint to any PCB. In very specific cases under a very noisy environment it could be helpful to add a can.

5. Optimal PCB placement of a module

In case the JN5189 is mounted on a module similar to the NXP JN5189-001-M10 care must be taken when mounting this module onto another PCB.

The area around the antenna must be kept clear of conductors or other metal objects for an absolute minimum of 20 mm. This is true for all layers of the PCB and not just the top layer. Any conductive objects close to the antenna could severely disrupt the antenna pattern resulting in deep nulls and high directivity in some directions.

The diagrams below show various possible scenarios. The top 3 scenarios are correct; groundplane may be placed beneath JN5168-001-M00 module as long as it does not protrude beyond the edge of the top layer ground plane on the module PCB.

The bottom 3 scenarios are incorrect; the left-hand side example because there is groundplane underneath the antenna, the middle example because there is insufficient clearance around the antenna (it is best to have no conductors anywhere near the antenna), finally the right-hand example has a battery's metal casing in the recommended keep out area.

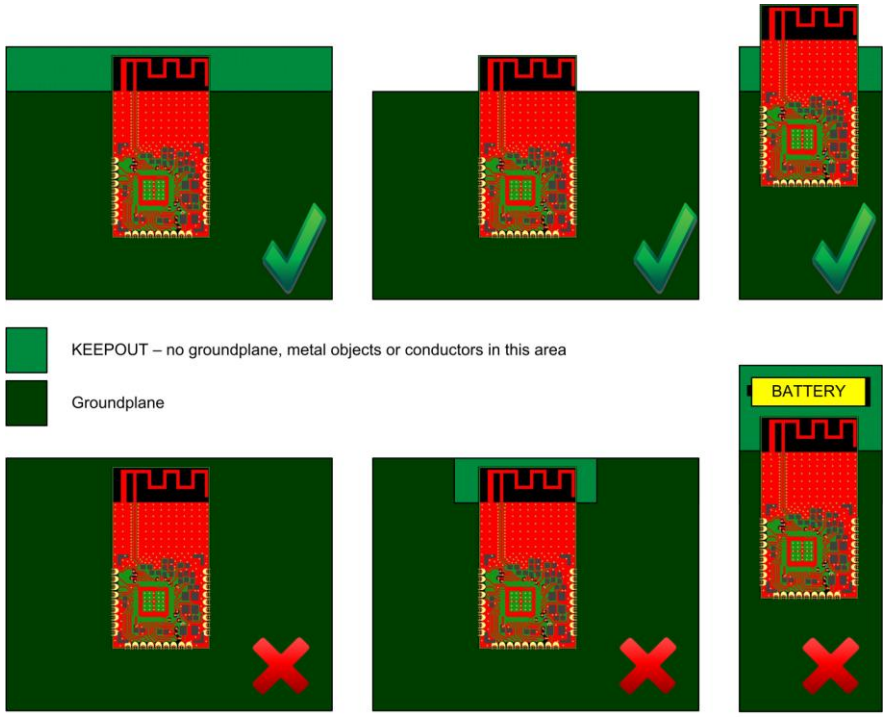


Fig 16. PCB placement of a JN5189 module with a printed antenna

6. Manufacturing considerations

The HVQFN package must be considered carefully when using reflow solder techniques.

Package footprint information can be found in the JN5189 data sheet.

The decal is shown in Fig 17. The pad stacks used are 0.25 mm by 1 mm for the smaller pads, and a 6.4 mm square pad for the paddle.

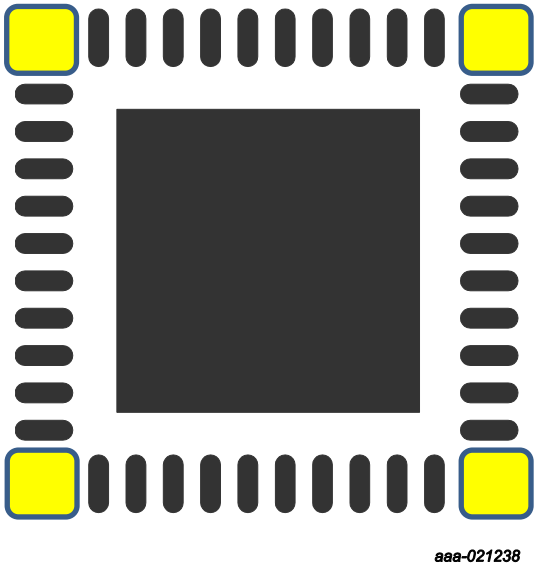


Fig 17. Recommended PCB decal for HVQFN40 40-pin QFN

The solder mask used is shown in Fig 19. The pad stacks used are 0.25 mm by 1 mm for the smaller pads, and four 1.6 mm square pads to apply paste to the paddle. The solder paste mask has a thickness of 6-thou (0.152 mm). If the paste thickness needs to deviate from that used NXP then it may be necessary to change the number of pads that the paste is applied to. Paste thickness may be dictated by additional components used in a design.

NOTE – Solder resist area:

A specific connection used on NXP production line has to be handled carefully when the layout is done (see nest figure)

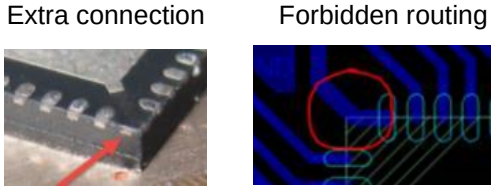


Fig 18. Extra test pin

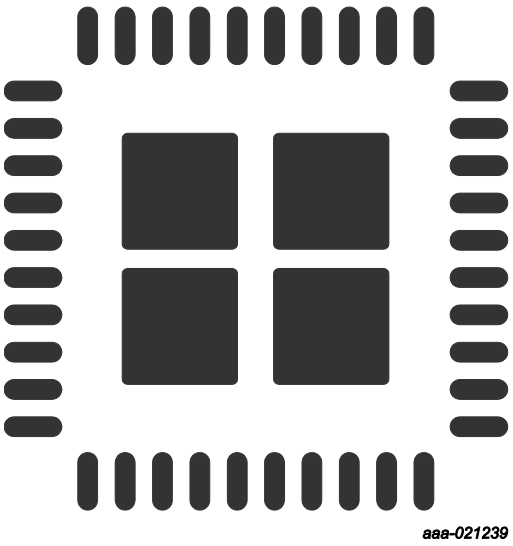


Fig 19. Solder paste mask for HVQFN40 40-pin QFN

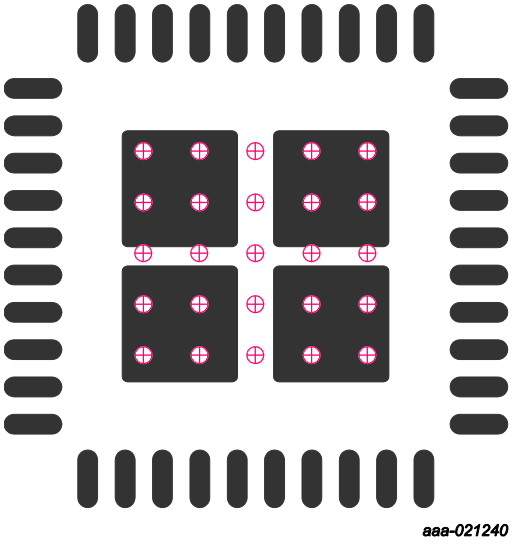


Fig 20. Vias on the paddle of the HVQFN40 40-pin QFN

25 vias are applied to the paddle. These allow excess solder paste and heated air to be vented away from the device, preventing the device from being lifted during soldering. In addition, these vias ensure that a low impedance ground is maintained, which is vital for optimum RF performance.

7. Regulations

The following information is provided per Article 10.8 of the Radio Equipment Directive 2014/53/EU:

(a) Frequency bands in which the equipment operates.

(b) The maximum RF power transmitted.

PN	RF Technology	(a) Freq Ranges (EU)	(b) Max Transmitted Power
JN5189-001-T10	IEEE 802.15.4	2400 - 2483 MHz	11 dBm

EUROPEAN DECLARATION OF CONFORMITY
(Simplified DoC per Article 10.9 of the Radio Equipment Directive 2014/53/EU)

This apparatus, namely JN5189-001-T10 module, conforms to the Radio Equipment Directive 2014/53/EU.
The full EU Declaration of Conformity for this apparatus can be found at this location:
www.nxp.com/JN5189-001-T10

8. Check list schematic

Table 2. Schematic design-in check list

Check number	SCHEMATICS DESIGN-IN REVIEW CHECK-LIST	Y/N/NA	Customer comments and/or actions	Check done by	NXP Feedback
1	**GENERAL**				
1.1	Have the schematics been checked versus NXP reference schematics & Application Notes?				
1.2	Have the schematics been reviewed by several people?				
1.3	Does the application use non-standard components? (e.g. components that had not previously used for such applications)				
1.4	Have the non-standard components been qualified so that they can be used in the application?				
1.5	Are recommendations for layout/form factor written on the schematics?				
1.6	Are the components sized for the wanted current drive capability?				
1.7	Has the JN5189 symbol pinning been checked and does it include the exposed pad?				
2	**RF IO**				
2.1	Is the characteristic impedance of the RF_IO input/output line 50 ohm over the full RF range?				
2.2	Have components with the correct type and value been connected to the RF port of the JN5189?				
2.3	For modules with external FEM is extra filtering needed for harmonics rejection?				
3	**32 MHz crystal reference Oscillator**				
3.1	Is the oscillator external configuration in accordance with the Application Note?				
3.2	Has XTAL model been recommended by NXP?				

3.3	In case the XTAL model has not been recommended by NXP have all the parameters been checked in order they fulfill NXP, standard and application requirements (load capacitance,pulling sensitivity, equivalent resistance, frequency tolerance, temperature range, frequency drift versus temperature, ageing) ?				
4	**32 kHz crystal Oscillator**				
4.1	Has the need of a 32 kHz XTAL been discussed? (Zigbee specifications can be met without an external XTAL)				
4.2	In case the 32 kHz XTAL oscillator has been implemented has the XTAL model been recommended by NXP ?				
4.3	In case the XTAL model has not been recommended by NXP have all the parameters been checked in order they fulfill NXP, standard and application requirements (load capacitance,pulling sensitivity, equivalent resistance, frequency tolerance, temperature range, frequency drift versus temperature, ageing) ?				
5	**Power Supply**				
5.1	Have all the VDD pins been connected according to NXP recommendations?				
5.2	Are the power supply regulators/battery well sized?				
5.3	Has the decoupling of the supply regulators/battery output been implemented?				
5.4	Have the power supply pins of the IC been properly decoupled (according to the Application Note and Reference Design schematics?)				
5.5	Have the recommendations for the values and models of the components of the DCDC converter been taken into account?				
5.6	Has the exposed die pad been connected to GND?				
6	**PIOs**				
6.1	Has the compatibility of the logic levels with other components been checked?				
6.2	Does the max source/sink current fit the application?				
7	**ADC**				
7.1	Does the ADC characteristics fit the application?				

8	**Programming and Debug**				
8.1	Has the flash programming connector been connected to the correct I/O on the microcontroler?				
8.2	Has a connector for debug been added that allows the microcontroler to be put into programming mode? (RSTN & PIO5/ISP pins)				
8.3	Is the reset pin RSTN properly connected?				
8.4	Add a test point at an unused DIO in order a trigger signal can be output from the pin for sensitivity measurements				
8.5	For printed and chip antenna: Is the RF line implemented in such a way that the HW can be easily modified in order to do conducted measurements on one hand and measure the antenna characteristics on the other hand ? For instance a 0 ohm resistor can be used to connect the JN5189 RF port to the antenna for the real application and a SMA or µFL connector footprint can be added for debug; the SMA or µFl connector will be connected/disconnected to/from the JN5189 RF port or the antenna with 0 ohm resistors.				
8.6	If I2C used, are the I2C lines pulled up?				
9	**External Memory**				
9.1	In case an external flash memory is used has the correct type of memory been used and is it connected to the microcontroller correctly?				
9.2	Has the flash memory symbol pinning been checked?				

9. Check list layout

Table 3. Layout design-in check list

Check number	LAYOUT DESIGN-IN REVIEW CHECK-LIST	Y/N/NA	Customer comments and/or actions	Check done by	NXP feedback
1	**GENERAL**				
1.1	Has the number of layers been clearly discussed?				
1.2	Has the layout been checked versus NXP reference board ? (i.e OM15069-2_JN5189_ANTENNA_MODULE)				
1.3	Have the HW recommendations of the JN-RM-2078 reference manual been followed?				
1.4	Has the correct PCB material been specified?				
1.5	Have the correct PCB thicknesses been specified?				
2	**RF IO**				
2.1	Is the RF_IO input/output line well sized for 50 ohm? The line width must be calculated according to the board thickness and PCB material.				
2.2	Are the RF wires as short as possible (wires behave as antenna so shortening them help to increase EMI immunity)				
2.3	Have vias been avoided in the RF line?				
2.4	Has the placement of the RFIO matching network been strictly copied from the NXP reference module?				
3	**Crystal reference Oscillator**				
3.1	Has the 32 MHz XTAL been placed close to the IC?				
3.2	Are there GND vias around the 32 MHz XTAL ?				
4	**Power Supply**				
4.1	Have all the VDD capacitors been placed as close as possible to the power pins and voltage regulators outputs?				
4.2	Provide multiple vias in the power lines when power is routed on several layers				

4.3	For low supply voltage application – close to 2.0V, please ensure that the supply track is well dimensioned so as to avoid IR drop and hence falsely trigger the brown-out. (IR drop is the voltage drop due to the supply current flowing into the supply track resistance).				
4.4	Have the VDD lines been isolated from potential interferences?				
4.5	Is GND plane continuous around and near all signals?				
4.6	Has the die pad been properly connected to GND?				
4.7	Are vias implemented in the die pad?				
5	**EMC and Misc**				
5.1	In case more than 2 layers are used, does one layer act as a continuous ground plane (GND reference plane)?				
5.2	Are numerous vias added near capacitor, near fingers,…?				
5.3	Remove small GND areas and isolated fingers that cannot be connected to the reference GND plane with a via.				
5.4	Have silk screens been added with relevant information? (components ref, logo, board name…)				
5.5	Are all silkscreen texts readable when the board is populated?				
5.6	Have traces been avoided below noisy or sensitive components?				
5.7	Check that traces do not cut across power or ground planes unnecessarily.				
5.8	Is the JN5189 footprint strictly similar to the NXP reference?				
5.9	If more than 2 layers are used, the inner layers must be left empty below the RF components and the antenna				
5.10	Each connection between a component and GND must be doubled with a via to the GND plane.				
5.11	Have the soldering/non soldering areas been respected? Is solder resist layer check in the empty area?				
5.12	If sold unit is a module is a CAN/shield implemented?				

10. Abbreviations

Table 4. Abbreviations

Acronym	Description
EMC	Electro Magnetic Compatibility
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
PAN	Personal Area Network
PCB	Printed Circuit Board
RF	Radio Frequency
SPI-bus	Serial Peripheral Interface-bus
TQFN	Thin Quad Flat No-lead
WPAN	Wireless Personal Area Network

11. References

JN5189 Datasheet – IEEE802.15.4 Wireless Microcontroller

12. List of figures

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