Fact Sheet



S32N55

# S32N55 Vehicle Super–Integration Processor

The S32N55 vehicle super-integration processor accelerates the development of centralized software-defined vehicle (SDV) architectures. The S32N55 processor is ideal for a central vehicle controller that consolidates many electronic control units (ECUs) by safely integrating cross-vehicle real-time functions. The S32N55 processor helps simplify the complexity and improves the time-to-market for SDV real-time ECU consolidation without compromising security or safety.

As the industry's first 5nm safe automotive processor, the S32N55 combines highperformance real-time processing with on-chip hardware isolation and virtualization, advanced functional safety and fault recovery, robust hardware security engine, network acceleration and flexible memory expansion support. The S32N55 processor is developed in accordance with ISO/SAE 21434 and UN R155 processes for cybersecurity and ISO 26262 for functional safety up to ASIL D.

# **Target Applications**

- Centralized real-time vehicle control for SDVs
- Domain and cross-domain real-time function
  integration
- Safety processing
- Factory automation / industrial controllers



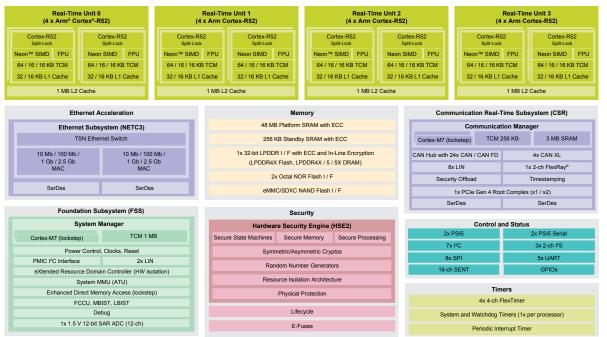




## Enablement

- Hardware evaluation boards
- S32N Vehicle Integration Platform reference software
- AUTOSAR® Classic Platform, Zephyr® Project and FreeRTOS™ real-time operating systems
- Real-Time Drivers (RTD) with AUTOSAR MCAL support
- Inter-Platform Communication Framework (IPCF)
- Type-1 hypervisor (EL2 monitor)
- S32 Design Studio IDE
  - GCC compiler, configuration tools (IVT, DCD, DDR, AUTOSAR), trace and debugger components, flash programmer
- Firmware for hardware accelerators (HSE2, Communication Real-Time Subsystem, System Manager)
- S32 Safety Software Framework (SAF) and Structural Core Self-Test (SCST)
- Automotive Math and Motor Control Library (AMMCLib)
- NXP eIQ<sup>®</sup> Auto ML Software Development Environment
- Virtual support for early software development and regression testing

## **Block Diagram**



## **Features and Benefits**

Key Features	Benefit(s)
16x Arm® Cortex®-R52 real-time processors operating up to 1.2 GHz	High-performance real-time processing with flexible split/lockstep support for integration of vehicle functions with mixed-criticality
Full on-chip hardware core-to-pin isolation and virtualization	Provides freedom from interference for multiple integrated ECUs. Keeps fault impact at ECU level with separate runtime control for each ECU.
Quality-of-Service mechanisms for shared resources	Ensures access and bandwidth for each integrated ECU
Safe System Manager implemented with dual-core lockstep Arm Cortex-M7 cores	Provides functional safety management for the device.
Large amount of on-chip SRAM with diverse memory interfaces	SRAM supports fast execution for multiple real-time applications. Flexible external memory interfaces (NOR flash, NAND flash, SDIO, LPDDR4x Flash and LPDDR4x/5 DRAM) allow for future memory expansion and OTA update support with execute in place (XiP) options.
Integrated hardware security engine (HSE2) for root of trust (RoT)	Supports secure boot, security services and key management
Distributed security approach with engines physically located near modules/peripheral	Provides increased availability of security services, increased parallelism of security operations, clearer prioritization between tasks, and minimized latency
Public key infrastructure and support of Post-Quantum Cryptography (PQC) algorithms	Support for secure boot and Over-the-Air (OTA) upgradability to help future-proof designs for emerging security requirements
CAN Hub with CAN I/O virtualization to share CAN I/O pins	CAN frames can be routed to multiple integrated ECUs. Provides efficient filtering and routing between ECUs. CAN handling is offloaded from the host core.
Integrated Time-Sensitive Networking (TSN) Gigabit Ethernet switch (NETC3) with dual Ethernet MACs each operating up to 2.5 Gbps	Removes external Ethernet switch for system BoM cost reduction

## SafeAssure Functional Safety Program

### Functional safety. Simplified.

The S32N55 processor is part of NXP's SafeAssure functional safety program, which is designed to help system manufacturers more easily achieve system compliance with International Standards Organization ISO 26262 functional safety standards. The program highlights our hardware and software solutions that are optimally designed to support functional safety implementations and come with a rich set of enablement collateral. For more information, visit <u>www.nxp.com/SafeAssure</u>.

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