

# LPC553x

Errata sheet LPC553x

Rev. 1.5 — May 24, 2023

Errata sheet

## Document information

Info	Content
Keywords	LPC5536, LPC5534
Abstract	LPC553x errata



**Revision history**

Rev	Date	Description
1.5	20230524	<ul style="list-style-type: none"><li>Added <a href="#">Section 3.5 “PLL.1: PLL LOCK bit is not reliable”</a>.</li></ul>
1.4	20230223	<ul style="list-style-type: none"><li>Updated revision identifiers in <a href="#">Section 1 “Product identification”</a>, and <a href="#">Section 2 “Errata overview”</a>.</li></ul>
1.3	20220711	<ul style="list-style-type: none"><li>Added I3C.2 <a href="#">Section 3.4 “I3C.2: More than one In Band Interrupt (IBI) extended data bytes (EXTDATA) emitted by I3C slave are not abortable by the I3C bus master.”</a>.</li><li>I3C is renamed as I3C.1.</li><li>Updated revision identifier from A to 0A throughout the document.</li></ul>
1.2	20220323	<ul style="list-style-type: none"><li>Added CRP.1 <a href="#">Section 3.3 “CRP.1: Boot ROM does not give correct Code Read Protection (CRP) status when in CRP_LEVEL3”</a></li></ul>
1.1	20220117	<ul style="list-style-type: none"><li>Added ADC.1 <a href="#">Section 3.1 “ADC.1: Missing code in Standard resolution mode”</a></li><li>Added I3C.1 <a href="#">Section 3.2 “I3C.1: Data lost when using the DMA to write transmit data to I3C, and the data size is greater than the I3C FIFO size”</a>.</li></ul>
1.0	20210916	Initial release.

**Contact information**

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## 1. Product identification

The LPC553x HLQFP100 package has the following top-side marking:

- First line: LPC553x
- Second line: xxxxxxx
- Third line: **zzzyywwxR**
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 0A, 1B

The LPC553x HTQFP64 package has the following top-side marking:

- First line: LPC553x
- Second line: JBD64
- Third line: xxxx
- Fourth line: xxxx
- Fifth line: **zzzyywwxR**
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 0A, 1B

The LPC553x HVQFN48 package has the following top-side marking:

- First line: LPC553x
- Second line: JHI48
- Third line: xxxxxxxx
- Fourth line: xxxx
- Fifth line: **zzzyywwxR**
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 0A, 1B

## 2. Errata overview

**Table 1. Functional problems table**

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	Missing code in Standard resolution mode.	0A	<a href="#">Section 3.1</a>
I3C.1	Data lost when using the DMA to write transmit data to I3C, and the data size is greater than the I3C FIFO size.	0A, 1B	<a href="#">Section 3.2</a>
CRP.1	Boot ROM does not give correct Code Read Protection (CRP) status when in CRP_LEVEL3.	0A	<a href="#">Section 3.3</a>
I3C.2	IBI Slave Data EXTDATA is not abortable by another master on the bus.	0A, 1B	<a href="#">Section 3.4</a>
PLL.1	PLL LOCK bit is not reliable	0A, 1B	<a href="#">Section 3.5</a>

Table 2. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 3. Errata notes

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

## 3. Functional problems detail

### 3.1 ADC.1: Missing code in Standard resolution mode

#### Introduction

LPC553x device family contains two instances of Analog to Digital Converter (ADC), ADC0 and ADC1. In single ended operation both ADCs support standard resolution mode (12-bit resolution) and High resolution mode (16-bit resolution).

#### Problem

In the standard resolution mode of single ended operation, both ADC0 and ADC1 may have approximately 1 missing code out of 20 codes. Both ADCs do not miss consecutive codes and maintain monotonicity in spite of missing codes.

#### Work-around

There is no work-around.

### 3.2 I3C.1: Data lost when using the DMA to write transmit data to I3C, and the data size is greater than the I3C FIFO size

#### Introduction

The LPC553x includes an I3C peripheral with a DMA interface that can be used to transfer data to or from the I3C data FIFO.

#### Problem

The issue occurs when using I3C to transmit data written by the SDMA to the Slave Write Data Half-word (SWDATAH)/Master Write Data Half-word (MWDATAH) registers or Master Write Message Data (MWMSG\_SDR\_DATA) register 2 bytes at a time. If the number of bytes to send exceeds the FIFO size of 8, data is overwritten by the SDMA after the FIFO becomes full.

#### Work-around

Set the DMAWIDTH field to 10 (Half word) in the Slave DMA Control (SDMACTRL)/Master DMA Control (MDMACTRL) registers and use the Slave Write Data Byte (SWDATAB)/Master Write Data Byte (MWDATAB) to write the SDMA data. Avoid using the Slave Write Data Half-word (SWDATAH)/Master Write Data Half-word (MWDATAH) registers or Master Write Message Data (MWMSG\_SDR\_DATA) register.

### 3.3 CRP.1: Boot ROM does not give correct Code Read Protection (CRP) status when in CRP\_LEVEL3

#### Introduction

Code Read Protection (CRP) is a mechanism that allows the user to enable different levels of protections in the system, so that access to the on-chip flash and use of the ISP can be restricted.

The LPC553x device family contains 5 CRP levels:

- CRP\_LEVEL0
- CRP\_LEVEL1
- CRP\_LEVEL2
- CRP\_LEVEL3
- CRP\_LEVEL4

Status of a CRP level can be returned by the LPC553x by using the debug mail box command get CRP Level (DM-AP command 2).

#### Problem

When the LPC553x is programmed with CRP\_LEVEL3 (LC\_STATE=0xF and ISP is disabled in CMPA), the Boot ROM does not return the correct status of CRP level. It returns CRP\_LEVEL2 instead. The CRP\_LEVEL3 restrictions are not impacted by this problem.

#### Work-around

There is no work-around.

### 3.4 I3C.2: More than one In Band Interrupt (IBI) extended data bytes (EXTDATA) emitted by I3C slave are not abortable by the I3C bus master.

#### Introduction

On these devices, I3C peripheral works in master (controller) as well as in slave (target) mode. This I3C peripheral supports IN Band Interrupt (IBI) feature which allows it in target mode to notify the I3C controller of an interrupt. The I3C target on this device supports up to 7 bytes of extended IBI data following mandatory data byte (MDB). Most IBIs would not use EXTDATA and are only a single MDB.

#### Problem

When I3C peripheral, on these devices is working as a target device and transmits EXTDATA with more than one byte past the MDB, EXTDATA in IBI are not abortable by the controller on I3C bus.

#### Work-around

None.

Only use the standard IBI model of one MDB or one MDB and one additional byte. It is recommended to agree on data-size(EXTDATA) with external controller before transfer, so that controller will not need to abort EXTDATA.

### 3.5 PLL.1: PLL LOCK bit is not reliable

#### Introduction

On the LPC553x devices, PLLxSTAT register of PLLs contains a LOCK detector status bit (bit 0 of PLLxSTAT register).

When the LOCK detector status bit is set to 1, the PLL is considered to be locked and stable.

The PLL LOCK signal is specified to work for Fref range from 100 kHz to 20 MHz. When the Fref is below 100 kHz or above 20 MHz, software should use a 6 ms time interval to insure the PLL will be stable.

#### Problem

On the LPC553x, the PLL status LOCK bit is not always reliable in the ranges specified and as a result, the PLL doesn't initialize correctly.

#### Work-around

For  $F_{ref} \geq 20$  MHz:

Software must wait at least  $(500\mu s + 400/F_{ref})$  ( $F_{ref}$  in Hz result in s) to ensure the PLL is stable.

For  $F_{ref} < 20$  MHz:

- If the PLL lock detector status bit is 1 before the wait time duration  $((500\mu s + 400/F_{ref}))$  is completed, the PLL is stable.
- If the PLL lock detector status bit is 0 but the wait time duration  $((500\mu s + 400/F_{ref}))$  is completed, the PLL is stable.

Software workaround is implemented in SDK 2.14 clock driver version 2.3.7.

**Remark:** This errata does not apply for spread spectrum mode.

## 4. AC/DC deviations detail

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No known errata.

## 5. Errata notes detail

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No known errata.

## 6. Contents

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