LPC54018JxM_LPC54S018JxM

Errata sheet LPC54018JxM_LPC54S018JxM

Rev. 1.3 — 27 January 2024 **Errata**

Document information

Information	Content
Keywords	LPC54018J2MET180, LPC54018J4MET180, LPC54S018J2MET180, LPC54S018J4MET180
Abstract	LPC54018JxM and LPC54S018JxM errata

1 Product identification

The LPC54018JxM_LPC54S018JxM TFBGA180 package have the following top-side marking:

- First line: LPC54018JxM_LPC54S018JxM
- Second line: ET180
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

Table 1. Device revision table

Revision identifier (R)	Revision description
1B	Initial device revision with Boot ROM version 21.1
1C	Second device revision with Boot ROM version 21.1

2 Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
USB.2	In USB full-speed device mode, the ROOT2 endpoint test fails.	1B, 1C	Section 3.1
ADC.1	High current consumption in reduced low power modes when using ADC.	1B, 1C	Section 3.2
SHA.1	Using MEMCTRL after DIGEST Ready to include more blocks via Mastering does not clear DIGEST bit.	1B, 1C	Section 3.3
USB.3	In USB high-speed device mode, device writes extra byte(s) to the buffer if the NBytes is not multiple of 8 for OUT transfer.	1B, 1C	Section 3.4
USB.4	In USB high-speed device mode, when device isochronous IN endpoint sends a packet of MaxPacketSize of 1024 bytes in response to IN token from host, the isochronous IN endpoint interrupt is not set and the endpoint command/status list entry for the isochronous IN endpoint is not updated.	1B, 1C	Section 3.5
USB.5	In USB high-speed host mode, only one transaction per micro-frame is allowed for isochronous IN endpoints.	1B, 1C	Section 3.6
PLL.1	P-divider set to 4 could generate the wrong output frequency from the PLL.	1B, 1C	Section 3.7

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3 Functional problems detail

3.1 USB.2: In USB full-speed device mode, the ROOT2 endpoint test fails

Introduction:

The LPC540xx/LPC54S0xx includes a USB full speed interface (USB0) that can operate in device mode at full speed. It supports 10 physical (5 logical) endpoints including control endpoints. The device should not respond to those endpoints which are not supported.

Problem:

The device NAKed the OUT token addressed to an endpoint that is not present on the device causing the ROOT2 endpoint test to fail.

Work-around:

There is no work-around.

3.2 ADC.1: High current consumption in reduced low power modes when using ADC

Introduction:

The 12-bit ADC controller is available on all LPC540xx/LPC54S0xx parts. The ADC can measure the voltage on any of the input signals on the analog input channel. For accurate voltage readings, the digital pin function on the ADC input channel must be disabled by writing a 0 to the DIGIMODE bit in the related IOCON register. This enables the analog mode functionality on the ADC input channel.

Problem:

For applications using the ADC, the current consumption could be higher than expected in reduced power modes (deep-sleep and deep power-down modes) or when the ADC is disabled using the PDRUNCFG register.

Work-around:

To prevent high current consumption, use the following steps in the software:

1. Following a chip reset, all 12 ADC input channels (ADC0_0 to ADC0_11) should be in Digital Mode (DIGIMODE = 1) in the related IOCON registers until the configuration of the ADC block is complete. See the Basic Configuration section in the LPC540xx/LPC54S0xx 12-bit ADC controller (ADC) chapter of the LPC540xx/LPC54S0xx User Manual.
2. After configuring the ADC, change only those pins that are used as ADC input channels to Analog Mode (DIGIMODE = 0) in the related IOCON registers before starting ADC conversions.
3. Before entering any reduced power mode (deep-sleep and deep power-down) or before powering down the ADC block (by writing to the PDEN_ADC0 bit in the PDRUNCFG register), the ADC input channel(s) must be changed back to Digital Mode.
4. After waking up from the reduced power mode or when re-enabling the ADC block (PDEN_ADC0 bit in the PDRUNCFG), the software must follow step 2 before starting ADC conversions.

3.3 SHA.1: Using MEMCTRL after DIGEST Ready to include more blocks via Mastering does not clear DIGEST bit

Introduction:

The LPC540xx/LPC54S0xx includes a SHA hash block to compute SHA1 and SHA2-256 hash digests on flash images or messages in RAM. For maximum performance and ease of use, the hash block includes a master on the internal buses of the chip to read multiple blocks of memory while hashing, without involvement of the processor. This mastering model permits hashing up to 128 K bytes of memory (Flash, RAM, or SPI Flash).

Problem:

If the application uses the mastering on up to 128 K bytes and then uses it for additional blocks (without starting new), the DIGEST (digest ready) status does not clear when starting the next sequence via mastering. If the processor or DMA is used for the additional blocks, the DIGEST status is cleared.

Work-around:

If the purpose for the additional block(s) is to hash the last block (with padding and length), then the processor or DMA may be used to write the 16 words via INDATA, and the DIGEST status will clear when the 1st word is written.

If the purpose for additional blocks is to do a large number of blocks (for example, after doing 128 K, another 64 K is to be hashed), then the 1st block may be started by the processor (that is, the processor writes the 16 words to INDATA) followed by configuring MEMADDR and MEMCTRL for the remaining blocks. The MEMCTRL should be written within 64 cycles of writing the last word to INDATA to ensure DIGEST is 0.

3.4 USB.3: In USB high-speed device mode, device writes extra byte(s) to the buffer if the NBytes is not multiple of 8 for OUT transfer

Introduction:

The LPC540xx/LPC54S0xx device family include a USB high-speed interface (USB1) that can operate in device mode at high-speed. The NBytes value represents the number of bytes that can be received in the buffer.

Problem:

The LPC540xx/LPC54S0xx USB device controller writes extra bytes to the receive data buffer if the size of the transfer is not a multiple of 8 bytes since the USB device controller always writes 8 bytes. For example, if the transfer length is 1 bytes, 7 extra bytes will be written to the receive data buffer. If the transfer length is 7 bytes, 1 extra bytes will be written to the receive data buffer.

Work-around:

Reserve an additional, intermediary buffer along with the buffer used by the application for USB data. After the USB data transfer into the intermediary buffer has been completed, use memcpy to move the data from the intermediary buffer into the application buffer, skipping the extraneous extra byte. This software work-around is implemented on the SDK software platform.

3.5 USB.4: In USB high-speed device mode, when device isochronous IN endpoint sends a packet of MaxPacketSize of 1024 bytes in response to IN token from host, the

isochronous IN endpoint interrupt is not set and the endpoint command/status list entry for the isochronous IN endpoint is not updated

Introduction:

The LPC540xx/LPC54S0xx device family include a USB high-speed interface (USB1) that can operate in device mode at high-speed. The isochronous IN endpoint supports a MaxPacketSize of 1024 bytes.

Problem:

When device isochronous IN endpoint sends a packet of MaxPacketSize of 1024 bytes in response to IN token from host, the isochronous IN endpoint interrupt is not set and the endpoint command/status list entry for the isochronous IN endpoint is not updated.

Work-around:

Restrict the isochronous IN endpoint MaxPacketSize to 1023 bytes in device descriptor.

3.6 USB.5: In USB high-speed host mode, only one transaction per micro-frame is allowed for isochronous IN endpoints

Introduction:

The LPC540xx/LPC54S0xx device family include a USB high-speed interface which can operate in host mode. Up to three high-speed transactions are allowed in a single micro-frame to support high-bandwidth endpoints. This mode is enabled by setting the Mult (Multiple) field in the Proprietary Transfer Descriptor (PTD) and is used to indicate to the host controller the number of transactions that should be executed per micro-frame. The allowed bit settings are:

00b Reserved. A zero in this field yields undefined results.

01b One transaction to be issued for this endpoint per micro-frame.

10b Two transactions to be issued for this endpoint per micro-frame.

11b Three transactions to be issued for this endpoint per micro-frame.

Problem:

For High-bandwidth mode, using multiple packets (MULT = 10b or 11b) in a frame causes unreliable operation. Only one transaction (MULT = 01b) can be issued per micro-frame.

Work-around:

There is no software workaround. Only one transaction can be issued per micro-frame.

3.7 PLL.1: P-divider set to 4 could generate the wrong output frequency from the PLL

Introduction:

On the LPC54018JxM_LPC54S018JxM PLL, the Fcco frequency must be either the actual desired output frequency, or the desired output frequency times 2 x P, where P is range from 1 to 32 (2^5). The Fcco frequency must also be a multiple of the PLL reference frequency, which is either the PLL input, or the PLL input divided by N, where N is from 2 to 256.

Problem:

The P-divider when set for divide by 4 mode can erroneously arrive in divide by 2 mode. The high frequency spikes coming from the level shifter during startup of the PLL can cause the P-divider to jump into the wrong division state only when set in divide by 4 mode. This issue affects both the System PLL and Audio PLL.

Work-around:

Use other P values other than 4 to achieve the desired output frequency. P = 1 – 32 and P ≠ 4.

4 AC/DC deviations detail

No known errata.

5 Errata notes

No known errata.

6 Revision history

Table 5. Revision history

Document ID	Release date	Description
ES_LPC54018JxM_LPC54S018JxM v. 1.3	27 January 2024	• Added revision identifier in Table 1 • Modified revision identifiers in Table 2 • Added Section 3.7
ES_LPC54018JxM_LPC54S018JxM v. 1.2	3 May 2021	• Added USB.4 errata
		• Added USB.5 errata
ES_LPC54018JxM_LPC54S018JxM v. 1.1	17 February 2021	• Added USB.3 errata
ES_LPC54018JxM_LPC54S018JxM v. 1	27 January 2019	• Initial version

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