Mask Set Errata for Mask P90A

This report applies to mask P90A for these products:

- MKM35Z512VLQ7
- MKM35Z256VLL7
- MKM35Z256VLQ7
- MKM35Z512VLL7

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR050324	2 bus cycles are required to make RNGA work correctly for first time enabling the RNGA by SCGC register since bootup
ERR007735	MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock
ERR006396	sLCD: LCD_GCR[RVTRIM] bits are in reverse order
ERR004647	UART: Flow control timing issue can result in loss of characters if FIFO is not enabled

Table 2. Revision History

Revision	Changes
15Apr2020	No changes to errata with this revision

ERR050324: 2 bus cycles are required to make RNGA work correctly for first time enabling the RNGA by SCGC register since bootup

Description: To make the RNGA work, the SCGC register bit need to be enabled to provide clock to RNGA module. However, if operate the RNGA register right after the SCGC register operation(ungate), the RNGA register write can't work properly but the actual write will happen 2 bus clock cycle later.

Workaround: 2 bus cycles are required to make RNGA work correctly for first time enabling the RNGA by SCGC register since bootup

ERR007735: MCG: IREFST status bit may set before the IREFS multiplexor switches the FLL reference clock

Description: When transitioning from MCG clock modes FBE or FEE to either FBI or FEI, the MCG_S[IREFST] bit will set to 1 before the IREFS clock multiplexor has actually selected the slow IRC as the reference clock. The delay before the multiplexor actually switches is:

2 cycles of the slow IRC + 2 cycles of OSCERCLK

In the majority of cases this has no effect on the operation of the device.

Workaround: In the majority of applications no workaround is required. If there is a requirement to know when the IREFS clock multiplexor has actually switched, and OSCERCLK is no longer being used by the FLL, then wait the equivalent time of:

2 cycles of the slow IRC + 2 cycles of OSCERCLK

after MCG_S[IREFST] has been set to 1.

ERR006396: sLCD: LCD_GCR[RVTRIM] bits are in reverse order

Description: The four bits of LCD_GCR[RVTRIM] are in reverse order, in such a way that the LSB corresponds to bit 27 and the MSB corresponds to bit 24 of the LCD_GCR. The RVTRIM adjustment from lower voltage to higher voltage does not follow a linear increase in the LCD_GCR[RVTRIM] value. The RVTRIM adjustment should follow this sequence:

0,8,4,12,2,10,6,14,1,9,5,13,3,7,11,15

to achieve a linear increase from lower voltage to higher voltage.

The reset value of this field is still 8, which corresponds to a low voltage value of the VIREG.

Workaround: You can use a lookup table with the correct order of RVTRIM values for a linear change on the VIREG voltage (contrast). If planning to use a user-selectable contrast, a memory buffer is required to keep track of the logic value of the RVTRIM. When required to increase or decrease the contrast of the LCD, the buffer pointer should be increased or decreased accordingly and the corresponding value from the lookup table should be written to the LCD_GCR[RVTRIM].

To avoid a low voltage on VIREG after reset, LCD_GCR[RVTRIM] must be updated during the LCD initialization routine.

ERR004647: UART: Flow control timing issue can result in loss of characters if FIFO is not enabled

Description: On UARTx modules with FIFO depths greater than 1, when the /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit

and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

Workaround: Always enable the RxFIFO if you are using flow control for UARTx modules with FIFO depths greater than 1. The receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

Note that only UARTx modules with FIFO depths greater than 1 are affected. The UARTs that do not have the RxFIFO feature are not affected. Check the Reference Manual for your device to determine the FIFO depths that are implemented on the UARTx modules for your device.

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