

K11D/K21D 50 MHz Rev 1.1 K11D/K21D 50 MHz Rev 2 Differences Document

1 Overview

This document outlines the feature differences between the following Kinetis MCUs:

- K11D or K21D 50 MHz Rev 1.1 (maskset 1N89E)
- K11D or K21D 50 MHz Rev 2 (maskset 0N62J)

NOTE

A non-disclosure agreement (NDA) is required for access to detailed information regarding security-related modules, including the DryIce tamper detection module. This document provides high-level differences between the 1N89E and 0N62J masksets but excludes detailed differences involving the DryIce tamper detection security module. Detailed differences involving DryIce is included in the NDA version of this document EB801.

For more information on obtaining an NDA, please contact your local Freescale sales representative.

[Table 1](#) shows the mask set number along with corresponding device revision number found in the System Device Identification Register

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(SIM_SDID[REVID]), Part Identification Number (PRN) from the JTAG ID Register, as well as the external revision number associated with each silicon mask set. The silicon mask set is marked on the top of each chip package below the part number.

Table 1. Mask set number to device revision

Revision	Mask Set	REVID	PRN
1.1	1N89E	0001	0001
2	0N62J	1001	1001

2 References

For more information, refer to the following documents:

- Kinetis K-Series K11D Reference Manual
 - 121-pin Package
 - K11P121M50SF4RM_NDA (applies to Rev 1.x silicon)
 - K11P121M50SF4V2RM_NDA (applies to Rev 2 silicon)
 - 80-pin Package
 - K11P80M50SF4RM_NDA (applies to Rev 1.x silicon)
 - K11P80M50SF4V2RM_NDA (applies to Rev 2 silicon)
- Kinetis K-Series K21D Reference Manual
 - 121-pin Package
 - K21P121M50SF4RM_NDA (applies to Rev 1.x silicon)
 - K21P121M50SF4V2RM_NDA (applies to Rev 2 silicon)
 - 80-pin Package
 - K21P80M50SF4RM_NDA (applies to Rev 1.x silicon)
 - K21P80M50SF4V2RM_NDA (applies to Rev 2 silicon)
- Kinetis K-Series K11D Data Sheet
 - 121-pin Package
 - K11P121M50SF4_NDA (applies to Rev 1.x silicon)
 - K11P121M50SF4V2_NDA (applies to Rev 2 silicon)
 - 80-pin Package
 - K11P80M50SF4_NDA (applies to Rev 1.x silicon)
 - K11P80M50SF4V2_NDA (applies to Rev 2 silicon)
- Kinetis K-Series K21D Data Sheet
 - 121-pin Package
 - K11P121M50SF4_NDA (applies to Rev 1.x silicon)
 - K11P121M50SF4V2_NDA (applies to Rev 2 silicon)
 - 80-pin Package

- K11P80M50SF4_NDA (applies to Rev 1.x silicon)
- K11P80M50SF4V2_NDA (applies to Rev 2 silicon)
- Kinetis K-Series Mask Set Errata for Mask 1N89E
- Kinetis K-Series Mask Set Errata for Mask 0N62J

3 Part Number Differences

The following part numbers refer to K11D or K21D 50 MHz Rev 1.1 (maskset 1N89E) units:

K11DN512 $xyy5$	K21DN512 $xyy5$
K11DX256 $xyy5$	K21DX256 $xyy5$
K11DX128 $xyy5$	K21DX128 $xyy5$

Where x refers to the operating temperature rating and yy refers to the package code (available in the data sheet).

The following part numbers refer to K11D or K21D 50 MHz Rev 2 (maskset 0N62J) units:

K11DN512A $xyy5$	K21DN512A $xyy5$
K11DX256A $xyy5$	K21DX256A $xyy5$
K11DX128A $xyy5$	K21DX128A $xyy5$

Note that K11D and K21D 50 MHz Rev 2 units are distinguished from Rev 1.1 units by the addition of the “A” character after the flash memory size indicator in the part number.

4 Functional Differences

4.1 Feature Enhancements from K11D/K21D Rev 1.1 to K11D/K21D Rev 2

Migrating from the K11D/K21D Rev 1.1 MCU to the K11D/K21D Rev 2 MCU provides the following primary benefits:

- Enhancements to DryIce tamper detection
- Reduction in VBAT current consumption

For details concerning the above benefits, please consult the NDA version of this document, EB801.

4.2 Software Migration Considerations

For details concerning software migration considerations between the K11D/K21D Rev 1.1 MCU and the K11D/K21D Rev 2 MCU, please consult the NDA version of this document, EB801.

4.3 Errata Fixes

[Table 2](#) outlines various errata that have been fixed when migrating to K11D/K21D Rev 2.

Table 2. Errata related to revision 2 migration

Errata ID	Errata Title	1N89E K11D/K21D Rev 1.1	0N62J K11D/K21D Rev 2
e5751	FTFx: Launching the Read 1's Section command (RD1SEC) on an entire flash block results in accesserror (ACCER).	Present	Fixed
e5706	FTFx: MCU security is inadvertently enabled (secured) if a mass erase is executed when the flash blocks/halves are swapped. This issue only affects applications that use the flash swap feature.	Present	Fixed
e5499	MCG: A reset or interrupt request due to a PLL loss of lock (LOL) condition will not occur asynchronously.	Present	Fixed
e4590	MCG: Transitioning from VLPS to VLPR low power modes while in BLPI clock mode is not supported.	Present	Fixed
e6665	Operating requirements: Limitation of the device operating range.	Present	Fixed
e6348	PMC: Incorrect reset source indication when waking up from VLLS0 mode.	Present	Fixed
e5472	SMC: Mode transition VLPR→VLLS0 (POR disabled)→RUN, will cause POR & LVD.	Present	Fixed
e5952	SMC: Wakeup via the LLWU from LLS/VLLS to RUN to VLPR incorrectly triggers an immediate wakeup from the next low power mode entry.	Present	Fixed
e5928 ¹	USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases.	Present	Fixed

¹ Applicable only to K21D devices because K11D devices do not feature USB.

5 Summary and Conclusion

This document outlined the primary differences between the Kinetis K11D/K21D Rev 1.1 MCU (maskset 1N89E) and the K11D/K21D Rev 2 MCU (maskset 0N62J).

Migrating to the K11D/K21D Rev 2 MCU from the K11D/K21D Rev 1.1 MCU is expected to provide benefits regarding DryIce tamper detection, reduction in VBAT current consumption, and various errata fixes.

6 Revision History

Revision 0 is the initial release of this document.

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