EB361
Rev. 3, 10/2005

Functional Differences Between the DSP56307 and DSP56L307

The DSP56307 and DSP56L307, two members of the Freescale DSP56300 family of programmable digital signal processors (DSPs), support wireless infrastructure applications with general filtering operations. Like other DSP56300 family members, these devices preserve code compatibility. Unique to each of these devices is an on-chip enhanced filter coprocessor (EFCOP) that processes filter algorithms in parallel with the operation of the core, thus increasing overall DSP performance and efficiency. The DSP56L307 and DSP56307 are signal pin-compatible. The DSP56307 is offered in the Freescale 15 mm × 15 mm 196-pin plastic ball grid array (PBGA) package. The DSP56L307 is offered in the Freescale 15 mm × 15 mm 196-pin mold array process-ball grid array (MAP-BGA) package.

Although the DSP56307 and DSP56L307 have similar features, they differ significantly in several areas. This document describes these functional differences.

CONTENTS

1 Design Requirements

The DSP56L307 uses the Freescale HiP4 process technology. At a minimum, the migration of the DSP56307 to the HiP4 process affects the core operating voltage, values used in the ID registers, memory block size, maximum operating frequency, thermal characteristics, and packaging. Applications using the DSP56307 can integrate the DSP56L307 directly as long as the correct core operating voltage is used, programming is changed to reflect the new ID register values, possible contention issues due to the different memory block size are addressed, and the

operating frequency does not exceed 100 MHz. Differences in thermal characteristics and packaging should not affect the application. Although the DSP56L307 can operate up to 150 MHz, there is a resulting trade-off because at that frequency, the DSP56L307 does not support DRAM access, external clock signals (CLKOUT, BCLK, and $\overline{\text{BCLK}}$), or Address Trace mode and requires additional wait states for correct SRAM access.

2 Summary of Differences

Table 1 summarizes the differences between the DSP56307 and the DSP56L307 presented in this document.

Table 1. Summary of Differences Between DSP56307 and DSP56L307

Feature	DSP56307	DSP56L307
Voltage	2.5 V ± 0.2 V (core and internal PLL)	1.8 V ± 0.1 V (core and internal PLL)
ID Registers Update	IDR = $XXX307 JTAG Identification Register = 0bXXXX 000110 00000 00111 00000001110 1	IDR = $XXX317 JTAG Identification Register = 0bXXXX 000110 00000 10001 00000001110 1
Internal Memory Block Size	256 × 24-bit words	1024 × 24-bit words
Maximum Operating Frequency	100 MHz	150 MHz
Thermal Characteristics	θ_{JA} = 51.9 °C/W θ_{JC} = 13.1 °C/W Ψ_{JT} = 2.45 °C/W	θ_{JA} = 53 °C/W θ_{JC} = 8 °C/W Ψ_{JT} = 2 °C/W
Packaging	15 mm × 15 mm 196-pin plastic ball grid array (PBGA) package	15 mm × 15 mm 196-pin mold array process-ball grid array (MAP-BGA) package
DRAM Access Support	Supported at 100 MHz (maximum operating frequency)	Supported up to 100 MHz, but not supported above 100 MHz.
Clock Outputs	CLKOUT, BLCK, and $\overline{\text{BCLK}}$ supported	CLKOUT, BCLK, and $\overline{\text{BLCK}}$ not supported above 100 MHz
Address Trace Mode	Supported	Not supported above 100 MHz
SRAM Access Wait States	Accesses require at least one wait state. Programming the Bus Control Register for two or three wait states adds no trailing wait states.	At 100 MHz: Accesses require at least one wait state. Programming the Bus Control Register for two or three wait states adds one trailing wait state. At 150 MHz: Accesses require at least two wait states. Programming the Bus Control Register for two or three wait states adds one trailing wait state.

3 Voltage

The DSP56L307 and DSP56307 are dual-voltage devices. The DSP56L307 core and internal PLL operate from a 1.8 V ± 0.1 V supply, while the DSP56307 core operates from a 2.5 V ± 0.2 V supply. The input/output pins on each device operate from an independent 3.3 V supply. Using a variable supply for the core voltage allows designers to use the same board design for either device.

4 ID Registers Update

The DSP56300 core provides a dedicated user-accessible test access port (TAP) based on the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*. With the IDCODE instruction, a user can determine from the TAP ID Register information about the manufacturer, part number, and version of a board component. The ID register is updated to reflect information specific to the DSP56L307.

The Device Identification register (IDR) is a 24-bit, read-only factory-programmed register that identifies DSP56300 family members. It specifies the derivative number and revision number of the device. This information is used in testing or by software. The IDR is updated to reflect information specific to the DSP56L307.

5 Memory Block Size

In the DSP56L307, the internal memory block size is 1024 × 24-bit words compared to 256 × 24-bit words in the DSP56307. This change in size affects DMA/core contention and EFCOP/core contention.

In the DSP56307, the internal RAM is divided into 256-word blocks. A situation of contention exists if the core and DMA access the same block of 256 words. If both the core and DMA access the same block, then the core always has priority, and the DMA is delayed until a free slot is available. If the core and DMA access different blocks, they do not interfere with one another; each continues to operate at its maximum speed. Memory block boundaries are located at 256 word addresses.

This same situation applies to the DSP56L307, except that contention exists if the core and DMA access the same block of 1024 words. Memory block boundaries are located at 1 K word addresses. To avoid DMA/core contention, DMA and core accesses must address different 1024-word blocks. **Figure 1** shows two examples of core and DMA accesses to different 256-word blocks in the DSP56307 (no contention) and the resulting effect of these same accesses in the DSP56L307.

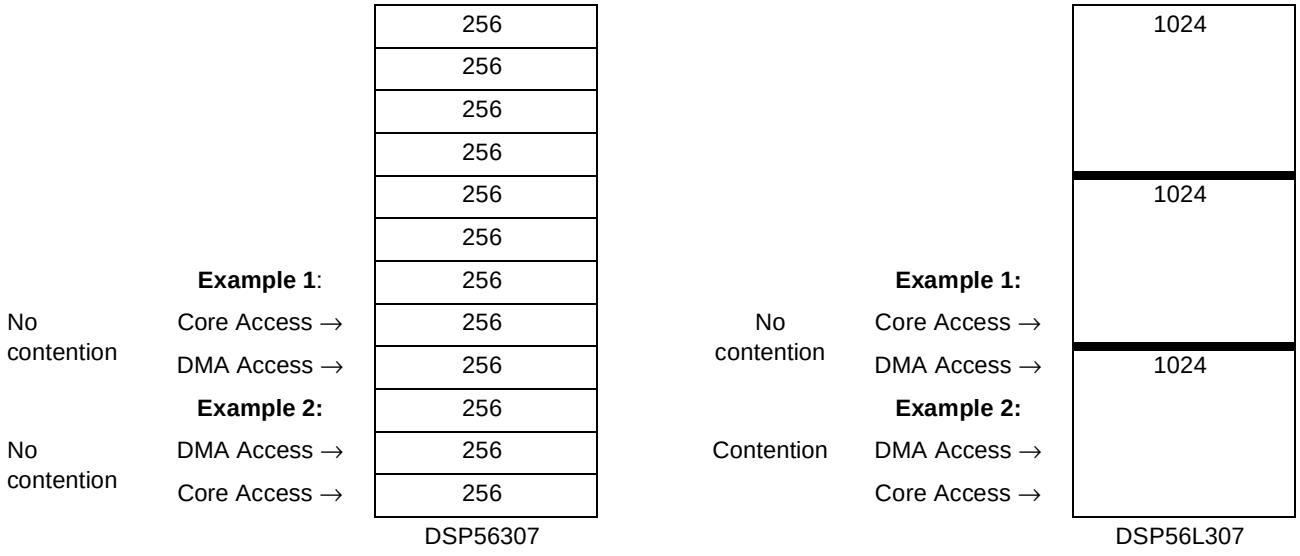

Figure 1. Memory Block Sizes and DMA/Core Accesses

The same change in block size applies to EFCOP/core contention. For both the DSP56307 and the DSP56L307, the DSP56300 core and the EFCOP share the lowest 4 K (sixteen 256-word blocks in the DSP56307 and four 1024-word blocks in the DSP56L307) of X and Y memory, and the DMA controller can not access these blocks. Unlike Core/DMA contention, EFCOP/core contention may result in faulty data output in the Filter Data Output Register.

For the DSP56307, contention occurs if the EFCOP and core attempt to access the same 256-word block. For the DSP56L307, contention occurs if the EFCOP and core attempt to access the same 1024-word block. Both the DSP56307 and DSP56L307 include the Data/Coefficient Transfer Contention (FCONT) bit in the EFCOP Control Status Register. The FCONT bit allows programmers to detect when EFCOP/core contention occurs.

6 Maximum Operating Frequency

The maximum operating frequency for the DSP56L307 is 150 MHz compared to 100 MHz for the DSP56307. The DSP56L307 is a fully static design and specified to operate down to 0 Hz (DC). The device is characterized at minimum frequencies approaching 0 Hz.

7 Thermal Characteristics

Because the die size of the DSP56L307 is smaller than that of the DSP56307, the θ_{JA} and θ_{JC} values for the DSP56L307 are expected to increase by no more than 10°C/W and 5°C/W, respectively. Preliminary thermal characteristics are made available in the technical data sheet for the DSP56L307.

8 Packaging

The DSP56L307 and DSP56307 are signal pin-compatible, but the DSP56307 uses the Freescale 15 mm × 15 mm 196-pin plastic ball grid array (PBGA) package, whereas the DSP56L307 uses the Freescale 15 mm × 15 mm 196-pin mold array process-ball grid array (MAP-BGA) package. The two packages have identical footprints. The detailed package information for the MAP-BGA package is included in the technical data sheet for the DSP56L307. For a detailed comparison of the PBGA and MAP-BGA packages, refer to *Mechanical Differences Between the 196-pin MAP-BGA and 196-pin PBGA Packages*, order number EB360, which is available through the web site listed on the back cover of this document.

9 DRAM Access Support

DRAM accesses are supported in the DSP56307 and DSP56L307 at 100 MHz. DRAM accesses are not supported in the DSP56L307 above 100 MHz operating frequency.

10 Clock Output Signals

At 100 MHz, the DSP56L307 operates the same way as the DSP56307, supporting the Clock Output (CLKOUT), Bus Clock (BCLK), and Bus Clock Not ($\overline{\text{BCLK}}$) signals. The CLKOUT output pin provides a 50 per cent duty cycle output clock synchronized to the internal processor clock when the Phase Lock Loop (PLL) is enabled and locked.

Above 100 MHz, CLKOUT produces a low-amplitude waveform that is not usable by devices external to the DSP. Therefore, the Clock Output (CLKOUT), Bus Clock (BCLK), and Bus Clock Not ($\overline{\text{BCLK}}$) pins are not supported in the DSP56L307 above 100 MHz. Data sheet tables and figures denote the frequency- dependent clocking features.

Several alternatives to using CLKOUT exist, such as enabling bus arbitration by setting the Asynchronous Bus Arbitration Enable Bit (ABE) in the Operating Mode register. When set, the ABE bit eliminates the setup and hold time requirements with respect to CLKOUT for $\overline{\text{BB}}$ and $\overline{\text{BG}}$.

11 Address Trace Mode

The Address Trace mode is not supported in the DSP56L307 above 100 MHz. When the Address Tracing Enable bit (ATE) in the Operating Mode register (OMR) is set in the DSP56307, Address Trace mode is enabled, allowing the user to determine the address of internal memory accesses. Specifically, when ATE is set, BCLK serves as a sampling signal and results in output of the memory access address on the address lines. Since the DSP56L307 does not support BCLK above 100 MHz, running the chip at its maximum operating frequency (150 MHz) means that BCLK signal does not have a high enough amplitude to initiate the sampling process, and the DSP does not output any addresses. At 100 MHz or below, the DSP56L307 operates just like the DSP56307. However, when operated at 150 MHz, the DSP56L307 does not support Address Trace Mode and the ATE bit in the OMR of the DSP56L307 is reserved.

12 SRAM Access Wait States

For 150 MHz operation, the data sheet for the DSP56L307 specifies that SRAM accesses require at least two wait states instead of the minimum one wait state specified for 100 MHz operation. In addition, when the Bus Control Register is configured for two or three wait states, the DSP adds one trailing wait state. The DSP56307 does not add any trailing wait states if the Bus Control Register is configured for two or three wait states. **Table 2** and **Table 3** show the number of trailing wait states associated with the number of wait states configured in the Bus Control Register for the DSP56307 versus the DSP56L307.

Table 2. Additional Trailing Wait States for DSP56307

Wait States in the Bus Control Register	Additional Trailing Wait States for DSP56307
1–3	0
4–7	1
≥ 8	2

Table 3. Additional Trailing Wait States for DSP56L307

Wait States in the Bus Control Register	Additional Trailing Wait States for DSP56L307
1 (at ≤100 MHz)	0
2–7	1
≥ 8	2

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations not listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GMBH
Technical Information Center
Schatzbogen 7
81829 München, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
+800 2666 8080

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Order No.: EB361
Rev. 3
10/2005