Functional Differences Between the DSP56307 and DSP56311

The DSP56311 and DSP56307, two members of the Freescale DSP56300 family of programmable DSPs, support wireless infrastructure applications with general filtering operations. Like other DSP56300 family members, these devices preserve code compatibility. Unique to each of these devices is an on-chip enhanced filter coprocessor (EFCOP) that processes filter algorithms in parallel with the operation of the core, thus increasing overall DSP performance and efficiency. The DSP56311 and DSP56307 are signal pin-compatible and offered in the Freescale 15 mm × 15 mm 196-pin Molded-Array Plastic-Ball Grid Array (MAP-BGA) package. Although the DSP56307 and DSP56311 have similar features, they differ significantly in size of on-chip memory, performance, and core voltage. This document describes these functional differences.

CONTENTS

1 DSP56307 Migration

The DSP56311 uses the Freescale process technology HiP4. The DSP56307 migrated to the HiP4 process as the DSP56L307. Migration to the HiP4 process affects the memory block size, voltage, operating frequency, DRAM access support, pins, Address Tracing mode, SRAM access wait states, and the JTAG and Device Identification registers for the DSP56307 in the same way as described for the DSP56311. The sections titled “Memory Block Size,” “DRAM Access Support,” “SRAM Access Support,” and “ID Registers Update” specifically address software implications for migrating DSP56307 designs to DSP56311 designs.

2 Summary of Differences

Table 1 summarizes the differences between the DSP56307 and the DSP56311 presented in this document.

Table 1. Summary of Differences Between DSP5307 and DSP56311

Feature	DSP56307	DSP56311
Voltage	2.5v +/- 0.2v (core and internal PLL)	1.8v +/- 0.1v (core and internal PLL)
Operating Frequency	100 MHz (maximum frequency)	150 MHz (maximum frequency)
DRAM Access Support	Supported at 100 MHz	Not supported above 100 MHz
Pins	CLKOUT and BCLK functional	CLKOUT and BCLK not functional above 100 MHz
Thermal Characteristics	Lower θ_{JA} and θ_{JC} values due to larger die size compared to the DSP56311	Higher θ_{JA} and θ_{JC} values due to smaller die size compared to the DSP56307
Address Trace Mode	Supported	Not supported above 100 MHz
SRAM Access Wait States	• Accesses at 1 wait state and above • No trailing wait states for Bus Control Register wait states 2 and 3	• Accesses at 2 wait states and above • One trailing wait state for Bus Control Register wait states 2 and 3
JTAG and Device ID Registers Update	JTAG and Device ID registers information specific to the DSP56307	JTAG and Device ID registers information specific to the DSP56311
Memory	64 K × 24-bit on-chip RAM	128 K × 24-bit on-chip RAM
Internal Memory Block Size	256 × 24-bit words	1024 × 24-bit words

3 Voltage

The DSP56311 and DSP56307 are dual-voltage devices. The DSP56311 core and internal PLL operate from a 1.8 ± 0.1 V supply, while the DSP56307 core operates from a 2.5 ± 0.2 V supply. The input/output pins on each device operate from an independent 3.3 V supply. Using a variable supply for the core voltage allows designers to use the same board design for either device.

4 Operating Frequency

The maximum operating frequency for the DSP56311 is 150 MHz compared to 100 MHz for the DSP56307.

The DSP56311 is a fully static design and specified to operate down 0 Hz (DC). The device is characterized at minimum frequencies approaching 0 Hz.

5 DRAM Access Support

DRAM accesses are not supported in the DSP56311 at 150 MHz. DRAM accesses are supported in the DSP56307 and the DSP56311 at 100 MHz.

6 Pins

The Clock Output (CLKOUT) and Bus Clock (BCLK and $\overline{\text{BCLK}}$) pins are not functional in the DSP56311 above 100 MHz. Data sheet tables and figures that reference these signals are modified accordingly.

The CLKOUT output pin provides a 50 percent duty cycle output clock synchronized to the internal processor clock when the Phase Lock Loop (PLL) is enabled and locked. Above 100 MHz, CLKOUT produces a low-amplitude waveform that is not guaranteed to be usable externally by other devices.

Several alternatives to using CLKOUT exist, such as enabling bus arbitration by setting the Asynchronous Bus Arbitration Enable Bit (ABE) in the Operating Mode register. When set, the ABE bit eliminates the setup and hold time requirements with respect to CLKOUT for $\overline{BB}$ and $\overline{BG}$.

7 Thermal Characteristics

Due to the smaller die size of the DSP56311 compared to the DSP56307, the θ_{JA} and θ_{JC} values for the DSP56311 are expected to increase by no more than 10°C/W and 5°C/W respectively. Preliminary thermal characteristics are available in the technical data sheet for the DSP56311.

8 Address Trace Mode

The Address Trace mode is not supported in the DSP56311 above 100 MHz. When the Address Tracing Enable bit (ATE) in the Operating Mode register (OMR) is set in the DSP56307, Address Trace mode is enabled, allowing the user to determine the address of internal memory accesses. Specifically, when ATE is set, BCLK and $\overline{BCLK}$ serve as sampling signals and results in output of the memory access address on the address lines. Above 100 MHz in the DSP56311, no BCLK signal is available to initiate the sampling process, and the DSP does not output any addresses. Therefore, the Address Trace Mode is not functional because BCLK is not functional in the DSP56311 above 100 MHz. The ATE bit in the OMR of the DSP56311 is reserved when operating above 100 MHz.

9 SRAM Access Wait States

The data sheet for the DSP56311 specifies SRAM accesses at 2 wait states and above instead of 1 wait state and above as specified for the DSP56307. In addition, the Bus Control Register wait states 2 and 3 have one trailing wait state in the DSP56311 compared to no trailing wait states for the Bus Control Register wait states 2 and 3 in the DSP56307. **Table 2** shows the number of additional trailing wait states associated with wait states in the Bus Control Register for the DSP56307 and the DSP56311.

Table 2. Additional Trailing Wait States

DSP56307		DSP56311	
Wait States in the Bus Control Register	**Additional Trailing Wait States**	**Wait States in the Bus Control Register**	**Additional Trailing Wait States**
1–3	0	2–7	1
4–7	1		
≥ 8	2	≥ 8	2

10 ID Registers Update

The DSP56300 core provides a dedicated user-accessible test access port (TAP) based on the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*. With the IDCODE instruction, a user can determine from the TAP ID Register information about the manufacturer, part number, and version of a board component. The ID register will be updated to reflect information specific to the DSP56311.

The Device Identification register (IDR) is a 24-bit, read-only factory-programmed register that identifies DSP56300 family members. It specifies the derivative number and revision number of the device. This information is used in testing or by software. The IDR was updated to reflect information specific to the DSP56311.

11 Memory

The DSP56311 has a total of 128 K × 24-bit on-chip RAM compared to the 64 K × 24-bit on-chip RAM of the DSP56307. In both devices, RAM is partitioned into program memory space (P), and X and Y data memory space. The program memory space (P) includes internal Program RAM, an internal Instruction Cache (that behaves as Program RAM when the cache is disabled or reassigned to external program RAM when cache is enabled), a boot program ROM, and an optional off-chip memory expansion. The data memory space is divided into X data memory and Y data memory in order to work with the two address arithmetic logic units (ALUs) and to feed two operands simultaneously to the data ALU. Each data memory space includes internal RAM and optional off-chip memory expansion. **Figure 1** shows the default memory block diagram for the DSP56307. **Figure 2** shows the default memory block diagram for the DSP56311.

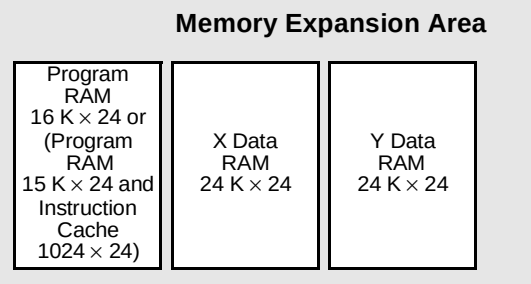


Figure 1. DSP56307 Memory Block Diagram

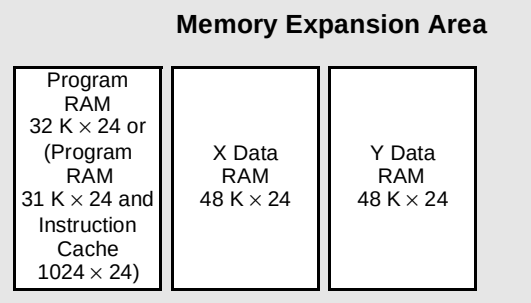


Figure 2. DSP56311 Memory Block Diagram

The size of partitions between Program and Data on-chip RAM depends on the settings of two bits:

- *Cache Enable bit (CE) in the Status Register.* When the CE bit is set, the Instruction Cache is enabled and the lowest 1 K of Program RAM is reserved as Instruction Cache.
- *Memory Switch Mode bit (MS bit 7 in the Operating Mode Register).* When the MS bit is set, Memory Switch Mode is enabled, and portions of the internal X and Y data memory become part of the on-chip internal Program RAM.

The amount of X and Y data memory that becomes part of program RAM depends on two additional bits, the Memory Switch Configuration bits (MSW[1–0], bits 14–13 in the Operating Mode Register). The MSW bits define four different size portions of X and Y data memory that become part of the internal program RAM. **Table 3** (DSP56307) and **Table 4** (DSP56311) show partitioning of on-chip RAM in the DSP56307 and DSP56311 relative to these bit settings.

Table 3. DSP56307 Switch Memory Configuration

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache (CE)	Switch Mode (MS)	MSW1	MSW0
16 K × 24-bit	0	24 K × 24-bit	24 K × 24-bit	disabled	disabled	0/1	0/1
15 K × 24-bit	1024 × 24-bit	24 K × 24-bit	24 K × 24-bit	enabled	disabled	0/1	0/1
48 K × 24-bit	0	8 K × 24-bit	8 K × 24-bit	disabled	enabled	0	0
47 K × 24-bit	1024 × 24-bit	8 K × 24-bit	8 K × 24-bit	enabled	enabled	0	0
40 K × 24-bit	0	12 K × 24-bit	12 K × 24-bit	disabled	enabled	0	1
39 K × 24-bit	1024 × 24-bit	12 K × 24-bit	12 K × 24-bit	enabled	enabled	0	1
32 K × 24-bit	0	16 K × 24-bit	16 K × 24-bit	disabled	enabled	1	0
31 K × 24-bit	1024 × 24-bit	16 K × 24-bit	16 K × 24-bit	enabled	enabled	1	0
24 K × 24-bit	0	20 K × 24-bit	20 K × 24-bit	disabled	enabled	1	1
23 K × 24-bit	1024 × 24-bit	20 K × 24-bit	20 K × 24-bit	enabled	enabled	1	1
*Includes 4 K × 24-bit shared memory (that is, memory shared by the core and the EFCOP)							

Table 4. DSP56311 Switch Memory Configuration

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache (CE)	Switch Mode (MS)	MSW1	MSW0
32 K × 24-bit	0	48 K × 24-bit	48 K × 24-bit	disabled	disabled	0/1	0/1
31 K × 24-bit	1024 × 24-bit	48 K × 24-bit	48 K × 24-bit	enabled	disabled	0/1	0/1
96 K × 24-bit	0	16 K × 24-bit	16 K × 24-bit	disabled	enabled	0	0
95 K × 24-bit	1024 × 24-bit	16 K × 24-bit	16 K × 24-bit	enabled	enabled	0	0
80 K × 24-bit	0	24 K × 24-bit	24 K × 24-bit	disabled	enabled	0	1
79 K × 24-bit	1024 × 24-bit	24 K × 24-bit	24 K × 24-bit	enabled	enabled	0	1
64 K × 24-bit	0	32 K × 24-bit	32 K × 24-bit	disabled	enabled	1	0
63 K × 24-bit	1024 × 24-bit	32 K × 24-bit	32 K × 24-bit	enabled	enabled	1	0
48 K × 24-bit	0	40 K × 24-bit	40 K × 24-bit	disabled	enabled	1	1
47 K × 24-bit	1024 × 24-bit	40 K × 24-bit	40 K × 24-bit	enabled	enabled	1	1
*Includes 10 K × 24-bit shared memory (that is, memory shared by the core and the EFCOP)							

Table 5 (DSP56307) and **Table 6** (DSP56311) specify the address ranges directly affected by the switch operation.

Table 5. DSP56307 Space and Address Mapping in Memory Switch Mode

No Switch (MS = 0)	Switch (MS = 1)	Affected Switch Configuration (MSW[1–0] bits when MS = 1)
X:$2000–$2FFF	P:$B000–$BFFF	MSW[1–0] = 00
Y:$2000–$2FFF	P:$A000–$AFFF	MSW[1–0] = 00

Table 5. DSP56307 Space and Address Mapping in Memory Switch Mode (Continued)

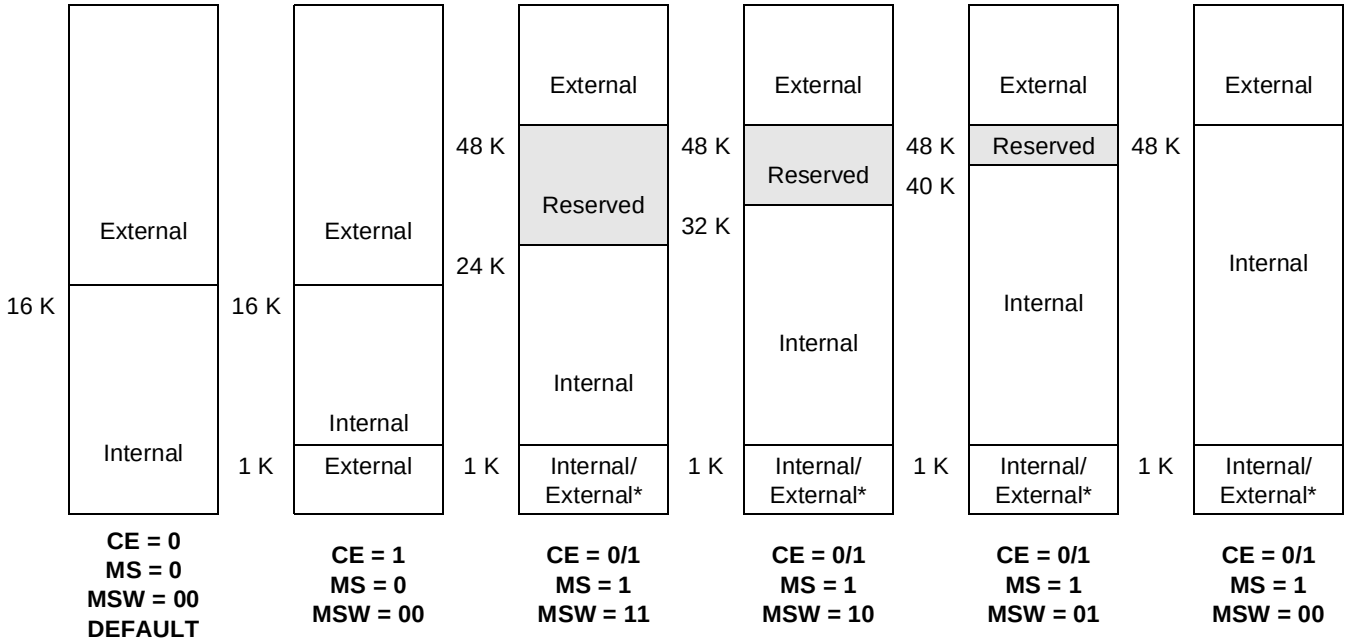
No Switch (MS = 0)	Switch (MS = 1)	Affected Switch Configuration (MSW[1–0] bits when MS = 1)
X:$3000–$3FFF	P:$9000–$9FFF	MSW[1–0] = 00 or 01
Y:$3000–$3FFF	P:$8000–$8FFF	MSW[1–0] = 00 or 01
X:$4000–$4FFF	P:$7000–$7FFF	MSW[1–0] = 00 or 01 or 10
Y:$4000–$4FFF	P:$6000–$6FFF	MSW[1–0] = 00 or 01 or 10
X:$5000–$5FFF	P:$5000–$5FFF	MSW[1–0] = 00 or 01 or 10 or 11
Y:$5000–$5FFF	P:$4000–$4FFF	MSW[1–0] = 00 or 01 or 10 or 11

Table 6. DSP56311 Space and Address Mapping in Memory Switch Mode

No Switch (MS = 0)	Switch (MS = 1)	Affected Switch Configuration (MSW[1–0] bits when MS = 1)
X:$4000–$5FFF	P:$16000–$17FFF	MSW[1–0] = 00
Y:$4000–$5FFF	P:$14000–$15FFF	MSW[1–0] = 00
X:$6000–$7FFF	P:$12000–$13FFF	MSW[1–0] = 00 or 01
Y:$6000–$7FFF	P:$10000–$11FFF	MSW[1–0] = 00 or 01
X:$8000–$9FFF	P:$E000–$FFFF	MSW[1–0] = 00 or 01 or 10
Y:$8000–$9FFF	P:$C000–$DFFF	MSW[1–0] = 00 or 01 or 10
X:$A000–$BFFF	P:$A000–$BFFF	MSW[1–0] = 00 or 01 or 10 or 11
Y:$A000–$BFFF	P:$8000–$9FFF	MSW[1–0] = 00 or 01 or 10 or 11

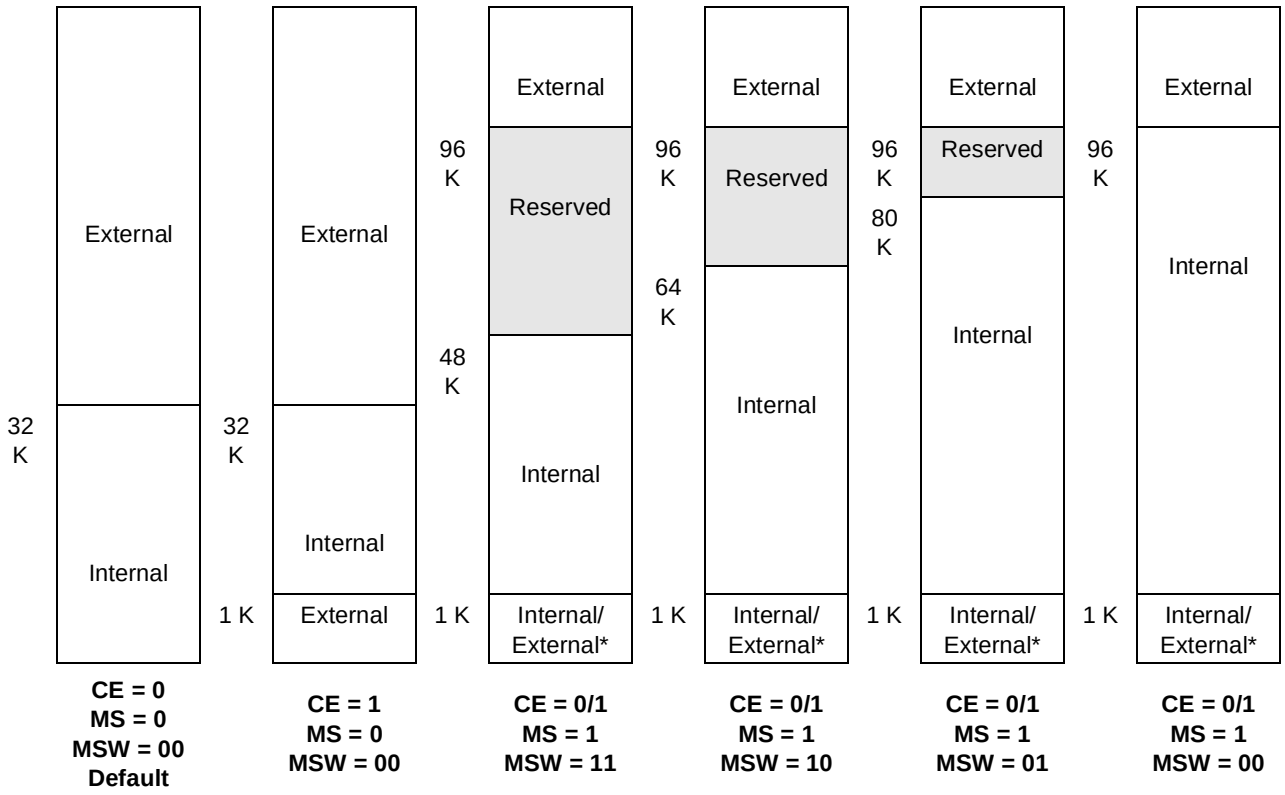
Figure 3 shows a memory map configuration of Program Memory switching for the DSP56307. **Figure 4** shows a memory map configuration of Program Memory switching for the DSP56311.

Figure 3. DSP56307 Program Memory Switching Configuration



*The lowest 1 K addressed by Program Memory is internal if CE = 0 and external if CE = 1.

Figure 4. DSP56311 Program Memory Switching Configuration



*The lowest 1 K addressed by Program Memory is internal if CE = 0 and external if CE = 1.

Figure 5 shows a memory map configuration of X and Y Data Memory switching for the DSP56307. **Figure 6** shows a memory map configuration of X and Y Data Memory switching for the DSP56311.

Figure 5. DSP56307 X and Y Data Memory Switching Configuration

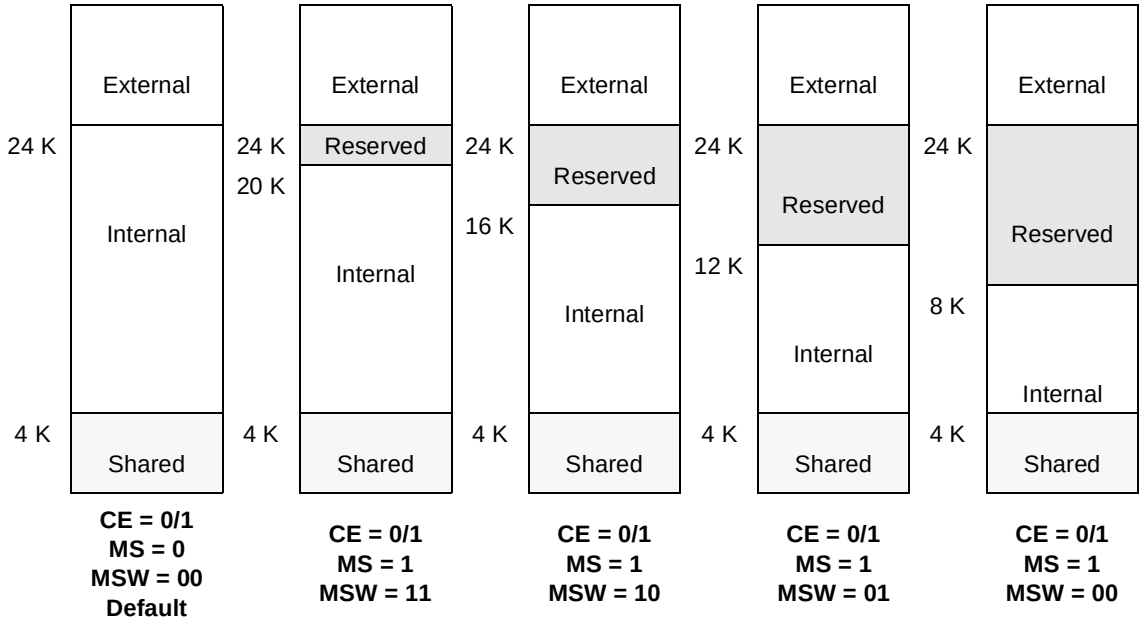
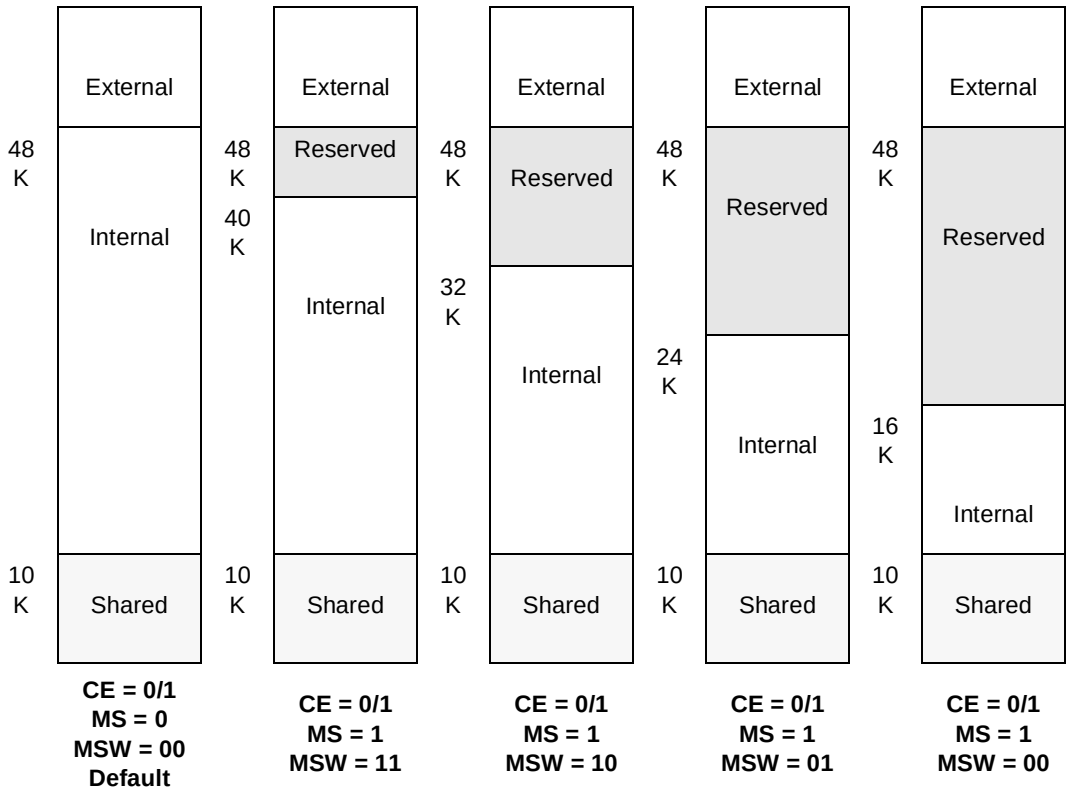


Figure 6. DSP56311 X and Y Data Memory Switching Configurations



Sixteen-bit Compatibility mode also affects the memory configuration for these devices. The following figures show the effect of Sixteen-bit Compatibility mode on the memory map.

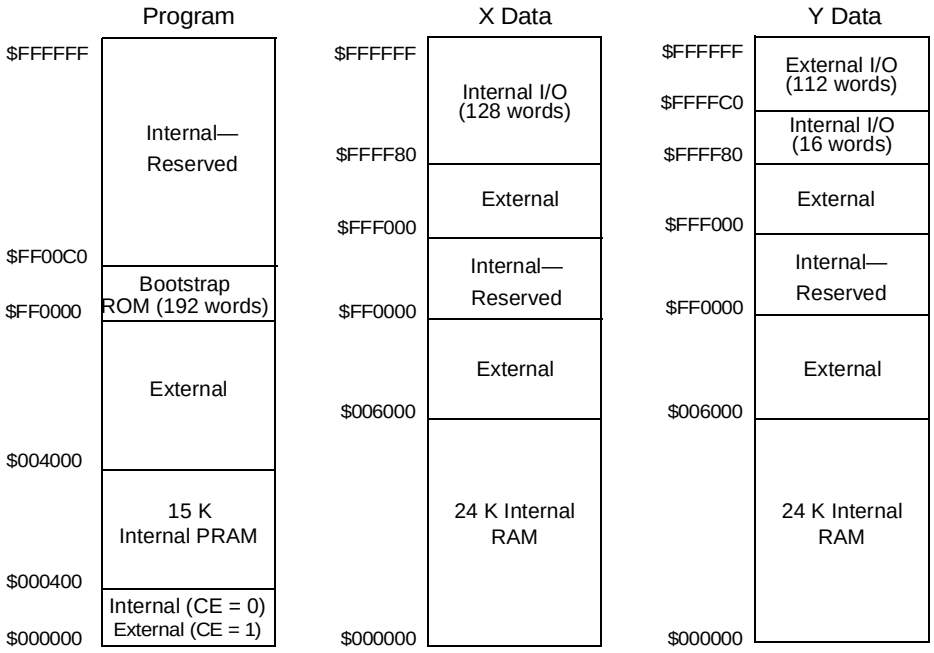


Figure 7. DSP56307 Memory Map—MS = 0 and SC = 0
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Disabled

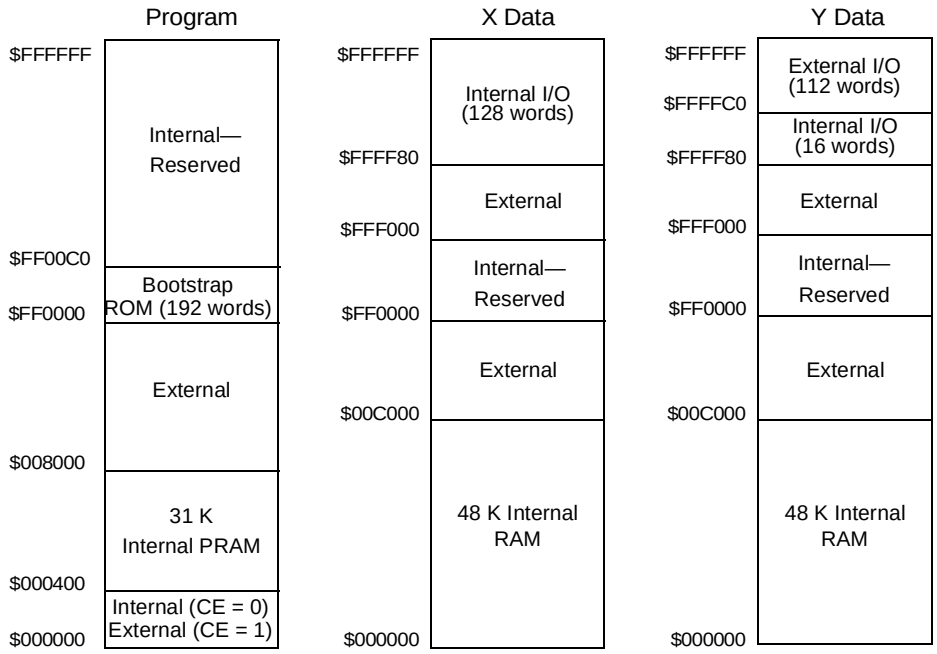


Figure 8. DSP56311 Memory Map—MS = 0 and SC = 0
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Disabled

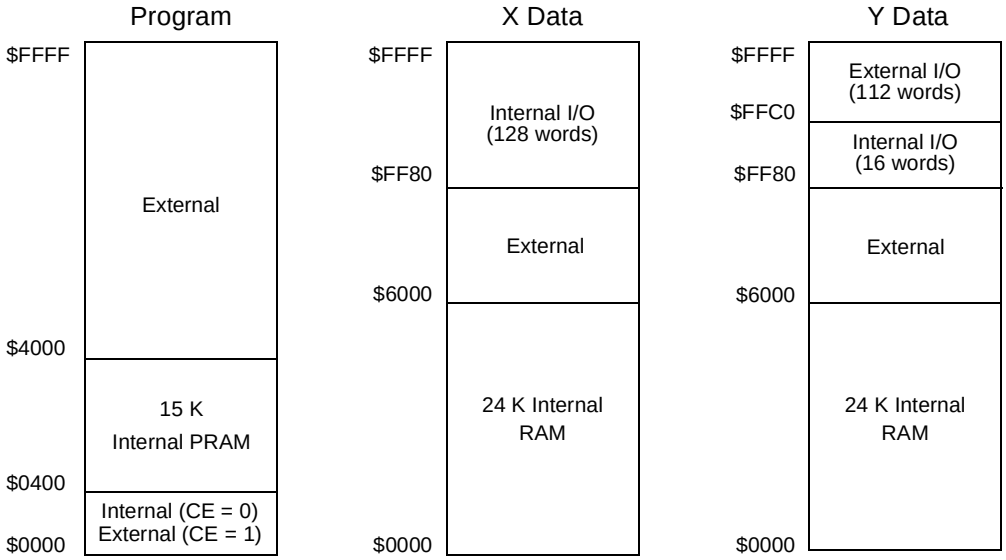


Figure 9. DSP56307 Memory Map—MS = 0 and SC = 1
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Enabled

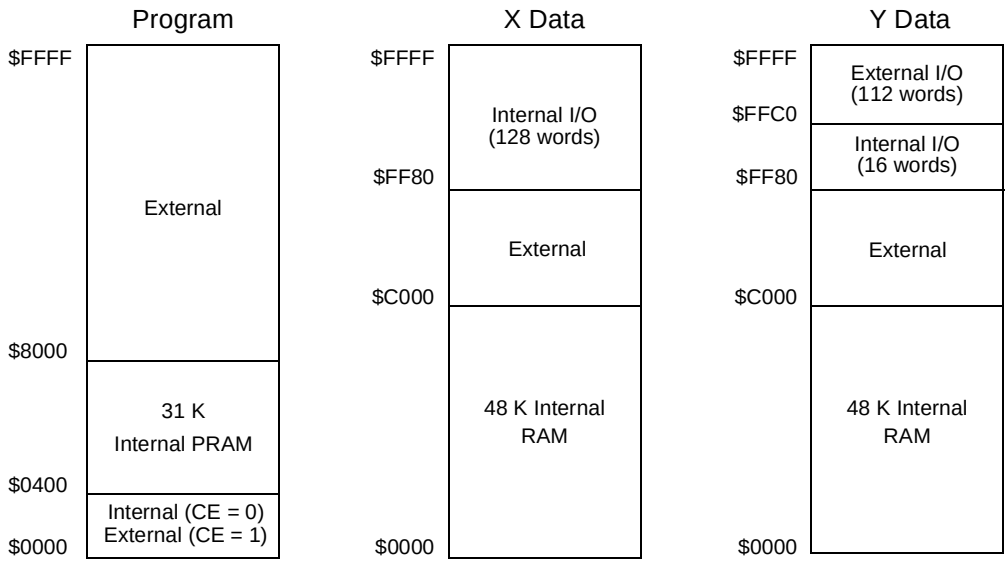


Figure 10. DSP56311 Memory Map—MS = 0 and SC = 1
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Enabled

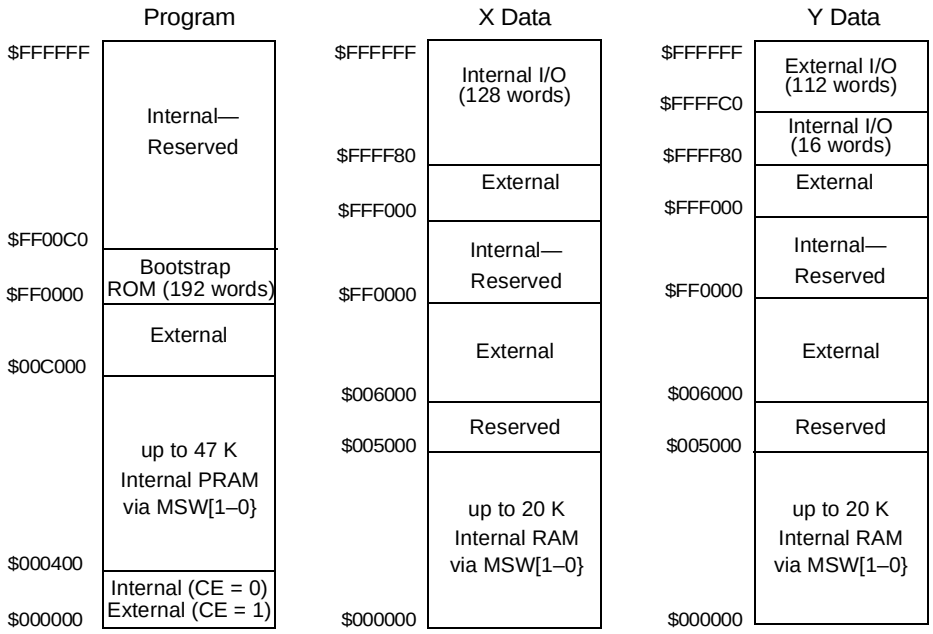


Figure 11. DSP56307 Memory Map—MS = 1 and SC = 0
Memory Switch Mode Enabled, Sixteen-bit Compatibility Mode Disabled

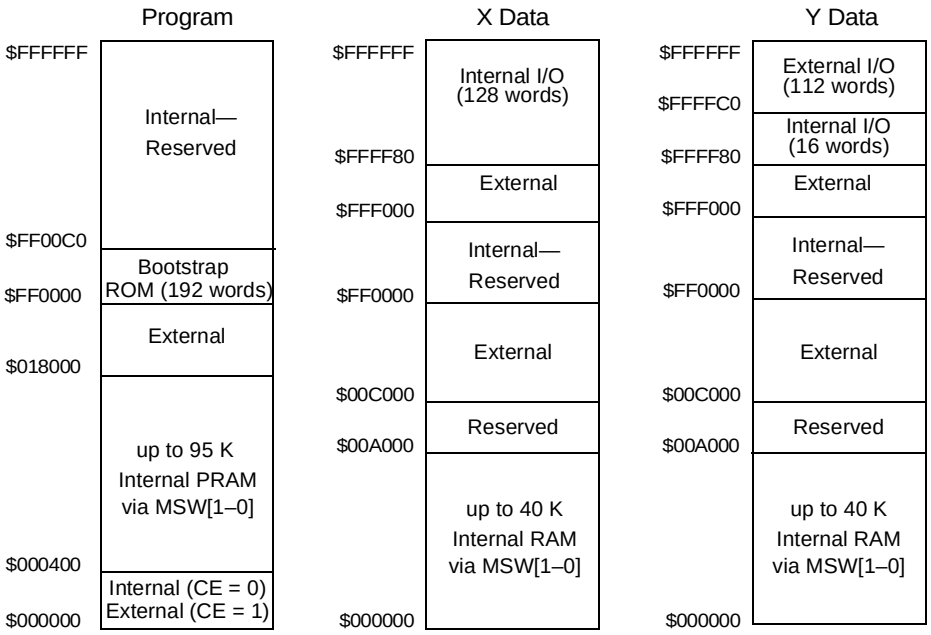


Figure 12. DSP56311 Memory Map—MS = 1 and SC = 0
Memory Switch Mode Enabled, Sixteen-bit Compatibility Mode Disabled

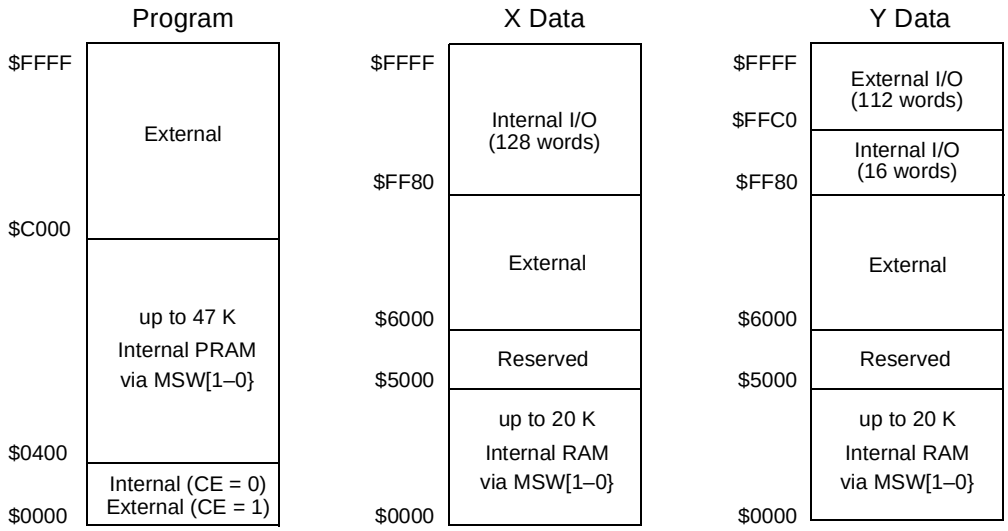


Figure 13. DSP56307 Memory Map—MS = 1 and SC = 1
Memory Switch Enabled, Sixteen-bit Compatibility Mode Enabled

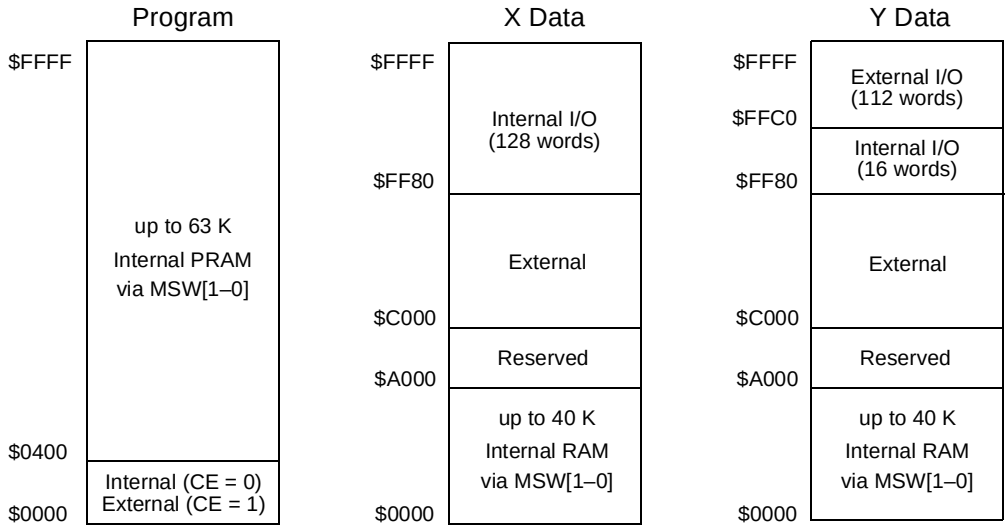


Figure 14. DSP56311 Memory Map—MS = 1 and SC = 1
Memory Switch Enabled, Sixteen-bit Compatibility Mode Enabled

12 Memory Block Size

In the DSP56311, the internal memory block size is 1024 × 24-bit words compared to 256 × 24-bit words in the DSP56307. This change in size affects DMA/core contention and EFCOP/core contention.

In the DSP56307, the internal RAM is divided into 256-word blocks. A situation of contention exists if the core and DMA access the same block of 256 words. If both the core and DMA access the same block, then the core always has priority, and the DMA is delayed until a free slot is available. If the core and DMA access different blocks, they do not interfere with one another; each continues to operate at its maximum speed. Memory block boundaries are located at 256 word addresses.

This same situation applies to the DSP56311, except that contention exists if the core and DMA access the same block of 1024 words. Memory block boundaries are located at 1 K word addresses. To avoid DMA/core contention, DMA and core accesses must address different 1024-word blocks. **Figure 15** shows two examples of core and DMA accesses to different 256-word blocks in the DSP56307 (no contention) and the resulting effect of these same accesses in the DSP56311.

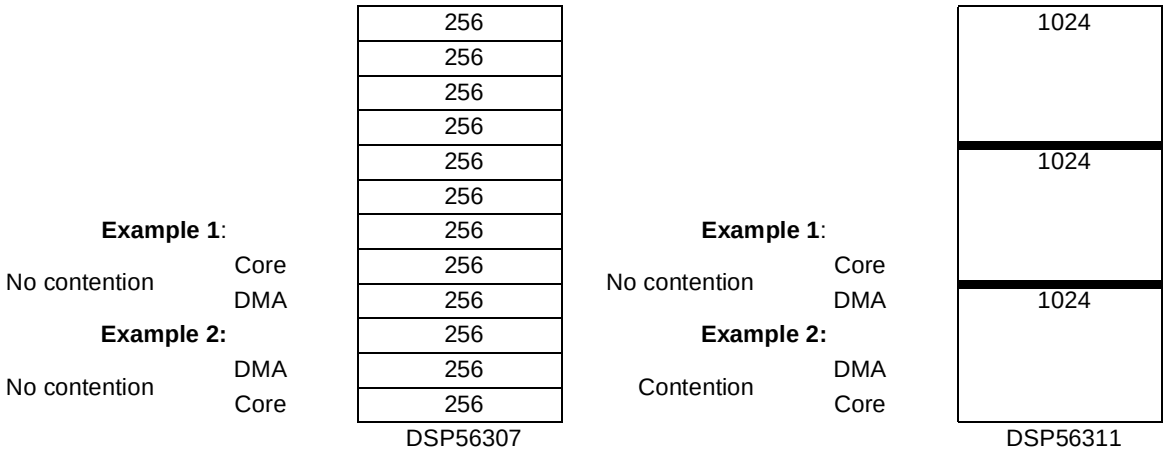


Figure 15. Memory Block Sizes and DMA/Core Accesses

The same change in block size applies to EFCOP/core contention. Unlike Core/DMA contention, EFCOP/core contention may result in faulty data output in the Filter Data Output Register. For the DSP56307, contention occurs if the EFCOP and core attempt to access the same 256 word block. For the DSP56311, contention occurs if the EFCOP and core attempt to access the same 1 K word block. Both the DSP56307 and DSP56311 include the Data/Coefficient Transfer Contention (FCONT) bit in the EFCOP Control Status Register. The FCONT bit allows programmers to detect when EFCOP/core contention occurs.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations not listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GMBH
Technical Information Center
Schatzbogen 7
81829 München, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
+800 2666 8080

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Order No.: EB344
Rev. 4
10/2005