PCA9421

Power management IC for low-power microcontroller applications

Rev. 1.0 — 16 October 2023 Product data sheet

1 General description

The PCA9421 is a highly integrated Power Management IC (PMIC), targeted to provide a full power management solution for low-power microcontroller applications or other similar applications.

The device also integrates two step-down (buck) DC-DC converters which have I^2C programmable output voltage. Both buck regulators have integrated high-side and low-side switches and related control circuitry, to minimize the external component counts; a Pulse-Frequency Modulation (PFM) approach is utilized to achieve better efficiency under light load condition. Other protection features such as overcurrent protection, under-voltage lockout (UVLO), etc., are also provided. By default, the input for these regulators is powered by either VIN or VIN_AUX, whichever is greater.

In addition, two on-chip LDO regulators are provided to power up various voltage rails in the system.

Other features such as Fm+ I^2C-bus interface, chip enable, interrupt signal, etc. are also provided.

The chip is offered in 2.09 mm x 2.09 mm, 5 x 5 bump, 0.4 mm pitch WLCSP package; and 3 mm x 3 mm, 24-pin QFN package.

2 Features and benefits

- Two step-down DC-DC converters
  - Very low quiescent current
  - Programmable output voltage
  - SW1: core buck converter, 0.5 V to 1.5 V output, 25 mV/step, and a fixed 1.8 V, up to 250 mA
  - SW2: system buck converter, 1.5 V to 2.1 V/2.7 V to 3.3 V output, 25 mV/step, up to 500 mA
  - Low-power mode for extra power saving
- Two LDOs
  - Programmable output voltage regulation
  - LDO1: always-on LDO, 1.70 V to 1.90 V output, 25 mV/step, up to 1 mA
  - LDO2: system LDO, 1.5 V to 2.1 V/2.7 V to 3.3 V output, 25 mV/step, up to 250 mA
- 1 MHz I^2C-bus target interface
- -40 °C to +85 °C ambient temperature range
- Offered in 5 x 5 bump-array WLCSP and 24-pin QFN package

3 Applications

- Low power microcontroller application
- Direct powered IoT and consumer

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9421BS	421	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3 x 3 x 0.85 mm	SOT905-1
PCA9421UK	9421	WLCSP25	wafer level chip-scale package, 25 terminals, 0.4 mm pitch, 2.09 mm x 2.09 mm x 0.525 mm body	SOT1401-4

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range (T_{amb})
PCA9421BS	PCA9421BSZ	HVQFN24	REEL 7" Q2 NDP	1400	-40 °C to +85 °C
PCA9421UK	PCA9421UKZ	WLCSP25	REEL 7" Q1 DP CHIPS	3000	-40 °C to +85 °C

5 Simplified block diagram

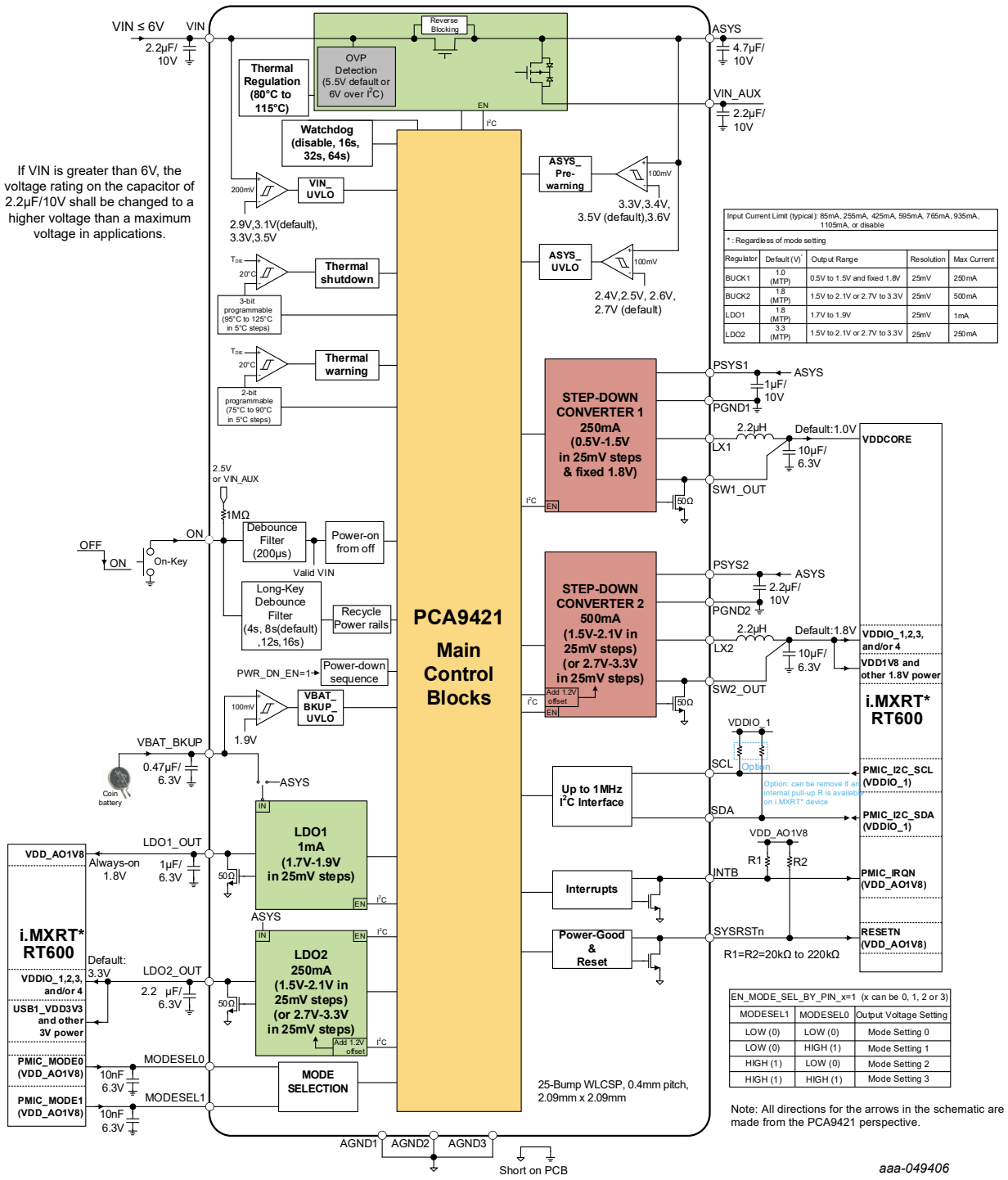


Figure 1. Simplified block diagram

6 Pinning information

6.1 Pinning

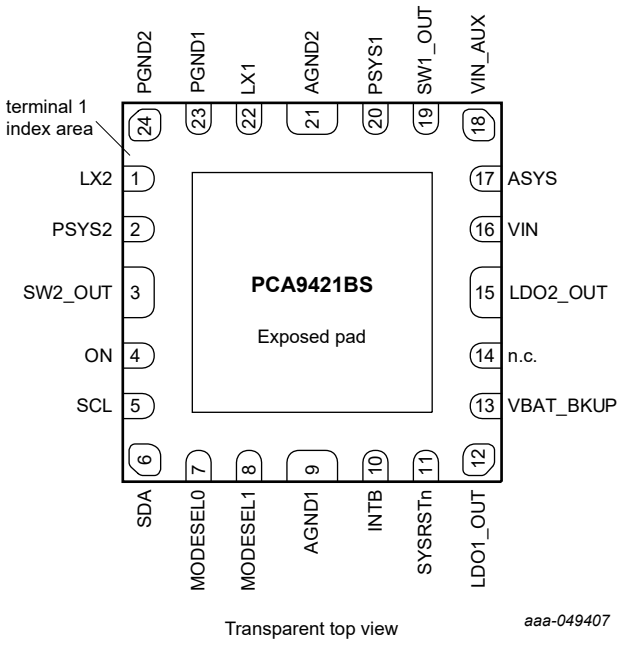


Figure 2. PCA9421BS pinout (HVQFN24) – top view

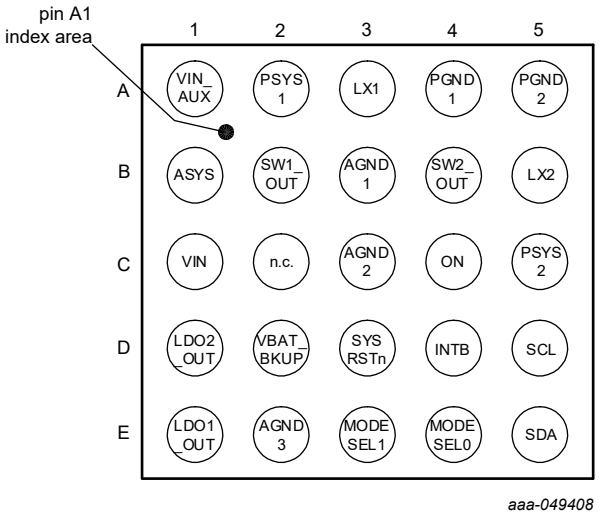


Figure 3. PCA9421UK pinout (WLCSP25) – top view

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Pin Type	Description
	HVQFN24	WLCSP25		
INPUT SUPPLY				
VIN	16	C1	P	Input supply voltage. Bypass with a 2.2 µF/10 V ceramic capacitor. If VIN is greater than 6 V, the voltage rating shall be changed to a higher voltage than the maximum voltage in applications.
ASYS	17	B1	P	Bypass output of VIN and input supply voltage for LDO2; connect with a typical 4.7 µF or 10 µF/10 V decoupling capacitor.
VBAT_BKUP	13	D2	P	Backup battery input voltage. LDO1 is powered by the greater of ASYS or VAT_BKUP. If a back-up battery with a coin cell is not connected, connect the pin to VIN_AUX power domain. Connect with a typical 0.47 µF/6.3 V decoupling capacitor.
VIN_AUX	18	A1	P	Auxiliary input supply voltage. Bypass with a 2.2 µF/10 V ceramic capacitor.
n.c.	14	C2	-	Not connected. Leave the pin open.
BUCK1 STEP_DOWN CONVERTER (SW1)				
PSYS1	20	A2	P	Input supply for SW1. Bypass with a typical 1 µF/10 V ceramic capacitor. Connect to ASYS power domain as short as possible in the system.
LX1	22	A3	P	Switching node for SW1. Connect to a 2.2 µH inductor. If the pin is not used, leave the pin open.
SW1_OUT	19	B2	I	Feedback pin. Bypass with a 10 µF/6.3 V ceramic capacitor. If the pin is not used, tie to PSYS1.
PGND1	23	A4	P	Power ground for buck 1 (SW1). Connect ground nodes of two bypass capacitors for PSYS1 and SW1_OUT as close to PGND1 pin as possible in the system.
BUCK2 STEP_DOWN CONVERTER (SW2)				
PSYS2	2	C5	P	Input supply for SW2. Bypass with a typical 2.2 µF/10 V ceramic capacitor. Connect to ASYS power domain as short as possible in the system.
LX2	1	B5	P	Switching node for SW2. Connect to a 2.2 µH inductor. If the pin is not used, leave the pin open.
SW2_OUT	3	B4	I	Feedback pin. Bypass with a 10 µF/6.3 V ceramic capacitor. If the pin is not used, tie to PSYS2.
PGND2	24	A5	P	Power ground for buck 2 (SW2). Connect ground nodes of two bypass capacitors for PSYS2 and SW2_OUT as close to PGND2 pin as possible in the system.
LOW_DROPOUT REGULATORS (LDO1 and LDO2)				
LDO1_OUT	12	E1	P	LDO1 output. It is always-ON supply. The input supply is a higher voltage between ASYS and VBAT_BKUP. Bypass with a 1 µF/6.3 V ceramic capacitor.

Table 3. Pin description...*continued*

Symbol	Pin		Pin Type	Description
	HVQFN24	WLCSP25		
LDO2_OUT	15	D1	P	LDO2 output. The input supply is ASYS. Bypass with a 2.2 µF/6.3 V ceramic capacitor.
LOGIC INPUTS				
ON	4	C4	I	ON Pin with an internal pullup resistor, 1 MΩ typ, to either 2.5 V or VIN_AUX. Refer to Section 8.6 for more details.
MODESEL0	7	E4	I	Mode selection input pin #1. Place a 10 nF/6.3 V capacitor for noise rejection.
MODESEL1	8	E3	I	Mode selection input pin #2. Place a 10 nF/6.3 V capacitor for noise rejection.
LOGIC OUTPUTS				
INTB	10	D4	O	Interrupt output, Open-drain type. Place a pullup resistor from 20 kΩ to 220 kΩ to a system I/O supply rail.
SYSRSTn	11	D3	O	Reset output for external MCU, Open-drain type. Place a pullup resistor from 20 kΩ to 220 kΩ to a system I/O supply rail.
SERIAL I^2C INTERFACE				
SCL	5	D5	I	I^2C Interface clock pin. Place a pullup resistor between 2.2 kΩ and 10 kΩ to a system I/O supply rail. If the pin is not used, leave the pin open.
SDA	6	E5	I/O	I^2C Interface data pin. Place a pullup resistor between 2.2 kΩ and 10 kΩ to a system I/O supply rail. If the pin is not used, leave the pin open.
DEVICE GROUND				
AGND1	9	B3	P	Analog ground. It shall be connected to system ground through a via. Do not connect AGND1 and AGND2 to PGND1 or PGND2 on the top PCB layer in the system.
AGND2	21	C3	P	
AGND3		E2	P	
	Exposed Pad			Exposed pad. Connect to system ground

P = Power, I = Input, I/O = input/output

7 System configuration diagram

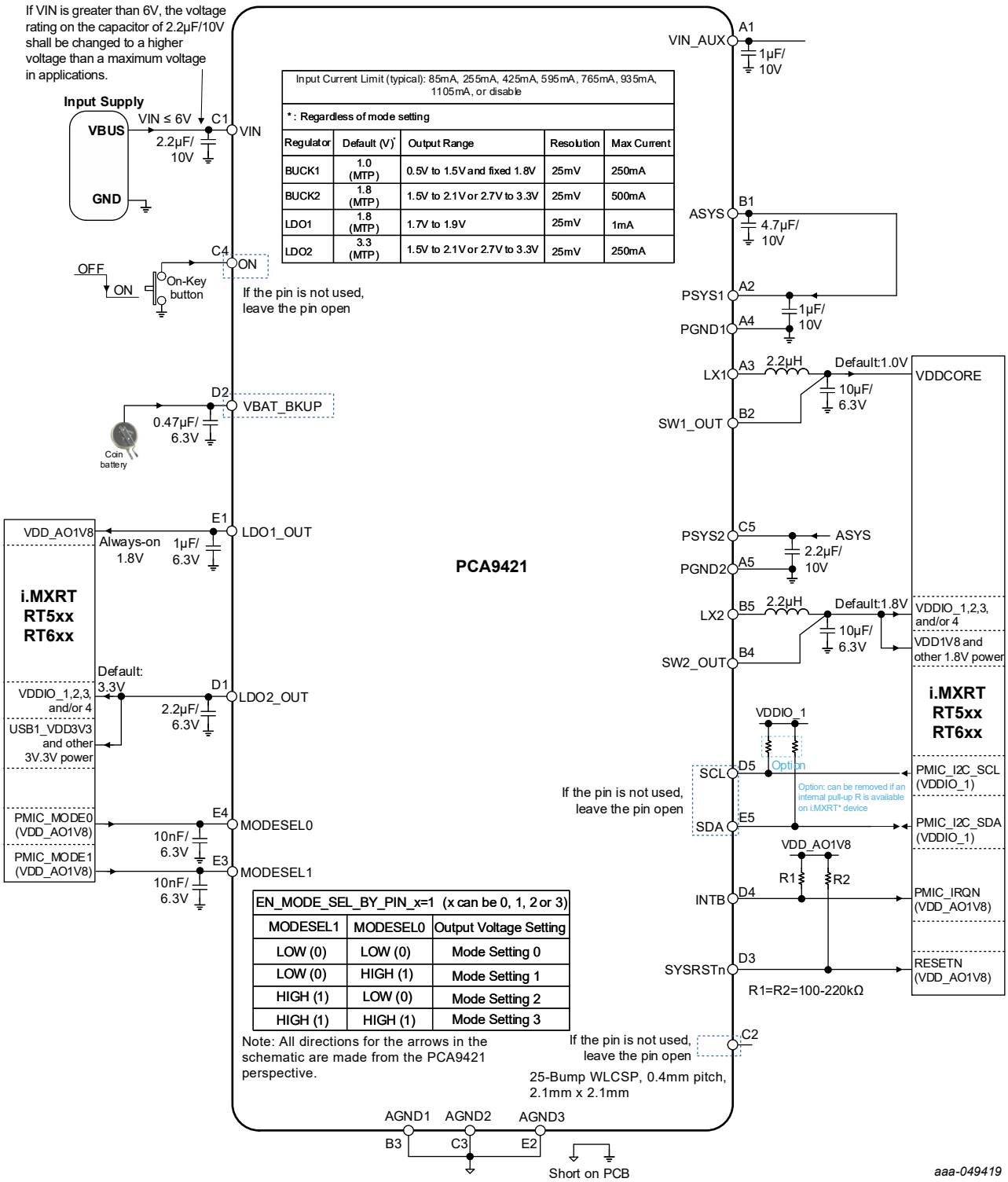


Figure 4. System configuration diagram; i.MXRT series

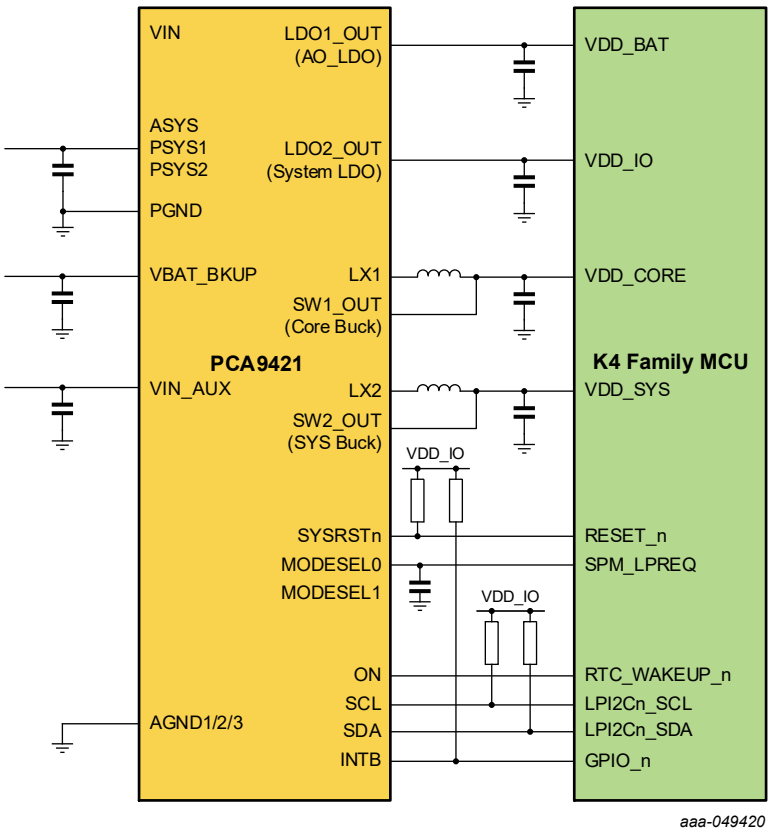


Figure 5. System configuration diagram; K4-family MCU

8 Functional description

8.1 Power control state diagram

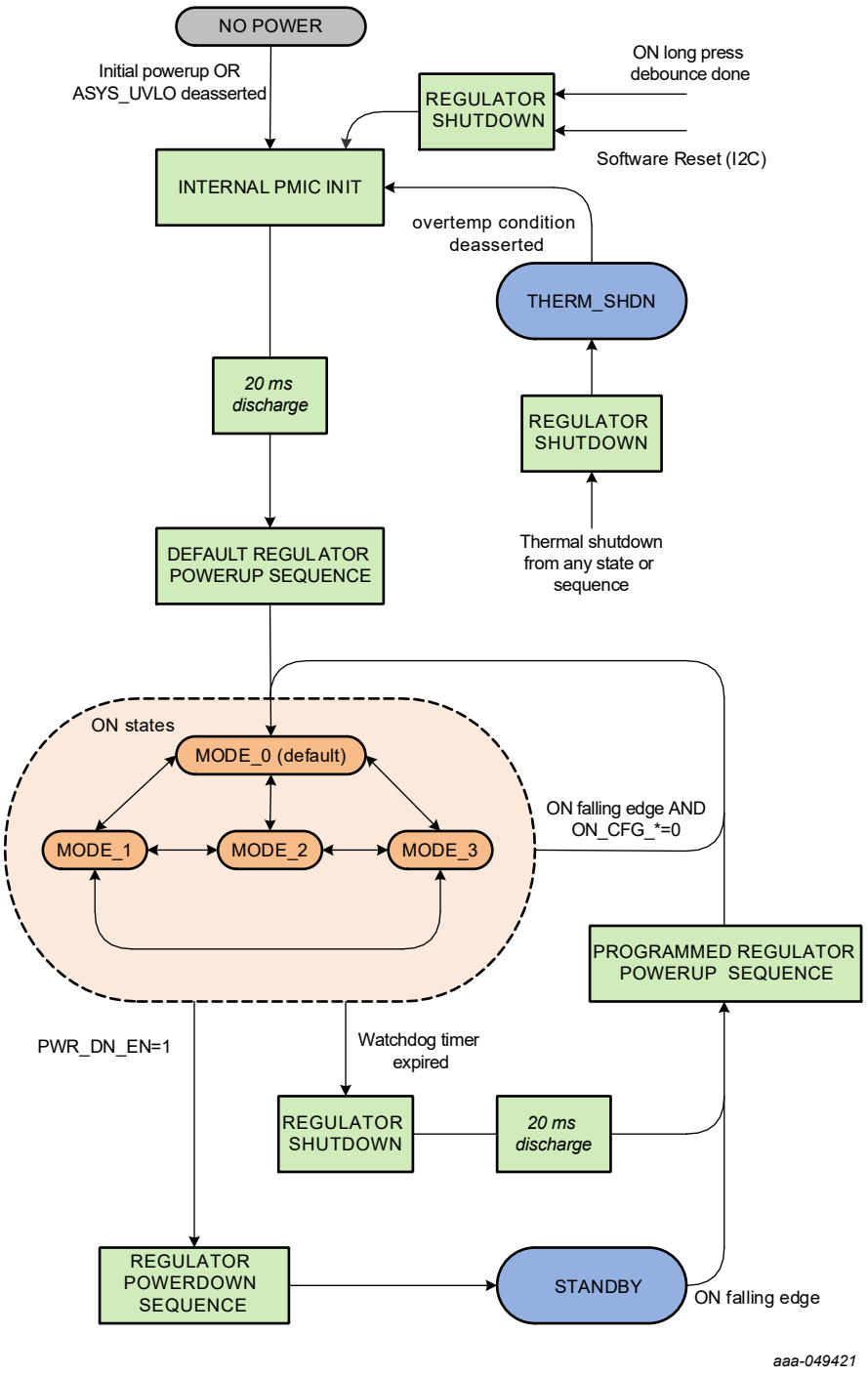


Figure 6. Power control state diagram

8.2 VIN

The VIN pin serves as the input power for ASYS and has the following functions implemented:

- An I^2C undervoltage lockout protection threshold (VIN_UVLO_SEL)
- An I^2C programmable input current limiting threshold (falling, VIN_ILIM_SEL [2:0]) which can be disabled. When the VIN_ILIM threshold is reached, the VIN current clamps at that VIN_ILIM_SEL level. This current limiting only applies to VIN
- 20 V tolerance on VIN pin
- An I^2C programmable overvoltage protection threshold (rising, VIN_OVP_SEL)

8.3 VIN_AUX

VIN_AUX is an auxiliary input power which, depending on ASYS_INPUT_SEL [1:0] register configuration, could be the power source for VSYS. By default VSYS is powered from VIN or VIN_AUX (whichever is greater). In the case of a current limit from VIN as the main power source, when VSYS < VIN_AUX, a current path from VIN_AUX to VSYS is enabled (supplemental mode feature) to provide the needed current as VIN current is limited. There is no internal current limit from VIN_AUX to VSYS.

8.4 ASYS

The ASYS pin serves as the input power pin for PSYS1, PSYS2 and LDO2. Internally by default it's powered by either VIN or VIN_AUX, whichever is greater. The internal ASYS input selection circuit ensures a seamless transition when its input source changes from VIN to VIN_AUX, or vice versa.

Through I^2C register setting selection (ASYS_INPUT_SEL [1:0]), the user also has the option to choose the ASYS input source. However, upon power cycling and/or chip reset, the ASYS input source goes back to the default setting (option 1 below).

SYS_INPUT_SEL [1:0]

1. 2b'00: From either VIN_AUX or VIN, whichever is greater (default setting);
2. 2b'01: From VIN_AUX only;
3. 2b'10: From VIN only;
4. 2b'11: Disconnect from VIN_AUX or VIN (not a normal operation condition, for INTERNAL test purposes only).

An I^2C programmable pre-warning ASYS voltage threshold (ASYS_PRE_WARNING [1:0]) can also be used to indicate when ASYS voltage drops below the ASYS pre-warning threshold voltage, which triggers an interrupt event.

If any peripheral regulators are connected to ASYS node, the ASYS node follows a VIN voltage up to a programmed OVP threshold (either 5.5 V or 6 V) with a various voltage difference depending on a load current.

8.5 VBAT_BKUP (back-up battery input)

Internally, the input power source for LDO1 is provided by either VBAT_BKUP or ASYS, whichever is greater. When a coin cell battery (or similar battery) is used in the system as a backup battery, it can be connected to VBAT_BKUP; thus the LDO1 is powered by either ASYS or the backup battery. When no such backup battery is used, the VBAT_BKUP pin should always be connected to VIN_AUX.

8.6 ON

The ON pin has the following functions implemented:

1. ON pin has internal 1 MΩ pullup resistor to either 2.5 V or VIN_AUX depending on VIN_AUX and VIN voltages:
   - When VIN is present (5 V): If VIN_AUX is less than 3.8 V (typical), ON is pulled up to 2.5 V (typical) and if VIN_AUX is greater than 3.8 V (typical), it is pulled to VIN_AUX.
   - When VIN is not present (0 V): ON pin follows VIN_AUX.

Falling edge (filtered after deglitching time, 200 µs typ), active-LOW signal enables the chip and starts the power-up sequence from STANDBY state. If the device is already in the middle of power-up or power-down sequence, the falling edge applied on the ON pin is ignored by the chip.

1. Long press (duration time, 4 s, 8 s, 12 s or 16 s, is programmable via I^2C, ON_GLT_LONG [1:0]). If the logic LOW signal is applied continuously over a programmed duration, the chip gets reset and recycles all power rails to their default values
2. Also, in mode setting 0, 1, 2, or 3, an I^2C bit “ON_CFG_x“ (x=0, 1, 2, or 3) is reserved; by setting its value to either 0 or 1, the user can configure whether a mode setting switches back to Mode Setting 0 or not, upon a valid falling edge detected from “ON” pin. Refer to ON_CFG_x bit description in the relation registers for more details.
3. The filtered falling edge on the ON pin resets the bit of EN_MODE_SEL_BY_PIN_X to the default value, 0, at 22h register. The status of the ON pin is available in reset monitor register (address 0x71, bit [7]).

8.7 Mode setting

When the MCU operates in different modes such as overdrive run mode or low power mode, it may require the power supply to operate in different settings accordingly (for example, enable/disable of each rail, output voltage of each rail, etc.) to achieve a better performance and efficiency.

On the PCA9421, there are four modes of registers representing Mode Setting 0/1/2/3 to accommodate such requirements from MCU, where Mode Setting A is the default mode setting (i.e., the initial mode setting upon initial power up). Depending on the user’s preference, switching among different mode settings can be controlled by either the external signal (ON pin), external pins (MODESEL0/1) or I^2C.

Within each mode setting, the user can program the follow parameters providing great flexibility to accommodate different MCU operation modes:

1. Enable/disable of the four output voltage rails
2. Voltage setting of the four output voltage rails
3. Watchdog timer setting
4. Mode control selection (EN_MODE_SEL_BY_PIN_x, x=0, 1, 2, or 3)

EN_MODE_SEL_BY_PIN_x = 0: under current mode setting, mode setting switch is controlled by internal I^2C register bits MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored.

EN_MODE_SEL_BY_PIN_x = 1: under current mode setting, mode setting switch is controlled by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^2C register bits MODE0_I2C and MODE1_I2C.

1. Mode setting switches back to Mode Setting A triggered by ON pin falling edge. Refer to register description for “ON_CFG_x” bit for more details.

In the event of switching from one mode setting (initial mode setting) to another mode setting (target mode setting):

1. If one output rail remains enabled in both initial mode setting and target mode setting but with different output voltage in each setting, such voltage transition should happen when the mode setting switch command (from either internal I^2C setting or external signal) is received;

2. If there are output rails which may be enabled or disabled from initial mode setting to target mode setting, then always make sure these rails which change from disabled to enabled take higher priority over rails which change from enabled to disabled, i.e., make sure all the rails change from disabled status to enabled status (reaches 90 % of its target value) first, and then start to disable these rails, changing from enable status to disable status.

8.8 Mode selection by external pins (MODESEL0, MODESEL1)

Up on initial power-up, PCA9421 enters its default setting (Mode Setting 0). While operating under Mode Setting 0, by default the I^2C register bit, EN_MODE_SEL_BY_PIN_0, is set to “0”, and the external signal applied on the MODESEL0 and MODESEL1 pins are ignored. Only when the user sets EN_MODE_SEL_BY_PIN_0 to “1”, can the mode control on the chip be programmed via MODESEL0 and MODESEL1 pin signal settings. The MODESEL0 and MODESEL1 pins are not allowed to change while a mode change is in progress.

When EN_MODE_SEL_BY_PIN_x (x=0, 1, 2, or 3) bits are set to "1", MCU should satisfy the following MODESEL signal conditions:

- No less than 5 µs pulse on each MODESEL signal.
- No more than 0.5 µs delay between MODESEL pins when transit from different modes.

In order to avoid impacting mode transition when there is disturbance in MODESELS pins (EN_MODE_SEL_BY_PIN_x =1), it is proposed to implement one of the following designs:

- Hardware: Adding 10 nF capacitors to remove noise injection on MODESEL pins.

Table 4. Mode selection by external pins (MODESEL0, MODESEL1)

MODESEL1 pin voltage level	MODESEL0 pin voltage level	All Settings from
LOW (0)	LOW (0)	Mode Setting 0
LOW (0)	HIGH (1)	Mode Setting 1
HIGH (1)	LOW (0)	Mode Setting 2
HIGH (1)	HIGH (1)	Mode Setting 3

8.9 SYSRSTn

The SYSRSTn is implemented as an open-drain output signal. It is used as an output of “power-good” indication as well as to reset the microcontroller system.

The SYSRSTn signal is held from HIGH to LOW under one of following conditions:

1. When any of the ***enabled*** voltage rail output voltage drops below 90 % (typ) of its target value.
2. When any of the ***enabled*** voltage rail output voltage goes above 110 % (typ) of its target value

If any of the voltage rail is disabled by the user (by setting the corresponding enable bit in I^2C register in each mode setting, i.e., LDO1_EN_x, LDO2_EN_x, SW1_EN_x, SW2_EN_x), the SYSRSTn signal should NOT assert (stays HIGH) under such scenario.

This also applies during the power-up/power-down sequence events, i.e., during power- up or power-down event, the SYSRSTn signal should assert when any of the enabled rail has not reaches the 90 % to 110 % of its target value. In other words, the SYSRSTn = 0 (LOW) needs to remain at such state until all enabled rails reach 90 % of the target values.

Once the condition that caused the SYSRSTn signal to go LOW is removed, then the SYSRSTn should refresh accordingly.

Meanwhile, during the voltage change on-the-fly, this could be caused by:

1. Mode setting remains the same, but the user chooses to change one or some of the enabled output rail voltage by programming its output voltage I^2C register setting
2. Mode setting changes by setting different values on MODESEL0/MODESEL1 pins or MODE0_I2C/ MODE1_I2C bits, and it causes one or some of the output rail voltage change

In such case, the SYSRSTn signal does NOT assert when any of the ***enabled*** voltage rail output voltage is in the middle of the transition from initial output voltage level to target level.

8.10 Watchdog timer

PCA9421 provides an on-chip watchdog timer, the duration of this watchdog can be programmed via I^2C register setting (WD_TIMER_x [1:0] in each mode configuration registers), or disabled if needed in each mode setting.

Upon initial enable, the watchdog timer starts counting. If the watchdog timer expires before reset, an interrupt signal is issued (WD_TIMER).

When the watchdog timer expires, the following operations are expected:

1. The SYSRSTn signal asserted (HIGH to LOW)
2. All settings for LDO1/LDO2/SW1/SW2 set to Mode 0 settings

The following events reset the watchdog timer:

1. When WD_TIMER_CLR bit is set to 3b'001 at 0Dh register
2. When the device changes the mode settings

8.11 Regulators

There are four regulators on PCA9421, which include two buck regulators and two LDOs. Table 5 shows the outline for each regulator:

Table 5. Regulator summary

Regulator name	Output regulation voltage range	Adjustable resolution	Max output current
SW1 (Core Buck)	0.5 V to 1.5 V and a fixed 1.8 V	25 mV/step	Up to 250 mA
SW2 (System Buck)	1.5 V to 2.1 V or 2.7 V to 3.3 V	25 mV/step	Up to 500 mA
LDO1 (Always-on LDO)	1.7 V to 1.9 V	25 mV/step	Up to 1 mA
LDO2 (System LDO)	1.5 V to 2.1 V or 2.7 V to 3.3 V	25 mV/step	Up to 250 mA

For each rail, its output target voltage can be set independently in mode setting 0, 1, 2 or 3. User can also choose to switch among any of the mode settings.

8.11.1 Enable/disable and active discharge

Enable/disable: Each rail can be enabled/disabled via I^2C register setting independently in each mode setting.

Active discharge: Additionally, there is an active discharge resistor on each rail, and the user can choose to enable/disable such feature through I^2C register setting, so that when the output rail is disabled, it can quickly discharge the output voltage to ground. In addition, the active discharge is also enabled during voltage step down. This can be disabled by MTP bit.

If the active discharge bleeding resistor is enabled AND there is a change to the output voltage of the buck regulators to a lower value (i.e. from 0.9 V to 0.75 V) there could be a small voltage peak of 5 % higher than the initial voltage (for 10 µs) during the transition. If this behavior is not desired, the bleeding resistor can be

disabled (nEN_SW1_BLEED = 1 or nEN_SW2_BLEED = 1) but with the effect of a potentially longer transition to the new voltage of the buck regulator output

8.11.2 Power-good indication

There is an output voltage comparator for each rail, comparing the actual output voltage against 90 % and 110 % of its target value; when the actual voltage is between 90 % and 110 % of its target value, the read-only related bits in I^2C register, Regulator Status_1 (address: 20h) are updated accordingly to report the output voltage status (Power-good Indication). These comparators can be enabled/disabled by setting I^2C register bit, PG_EN. A corresponding interrupt is triggered if unmasked. During steady state, only 90 % threshold is monitored.

The power-good indication is shown as “not good”, and refreshes upon the completion of any of the following events:

1. During the power-up sequence stage
2. During power-down sequence stage
3. During the on-the-fly change of output voltage

8.11.3 Power-up/down sequence and on-the-fly voltage change

Power-up sequence

The device initiates the default power-up sequence in three different conditions.

Condition 1) The device is off with no any power supply (No valid VIN or VIN_AUX). In this condition, two signals below are able to start the default power-up sequence.

- A valid VIN supply on VIN pin
- A voltage on ASYS higher than ASYS_UVLO, a 2.8 V typical

Condition 2) The device stays off by enabling PWR_DN_EN bit setting to 1 with VIN_AUX ≥ 2.8 V attached. In this condition, only one signal is able to start the default power-up sequence.

- A falling edge on ON key over a 200 µs

Condition 3) The device stays at VIN OVP condition with no any valid supply attached at VIN_AUX. In result, all enabled power rails have been off. The following condition re-initiates the power-up sequence.

- The VIN goes below its VIN OVP hysteresis (typ 100 mV)

The power-up sequence by ON key = LOW over the debounce time is described as shown in Figure 7.

For the power-up sequence, the chip can set the default sequence per the customer requirement at factory setting (i.e. MTP option), from one of the 64 options. Once the chip enters the power-down stage, the power-down sequence is implemented as the reverse of the power-up sequence (i.e., first up, last down). SYSRSTn goes LOW as soon as the power-down sequence is asserted as shown in Figure 7.

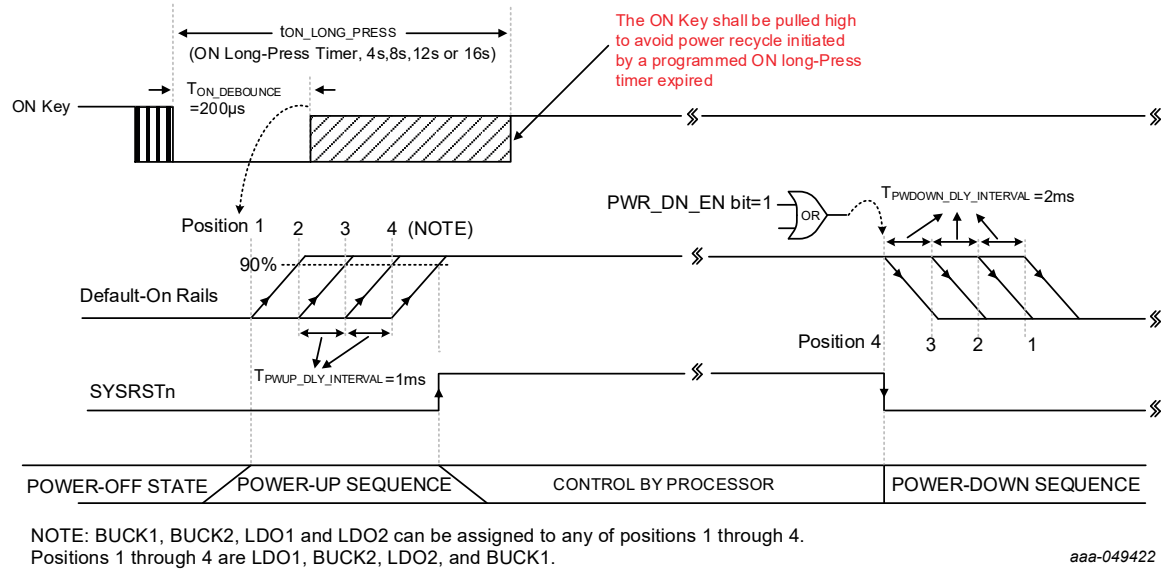


Figure 7. Power-up/down sequence

On-the-fly output voltage change sequence

On-the-fly output voltage change is defined as the following: for any output rail, its output voltage changes from one level (initial level) to another level (target level). Note this assumes the output rail is always enabled before and after the on-the-fly change transition. It does not include the case when any output rail is changed from disabled state to enabled state, or vice versa.

If a user prefers to change any rail voltage on-the-fly, depending on the scenarios listed below, the chip behavior is described as follows:

1. While the chip remains in its current operation mode, and the user programs the output voltage setting I^2C register value or enables/disables any or some of output voltage rail(s), the chip simply executes the I^2C command
2. While the user chooses to switch modes, i.e. change mode between any of the two mode settings among Mode 0/1/2/3, and if this involves on-the-fly voltage change for one or some output rails, such change should occur simultaneously when the chip switches from initial mode to the target mode.

CAUTION: The user should not send an I^2C command related to changing the setting of the output rails during the power up/down or mode setting change process.

8.11.4 BUCK1 (SW1, core buck regulator)

The SW1 supplies the core power.

Its output voltage can be programmed via I^2C from 0.5 V to 1.5 V at 25 mV step and a fixed 1.8 V, which is capable of providing up to 250 mA loading. The application circuit uses typical 2.2 µH inductor and 10 µF/6.3 V output capacitor.

This regulator implements an output current limit protection. When the inductor peak current reaches $I_{LIM(SW1)}$ it enters a cyclic mechanism where the inductor current ramps down until it reaches 0 A. The regulator increases inductor current and retries start up. This cyclic current limiting stops once the overcurrent condition is removed. The output voltage collapses during the cyclic current limiting.

8.11.5 BUCK2 (SW2, system buck regulator)

The SW2 output voltage can be programmed via I^2C register from 1.5 V to 2.1 V, or from 2.7 V to 3.3 V in both at 25 mV/step and is capable of providing up to 500 mA loading. The application circuit uses a 2.2 µH inductor and 10 µF output capacitor.

In SW2, a pass-through mode is implemented. When its input (ASYS) is close to the output voltage (within typical 200 mV), the SW2 enters the pass-through mode operation; the high-side switch is fully turned on and the low-side switch is turned off, and the output voltage can be calculated as input voltage – (RDSON*I_{LOAD}), where RDSON is the on-resistance of the high-side switch, and the I_{LOAD} refers to the load current. When the input voltage rises again, so that the voltage different between input and output crosses the typical 250 mV threshold, the SW2 exits the pass-through mode and re- enters the normal switching mode operation.

This regulator implements an output current limit protection. When the inductor peak current reaches $I_{LIM(SW2)}$ it enters a cyclic mechanism where the inductor current ramps down until it reaches 0 A. The regulator increases inductor current and retries start up. This cyclic current limiting stops once the overcurrent condition is removed. The output voltage collapses during the cyclic current limiting.

While SW2 operates in pass-through mode, protection features such as over-current protection are also implemented as well.

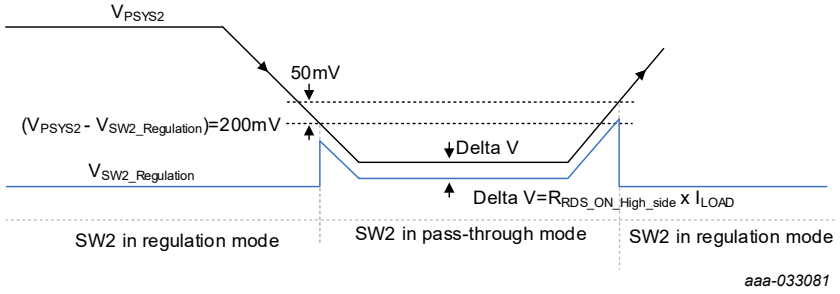


Figure 8. Pass-Through mode of BUCK2 (SW2)

8.11.6 LDO1 (always-on LDO)

The LDO1 (Always-on LDO) output can be programmed from 1.7 V to 1.9 V at 25 mV step, depending on the system requirements (selectable through I^2C register). Typically, a 1 µF/6.3 V MLCC output capacitor providing at least 1 mA loading capability is needed.

LDO1 operates based on the principle of hysteretic on/off regulation. The LDO1 output voltage is generated from a frequent activation/deactivation of the output stage connecting VIN_AUX to the LDO1 output depending on the programmed output voltage for LDO1. The ripple frequency and amplitude greatly depends on the load current and external capacitance. The greater the load current, the higher the on/off activation of this output stage to ensure LDO1 stays within the defined output voltage accuracy specified in the electrical specification section. LDO1 is powered by the greater of ASYS or VBAT_BKUP.

SW_RST event will not shut down LDO1, but sets LDO1 to default value. Watchdog Reset will not shut down LDO1, but changes LDO1 to Mode 0 setting. Hardware Reset (ON Long Press) shuts down LDO1 and recycles power up to default output voltage.

This regulator implements an output current limit protection. As output current is limited by $I_{OUT\_LDO1\_LIMIT}$, the output voltage collapses if the load current is higher than $I_{OUT\_LDO1\_LIMIT}$. Once the overcurrent is removed the regulator restarts automatically.

8.11.7 LDO2 (system LDO)

The LDO2 (system LDO) output can be programmed via the I^2C register from 1.5 V to 2.1 V, or 2.7 V to 3.3 V at 25 mV/step. Typically, a 2.2 µF/6.3 V MLCC output capacitor providing at least 250 mA loading current is needed.

This regulator implements an output current limit protection. As output current is limited by $I_{OUT\_LDO2\_LIMIT}$, the output voltage collapses if the load current is higher than $I_{OUT\_LDO2\_LIMIT}$. Once the overcurrent is removed the regulator restarts automatically.

8.12 Hardware and software reset

Please refer to description for ON pin for the hardware reset function by a long time ON key pressed. The "software reset" is achieved by setting “1” to SW_RST bit in I^2C register. If the user writes a “1” to this bit, it resets all other I^2C register bits to their default setting; this bit is cleared and reset back to “0” as well.

8.13 Device level protection features

The device contains several protection features at both the complete IC level and have a reaction at each of the functional blocks (DC-DC converters, LDOs, VIN, VSYS). There are additional protection mechanisms at the functional block level, but those are already documented on its respective functional description section.

Table 6. Device level protection features

Condition	Triggering point	Protection reaction			
		Overall Device state	DC-DC converters	LDOs	Register contents
VIN undervoltage	VIN < VIN_UVLO	Operational	Remain operational although might deliver a reduced output voltage (due to low VIN)	Remain operational although might deliver a reduced output voltage (due to low VIN)	Maintained. Interrupt triggered, status reported.
VIN overcurrent (ILIM)	VIN current is > VIN_ILIM	Limit input current to VIN_ILIM setting	Remain operational	Remain operational	Maintained unless reset happened; Interrupt and status reported.
ASYS undervoltage	ASYS < ASYS_UVLO	RESET	Turned off, restarted in initial state when condition goes away	Turned off, restarted in initial state when condition goes away	Reset to their default value
IC overtemperature	Chip temperature > THM_REG	RESET	Turned off, restarted in initial state when condition goes away	Turned off , restarted in initial state when condition goes away	Reset to their default value. Status available in register 0x71.
Watchdog timer expiration	Watchdog counter > WD_Timer_0 setting	Operational	Set to mode 0	Set to mode 0	Maintained. Status available in register 0x71.

9 I^2C-bus interface and register

The PCA9421 implements an I^2C-bus target interface to communicate with the host system. The interface supports Fast Mode plus Fm+ with up to 1 Mbit/s. A detailed description of the I^2C-bus specification is given in UM10204, Rev. 06, 4 April 2014 ,“ I^2C-bus specification and user manual”.

Features such as clock-stretching and 10-bit target address are not supported; general call is supported by default but can be disabled via metal option. Auto increment with address wrap-around is supported as well.

9.1 I^2C target address

Following a START condition, the bus controller must send the target address followed by a read or write operation. The target address of the PCA9421 is shown below:

Table 7. I^2C target address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	0	0	1	0/1
Fixed	Fixed	Fixed	MTP option	Fixed	Fixed	Fixed	R/W

Bit 4 should be reserved as MTP option, with its default value set as “0” but can be trimmed to “1” when needed.

9.2 General call and device ID addresses

The device implements two different addresses for general call and device ID.

9.3 Register type

There are four register types used on the device:

- Read and Write (R/W)
- Read Only (R)
- Write Only (W)
- Write and Clear (W/C)

For Write and Clear (W/C), a write to a register with a bit-mask specifies which interrupts to clear.

For example, if the status register shows 8’b0000_1001 as an interrupt status (i.e. interrupt [0] and interrupt [3] are both set), user may write 8’b0000_1000, meaning the intent is to only clear interrupt [3] (but interrupt [0] should NOT be “cleared”). If the intent is to clear both interrupts, then the user could write back 8’b0000_1001.

9.4 Register map

Table 8. Register map

Address (Hex)	Register Name	Description	Type	Reset Value (Binary)
System Control Registers				
00	Device Information, DEV_INFO	Device ID, revision	R	0000 0001
01	Top Level Interrupt Status, TOP_INT	Top level interrupt event status	R/C	0000 0000
02	Sub Level Interrupt_0, SUB_INT0	Sub-level interrupt indication_0	W/C	0000 0000
03	Sub Level Interrupt_0 Mask, SUB_INT0_MASK	Sub-level interrupt mask for SUB_INT0	R/W	0011 1111
04	Sub Level Interrupt_1, SUB_INT1	Sub-level interrupt indication_1	W/C	0000 0000
05	Sub Level Interrupt_1 Mask, SUB_INT1_MASK	Sub-level interrupt mask for SUB_INT1	R/W	0111 1111
06	Sub Level Interrupt_2, SUB_INT2	Sub-level interrupt indication_2	W/C	0000 0000
07	Sub Level Interrupt_2 Mask, SUB_INT2_MASK	Sub-level interrupt mask for SUB_INT2	R/W	1111 1111
08	RSVD	Reserved	R/W	0000 0000
09	Top Level Control_0, TOP_CNTL0	Top level system control_0	R/W	0100 0001
0A	Top Level Control_1, TOP_CNTL1	Top level system control_1	R/W	1000 1001
0B	Top Level Control_2, TOP_CNTL2	Top level system control_2	R/W	1100 1110
0C	Top Level Control_3, TOP_CNTL3	Top level system control_3	R/W	0000 0001
0D	Top Level Control_4, TOP_CNTL4	Top level system control_4	W	0000 0000

Table 8. Register map*...continued*

Address (Hex)	Register Name	Description	Type	Reset Value (Binary)
0E – 17	RSVD	Reserved		
18	VIN_PWR Status_0, PWR_STATUS_0	VIN_PWR status indication_0	R	0001 0000
19	VIN_PWR Status_1, PWR_STATUS_1	VIN_PWR status indication_1	R	0000 0000
1A – 1F	RSVD	Reserved		
Regulator Control				
20	Regulator Status, REG_STATUS	Regulators status indication	R	0000 0000
21	Active Discharge Control, ACT_DISCHARGE_CNTL_1	Active Discharge control register	R/W	0000 0000
22	Mode Configuration Mode Setting 0_0, MODECFG_0_0	Mode configuration settings for Mode 0_0	R/W	0001 0100
23	Mode Configuration Mode Setting 0_1, MODECFG_0_1	Mode configuration settings for Mode 0_1	R/W	0000 1100
24	Mode Configuration Mode Setting 0_2, MODECFG_0_2	Mode configuration settings for Mode 0_2	R/W	0100 1111
25	Mode Configuration Mode Setting 0_3, MODECFG_0_3	Mode configuration settings for Mode 0_3	R/W	0011 1001
26	Mode Configuration Mode Setting 1_0, MODECFG_1_0	Mode configuration settings for Mode 1_0	R/W	0001 1100
27	Mode Configuration Mode Setting 1_1, MODECFG_1_1	Mode configuration settings for Mode 1_1	R/W	0100 1100
28	Mode Configuration Mode Setting 1_2, MODECFG_1_2	Mode configuration settings for Mode 1_2	R/W	0100 1111
29	Mode Configuration Mode Setting 1_3, MODECFG_1_3	Mode configuration settings for Mode 1_3	R/W	0000 1100
2A	Mode Configuration Mode Setting 2_0, MODECFG_2_0	Mode configuration settings for Mode 2_0	R/W	0001 1100
2B	Mode Configuration Mode Setting 2_1, MODECFG_2_1	Mode configuration settings for Mode 2_1	R/W	0100 1100
2C	Mode Configuration Mode Setting 2_2, MODECFG_2_2	Mode configuration settings for Mode 2_2	R/W	0100 1111
2D	Mode Configuration Mode Setting 2_3, MODECFG_2_3	Mode configuration settings for Mode 2_3	R/W	0000 1100
2E	Mode Configuration Mode Setting 3_0, MODECFG_3_0	Mode configuration settings for Mode 3_0	R/W	0001 1100
2F	Mode Configuration Mode Setting 3_1, MODECFG_3_1	Mode configuration settings for Mode 3_1	R/W	0100 1100
30	Mode Configuration Mode Setting 3_2, MODECFG_3_2	Mode configuration settings for Mode 3_2	R/W	0100 1111
31	Mode Configuration Mode Setting 3_3, MODECFG_3_3	Mode configuration settings for Mode 3_3	R/W	0000 1100
71	Reset monitor	Reset reason monitor	R RO R/W	1000 0000

9.5 Register description

9.5.1 Device information (DEV_INFO, address 00h)

The device identification code stores a unique identifier for each version and/or revision of device, so that the connected MCU recognizes it automatically.

This is a READ ONLY register.

Table 9. DEV_INFO register bit description

Bit	Symbol	Default value	Type	Function
7	DEV_ID [4]	0	R	Device ID
6	DEV_ID [3]	0	R	
5	DEV_ID [2]	0	R	
4	DEV_ID [1]	0	R	
3	DEV_ID [0]	0	R	
2	DEV_REV [2]	0	R	Device revision
1	DEV_REV [1]	0	R	
0	DEV_REV [0]	1	R	

9.5.2 Top level interrupt status (TOP_INT, address 01h)

The top-level interrupt register contains flags indicating various top level interrupt events as indicated below. An event is latched and only its first occurrence triggers the interrupt signal INTB (if it is not being masked). Reoccurring events do not change the flag's status or trigger an additional interrupt. If multiple interrupt events happen, its corresponding interrupt bits in the related registers are “triggered”, however, the INTB signal is only triggered upon the first interrupt event.

The interrupt event reporting on the device is structured in a two-layer configuration. The interrupt events are grouped as (1) system level; (2) buck regulator block; (3) LDO block. When any interrupt event is triggered, based on which mode it falls into, the related bit for that mode in TOP_INT flags “1”. Any of the related bits in TOP_INT only change back to 0 when all the interrupt events in its affiliated mode are cleared.

This is READ Only register.

Table 10. TOP_INT register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R	Reserved bit
6	RSVD	0	R	Reserved bit
5	RSVD	0	R	Reserved bit
4	RSVD	0	R	Reserved bit
3	SYS_INT	0	R	System level interrupt event trigger indication from events reflected on Sub level interrupt_0 register. 0: no system level interrupt event triggered 1: system level interrupt event triggered
2	VIN_INT	0	R	VIN_INT interrupt event trigger indication 0: no VIN_AUX_OK or VIN_ILIM interrupt event triggered 1: VIN_AUX_OK or VIN_ILIM interrupt event triggered

Table 10. TOP_INT register bit description*...continued*

Bit	Symbol	Default value	Type	Function
1	SW_INT	0	R	Buck regulator blocks (SW1, SW2) interrupt event trigger indication 0: no interrupt event on SW1 and/or SW2 blocks triggered 1: interrupt event on SW1 and/or SW2 blocks triggered
0	LDO_INT	0	R	LDO block (LDO1, LDO2) interrupt event trigger indication 0: no interrupt event on LDO1 and/or LDO2 blocks triggered 1: interrupt event on LDO1 and/or LDO2 blocks triggered

9.5.3 Sub level interrupt_0 (SUB_INT0, address 02h)

The sub-level interrupt register contains flags indicating the second-tier interrupt event. For this register, it contains system level related interrupt events. Any of the interrupt sources of this register trigger the SYS_INT bit on the TOP_INT register as long as they are unmasked on the Sub_INT0_Mask register.

This is WRITE AND CLEAR register.

Table 11. Sub_INT0 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	W/C	Reserved bit
6	RSVD	0	W/C	Reserved bit
5	ON_PUSH_INT	0	W/C	ON falling edge longer than 5 ms happened
4	TEMP_ PREWARNING	0	W/C	Die temperature pre-warning interrupt 1: die temp ≥ TWARNING 0: die temp < TWARNING. TWARNING threshold is configured by T_ WARNING [1:0]
3	THEM_SHDN	0	W/C	Thermal shutdown interrupt 0: thermal shutdown is not triggered 1: die temp ≥ TSHDN (set in THEM_SHDN [2:0], thermal shutdown is triggered
2	ASYS_ PREWARNING	0	W/C	ASYS Pre-Warning Voltage Interrupt 0: ASYS voltage does NOT fall below the threshold set in ASYS_ PREWARNING [1:0] 1: ASYS voltage falls below the threshold set in ASYS_PREWARNING [1:0]
1	WD_TIMER	0	W/C	Watchdog Timer Expiration Interrupt 0: The watchdog timer expiration has not happened since the last time this bit was cleared. 1: The watchdog timer expiration has happened since the last time this bit was cleared.
0	IN_PWR	0	W/C	Input Voltage Interrupt 0: The IN_PWR bit has not changed since the last time this bit was cleared. 1: The IN_PWR bit has changed since the last time this bit was cleared.

9.5.4 Sub level interrupt_0 mask (Sub_INT0_Mask, address 03h)

This is a READ AND WRITE register.

Table 12. Sub_INT0_Mask bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5	ON_PUSH_INT_MASK	1	R/W	ON Key falling interrupt mask bit 0: Not Masked 1: Masked
4	TEMP_PREWARNING_MASK	1	R/W	Die temp pre-warning interrupt mask bit 0: Not Masked 1: Masked
3	THEM_SHDN_MASK	1	R/W	Thermal shutdown interrupt mask bit 0: Not Masked 1: Masked
2	ASYS_PREWARNING_MASK	1	R/W	ASYS Pre-Warning Voltage Interrupt Mask bit 0: Not Masked 1: Masked
1	WD_TIMER_MASK	1	R/W	Watchdog Timer Expiration Interrupt Mask bit 0: Not Masked 1: Masked
0	IN_PWR_MASK	1	R/W	Input Voltage Interrupt Mask bit 0: Not Masked 1: Masked

9.5.5 Sub level interrupt_1 (Sub_INT1, address 04h)

The sub-level interrupt register contains flags indicating the second-tier interrupt event. For this register, it contains VIN and VIN_AUX related interrupt events. Any of the interrupt sources of this register trigger the VIN_INT bit on the TOP_INT register as long as they are unmasked on the Sub_INT1_Mask register.

This is WRITE AND CLEAR register.

Table 13. Sub_INT1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	W/C	Reserved bit
6	RSVD	0	W/C	Reserved bit
5	VIN_ILIM	0	W/C	Input Current Limit Interrupt 0: no Input current limit has been triggered since the last time this bit is cleared; 1: input current limit event is triggered since last time this bit is cleared.
4	RSVD	0	W/C	Reserved bit
3	RSVD	0	W/C	Reserved bit
2	RSVD	0	W/C	Reserved bit
1	VIN_AUX_OK	0	W/C	VIN_AUX Interrupt 0: The VIN_AUX_OK bit has not changed since the last time this bit was cleared.

Table 13. Sub_INT1 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				1: The VIN_AUX_OK bit has changed since the last time this bit was cleared.
0	RSVD	0	W/C	Reserved bit

9.5.6 Sub level interrupt_1 mask (Sub_INT1_Mask, address 05h)

This is a READ AND WRITE register.

Table 14. Sub_INT1_Mask register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	1	R/W	Reserved bit
5	VIN_ILIM_MASK	1	R/W	Input Current Limit Interrupt Mask bit 0: Not Masked 1: Masked
4	RSVD	1	R/W	Reserved bit
3	RSVD	1	R/W	Reserved bit
2	RSVD	1	R/W	Reserved bit
1	RSVD	1	R/W	Reserved bit
0	RSVD	1	R/W	Reserved bit

9.5.7 Sub level interrupt_2 (Sub_INT2, address 06h)

The sub-level interrupt register contains flags indicating the second-tier interrupt event. For this register, it contains LDO1/LDO2, SW1/SW2 related interrupt events reflected on the SW_INT and LDO_INT bits on the TOP_INT register as long as they are unmasked on the Sub_INT2_Mask register.

This is WRITE AND CLEAR register.

Table 15. Sub_INT2 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	W/C	Reserved bit
6	RSVD	0	W/C	Reserved bit
5	RSVD	0	W/C	Reserved bit
4	RSVD	0	W/C	Reserved bit
3	VOUTSW1	0	W/C	SW1 Output Voltage Interrupt 0: The VOUTSW1_OK bit has not changed since the last time this bit was cleared. 1: The VOUTSW1_OK bit has changed since the last time this bit was cleared.
2	VOUTSW2	0	W/C	SW2 Output Voltage Interrupt 0: The VOUTSW2_OK bit has not changed since the last time this bit was cleared.

Table 15. Sub_INT2 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				1: The VOUTSW2_OK bit has changed since the last time this bit was cleared.
1	VOUTLDO1	0	W/C	LDO1 Output Voltage Interrupt 0: The VOUTLDO1_OK bit has not changed since the last time this bit was cleared. 1: The VOUTLDO1_OK bit has changed since the last time this bit was cleared.
0	VOUTLDO2	0	W/C	LDO2 Output Voltage Interrupt 0: The VOUTLDO2_OK bit has not changed since the last time this bit was cleared. 1: The VOUTLDO2_OK bit has changed since the last time this bit was cleared.

9.5.8 Sub level interrupt_2 mask (Sub_INT2_Mask, address 07h)

This is a READ AND WRITE register.

Table 16. Sub_INT2_Mask register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	1	R/W	Reserved bit
6	RSVD	1	R/W	Reserved bit
5	RSVD	1	R/W	Reserved bit
4	RSVD	1	R/W	Reserved bit
3	VOUTSW1 _MASK	1	R/W	VOUTSW1 Voltage Interrupt Mask bit 0: Not Masked 1: Masked
2	VOUTSW2 _MASK	1	R/W	VOUTSW2 Voltage Interrupt Mask bit 0: Not Masked 1: Masked
1	VOUTLDO1 _MASK	1	R/W	VOUTLDO1 Voltage Interrupt Mask bit 0: Not Masked 1: Masked
0	VOUTLDO2_MASK	1	R/W	VOUTLDO2 Voltage Interrupt Mask bit 0: Not Masked 1: Masked

08h register: Reserved

9.5.9 Top level control_0 (TOP_CTL0, address 09h)

This register contains various configuration bits for top level related functions, part 0. This is a READ AND WRITE register.

Table 17. TOP_CNTL0 register bit description

Bit	Symbol	Default value	Type	Function
7:5	VIN_ILIM_SEL	010	R/W	VIN input current limit selection: (min/typ/max)

Table 17. TOP_CNTL0 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
	[2:0]			000: 74 mA/85 mA/98 mA, (another default setting by MTP) 001: 222 mA/255 mA/293 mA 010: 370 mA/425 mA/489 mA (default setting) 011: 517 mA/595 mA/684 mA 100: 665 mA/765 mA/880 mA 101: 813 mA/935 mA/1075 mA 110: 961 mA/1105 mA/1271 mA 111: Input current limit disabled Note: VIN_ILIM_SEL [1] is the only bit that is MTP configurable
4	RSVD	0	R/W	Reserved bit
3	PWR_DN_EN[1]	0	R/W	Power-down Sequence Enable 0: Do not start power-down sequence 1: Start power-down sequence
2	RSVD	0	R/W	Reserved bit
1	RSVD	0	R/W	Reserved bit
0	PGood_EN	1	R/W	LDO1, LDO2, SW1, SW2 Output Voltage Status Indication 0: Output voltage power-good comparators are disabled. This will also set “VOUTSW1 _OK”, “VOUTSW2 _OK”, “VOUTLDO1_OK” and “VOUTLDO2 _OK” bits to 0 1: Output voltage power-good comparators are enabled

[1] A valid VIN does not generate the initial power-up sequence if all power rails have been turned off by setting PWR_DN_EN to 1. The use of PWR_DN_EN bit is prohibited to be used in any application that requires power-up sequence by both VIN and ON key.

9.5.10 Top level control_1 (TOP_CTL1, address 0Ah)

This register contains various configuration bits for top level related functions, part 1. This is a READ AND WRITE register.

Table 18. TOP_CNTL1 register bit description

Bit	Symbol	Default value	Type	Function
7 6	ASYS_PREWARNING [1:0]	10	R/W	ASYS Program a pre-warning voltage threshold on ASYS 00: 3.3 V 01: 3.4 V 10: 3.5 V 11: 3.6 V
5 4	ASYS_INPUT_SEL [1:0]	00	R/W	ASYS input source selection 00: ASYS is powered by either VIN_AUX or VIN (VIN has higher priority over VIN_AUX if both are presented but only when VIN>VIN_AUX) 01: ASYS is powered by VIN_AUX only 10: ASYS is powered by VIN only 11: ASYS is disconnected to either VIN_AUX or VIN (for internal testing purpose only)
3	RSVD	1	R/W	Reserved bit
2	VIN_OVP_SEL	0	R/W	VIN over-voltage protection threshold (rising) selection

Table 18. TOP_CNTL1 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				0: 5.50 V 1: 6.0 V **Note: The current default value for VIN_OVP_SEL is set at 5.5 V, but it should be MTP programmable**
1 0	VIN_UVLO_SEL [1:0]	01	R/W	Program an under-voltage lockout threshold (falling) on VIN 00: 2.9 V 01: 3.1 V 10: 3.3 V 11: 3.5 V

9.5.11 Top level control_2 (TOP_CTL2, address 0Bh)

This register contains various configuration bits for top level related functions, part 2. This is a READ AND WRITE register.

Table 19. TOP_CNTL2 register bit description

Bit	Symbol	Default value	Type	Function
7 6	ASYS_UVLO_SEL [1:0]	11	R/W	Program a UVLO threshold on ASYS 00: 2.4 V 01: 2.5 V 10: 2.6 V 11: 2.7 V
5	RSVD	0	R/W	Reserved bit
4 3 2	THEM_SHDN [2:0]	011	R/W	Program a thermal shutdown threshold, TSHDN, in rising(hysteresis with 20°C) 000: 95 °C 001: 100 °C 010: 105 °C 011: 110 °C 100: 115 °C 101: 120 °C 110: 125 °C 111: reserved
1 0	DIE_TEMP_WARNING [1:0]	10	R/W	Program a Die temperature warning threshold 00: 75 °C 01: 80 °C 10: 85 °C 11: 90 °C

9.5.12 Top level control_3 (TOP_CTL3, address 0Ch)

This register contains various configuration bits for top level related functions, part 3. This is a READ AND WRITE register.

Table 20. TOP_CNTL3 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5	RSVD	0	R/W	Reserved bit
4	MODE1_I2C	0	R/W	Depending on EN_MODE_SEL_BY_PIN_x (x="0", or "1", or "2", or "3") bit setting, the chip mode control is set by either the I^2C bit MODE1_I2C/ MODE0_I2C value, or the signal applied on external MODESEL1/ MODESEL1 pins. Refer to EN_MODE_SEL_BY_PIN description for more details. With EN_MODE_SEL_BY_PIN=0, the mode selection is determined by the following: [MODE1_I2C: MODE0_I2C] = 00, mode 0 setting [MODE1_I2C: MODE0_I2C] = 01, mode 1 setting [MODE1_I2C: MODE0_I2C] = 10, mode 2 setting [MODE1_I2C: MODE0_I2C] = 11, mode 3 setting
3	MODE0_I2C	0	R/W	
2	SW_RST	0	W/C	Chip software reset bit. If user write "1" to this bit, it will reset all other I^2C register bit to its default setting and cycle the regulator outputs, and meanwhile, this bit is cleared and reset back to "0" as well.
1	ON_GLT_LONG [1:0]	01	R/W	Program a long glitch timer on ON key 00: 4 s 01: 8 s 10: 12 s 11: 16 s Note: 2-bit MTP should be reserved to change the default setting
0				

9.5.13 Top level control_4 (TOP_CTL4, address 0Dh)

This register contains various configuration bits for top level related functions, part 4. This is a WRITE ONLY register.

Table 21. TOP_CNTL4 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	00000	W	Reserved bit
6				
5				
4				
3				
2	WD_TIMER_CLR [2:0]	000	W	Watchdog Timer Reset. 001: When written 001 to WD_TIMER_CLR [2:0], the watchdog timer is reset. All other values: when written to WD_TIMER_CLR [2:0], watchdog timer remains unaffected.
1				
0				

9.5.14 VIN_PWR Status_0 (PWR_STATUS_0, address 18h)

This register stores the present status of VIN power, part 0. This is a READ ONLY register. The status of this register is only valid when VIN_ILIM condition is not reached.

Table 22. VIN_PWR Status_0 register bit description

Bit	Symbol	Default value	Type	Function
7:6	RSVD	0	R	Reserved bit
5	IN_PWR_OK	0	R	IN_PWR (input power) status, refer to IN_PWR_STATUS [1:0] for more details 0: Input power voltages are invalid, i.e., IN_PWR_STATUS [1:0] ≠ 0b11 1: Input power voltages are valid, i.e., IN_PWR_STATUS [1:0] = 0b11
4:0	RSVD	0	R	Reserved bit

9.5.15 VIN_PWR Status_1 (PWR_STATUS_1, address 19h)

This register stores the present status of VIN power, part 1. This is a READ ONLY register. The status of this register is only valid when VIN_ILIM condition is not reached.

Table 23. VIN_PWR Status_1 register bit description

Bit	Symbol	Default value	Type	Function
7:6	IN_PWR_ STATUS	00	R	VIN and ASYS input power status 00: Input power is invalid. VIN < VIN_UVLO 01: Input power is invalid. ASYS < VIN_AUX + 100 mV typical, VIN > VIN_UVLO 10: input power is invalid. VIN > VIN_OVP 11: Input power is valid. VIN > VIN_UVLO, ASYS > VIN_AUX + 100 mV typical, VIN < VIN_OVP
5:0	RSVD	0	R	Reserved bit

9.5.16 Regulator status (REG_STATUS, address 20h)

This register stores the present status of the SW1, SW2, LDO1, LDO2. This is a READ ONLY register.

Table 24. REG_STATUS register bit description

Bit	Symbol	Default value	Type	Function
7	VOUTSW1 _OK	0	R	SW1 VOUT “Power-good” Status 0: VOUT_SW1 is not OK, i.e., VOUTSW1 / VOUTSW1(nominal) ≤ 90 % or VOUTSW1 / VOUTSW1(nominal) ≥ 110 % 1: VOUT_SW1 is OK, i.e., 110 % > VOUTSW1 / VOUTSW1(nominal) > 90 %
6	VOUTSW2 _OK	0	R	SW2 VOUT “Power-good” Status 0: VOUT_SW2 is not OK, i.e., VOUTSW2 / VOUTSW2(nominal) ≤ 90 % or VOUTSW2 / VOUTSW2(nominal) ≥ 110 % 1: VOUT_SW2 is OK, i.e., 110 % > VOUTSW2 / VOUTSW2(nominal) > 90 %
5	VOUTLDO1 _OK	0	R	LDO1VOUT “Power-good” Status 0: VOUTLDO1 is not OK, i.e., VOUTLDO1 / VOUTLDO1 (nominal) ≤ 90 % or VOUT LDO1 / VOUT LDO1 (nominal) ≥ 110 % 1: VOUTLDO1 is OK, i.e., 110 % > VOUTLDO1 / VOUTLDO1 (nominal) > 90 %
4	VOUTLDO2_OK	0	R	LDO2VOUT “Power-good” Status 0: VOUTLDO2 is not OK, i.e., VOUTLDO2 / VOUTLDO2 (nominal) ≤ 90 % or VOUTLDO2 / VOUTLDO2 (nominal) ≥ 110 %

Table 24. REG_STATUS register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				1: VOUTLDO2 is OK, i.e., 110 % > VOUTLDO2 / VOUTLDO2 (nominal) > 90 %
3	RSVD	0	R	Reserved bit
2	RSVD	0	R	Reserved bit
1	RSVD	0	R	Reserved bit
0	RSVD	0	R	Reserved bit

9.5.17 Active Discharge Regulator control (ACT_DISCHARGE_CNTL, address 21h)

This register stores the control functions of the SW1, SW2, LDO1, LDO2. This is a READ AND WRITE register.

Table 25. ACT_DISCHARGE_CNTL register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5	RSVD	0	R/W	Reserved bit
4	RSVD	0	R/W	Reserved bit
3	nEN_SW1_BLEED	0	R/W	SW1 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor
2	nEN_SW2_BLEED	0	R/W	SW2 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor
1	nEN_LDO1_ BLEED	0	R/W	LDO1 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor
0	nEN_LDO2_ BLEED	0	R/W	LDO2 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor

9.5.18 Mode configuration mode setting 0_0 (MODECFG_0_0, address 22h)

This register contains mode setting 0, part 0 configuration register. This is a READ AND WRITE register.

Table 26. MODECFG_0_0 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	EN_MODE_ SEL_BY_PIN_0	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 0: 0: mode control by internal I^2C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored.

Table 26. MODECFG_0_0 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^2C register bits, MODE0_I2C and MODE1_I2C **[1-bit MTP to set default value]**
5	SW1_OUT_0 [5:0]	010100	R/W	SW1 output voltage for mode setting 0 (see below). **[Note: The default value for SW1 _OUT_0[5:0] is set at 1.00 V, but it should be MTP programmable.]**
4				
3				
2				
1				
0				

Table 27. SW1 output voltage for Mode Setting 0

000000=0.500 V	001110=0.850 V	011100=1.200 V
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V
000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V **(default)**	100010=1.350 V
000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V
001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V
001100=0.800 V	011010=1.150 V	101000=1.500 V
001101=0.825 V	011011=1.175 V	101001 to 111110=1.5 V
		111111 = 1.8 V

9.5.19 Mode configuration mode setting 0_1 (MODECFG_0_1, address 23h)

This register contains mode setting A, part 1 configuration register. This is a READ AND WRITE register.

Table 28. MODECFG_0_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_0	0	R/W	Mode configuration upon falling edge applied on “ON” pin in Mode Setting 0: 0: upon valid falling edge applied on “ON” pin, the device will switch back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch)

Table 28. MODECFG_0_1 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				1: upon valid falling edge applied on “ON” pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_0_OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 0 0: SW2 Output Voltage = SW2_OUT_0_LSB [4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_0_LSB [4:0] + 1.2 V
4	SW2_OUT_0_LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 0 (see below). **Note: The default value for SW2_OUT_A_LSB [4:0] is set at 1.8 V, but it should be MTP programmable.**
3				
2				
1				
0				

Table 29. SW2 default output voltage for mode setting 0

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.20 Mode configuration mode setting 0_2 (MODECFG_0_2, address 24h)

This register contains mode setting 0, part 2 configuration register. This is a READ AND WRITE register.

Table 30. MODECFG_0_2 register bit description

Bit	Symbol	Default value	Type	Function
7	LDO1_ OUT_0 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 0 (see below). **Note: The default value for LDO1_OUT_0 [3:0] is set at 1.8V, but it should be MTP programmable.**
6				
5				
4				
3	SW1_EN_0	1	R/W	SW1 Enable Control in mode setting 0: 0: SW1 disabled 1: SW1 enabled **Note: reserve 1-bit MTP to set its default value**
2	SW2_EN_0	1	R/W	SW2 Enable Control in mode setting 0: 0: SW2 disabled 1: SW2 enabled **Note: reserve 1-bit MTP to set its default value**

Table 30. MODECFG_0_2 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
1	LDO1_EN_0	1	R/W	LDO1 Enable Control in mode setting 0: 0: LDO1 disabled 1: LDO1 enabled **Note: reserve 1-bit MTP to set its default value**
0	LDO2_EN_0	1	R/W	LDO2 Enable Control in mode setting 0: 0: LDO2 disabled 1: LDO2 enabled **Note: reserve 1-bit MTP to set its default value**

Table 31. LDO1 default output voltage for mode setting 0

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.21 Mode configuration mode setting 0_3 (MODECFG_0_3, address 25h)

This register contains mode setting 0, part 3 configuration register. This is a READ AND WRITE register.

Table 32. MODECFG_0_3 register bit description

Bit	Symbol	Default value	Type	Function
7 6	WD_TIMER_0 [1:0]	00	R/W	Watchdog timer setting in mode setting 0: 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s 10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s **[2-bit MTP to set default value]**
5	LDO2_OUT_0_ OFFSET	1	R/W	LDO2 output voltage offset selection in mode setting 0: 0: LDO2 Output Voltage = LDO2_OUT_0_LSB[4:0] + 0 V 1: LDO2 Output Voltage = LDO2_OUT_0_LSB[4:0] + 1.2 V **[1-bit MTP to set default value]**
4 3 2 1 0	LDO2_OUT_0_ LSB [4:0]	11001	R/W	LDO2 default output voltage for mode setting 0 (see below). **Note: The default value for LDO2_OUT_0_LSB [4:0] is set at 3.3 V, but it should be MTP programmable.**

Table 33. LDO2 default output voltage for mode setting 0

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V	10101=2.025 V

Table 33. LDO2 default output voltage for mode setting 0*...continued*

00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V **(default)**
01000=1.700 V	10001=1.925 V	

9.5.22 Mode configuration mode setting 1_0 (MODECFG_1_0, address 26h)

This register contains mode setting 1, part 0 configuration register. This is a READ AND WRITE register.

Table 34. MODECFG_1_0 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	EN_MODE_ SEL_BY_PIN_1	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 1: 0: mode control by internal I^2C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored. 1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^2C register bits, MODE0_I2C and MODE1_I2C
5	SW1_OUT_1 [5:0]	011100	R/W	SW1 output voltage for mode setting 1 (see below).
4				
3				
2				
1				
0				

Table 35. SW1 output voltage for Mode Setting 1

000000=0.500 V	001110=0.850 V	011100=1.200 V **(default)**
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V
000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V	100010=1.350 V
000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V
001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V

Table 35. SW1 output voltage for Mode Setting 1*...continued*

001100=0.800 V	011010=1.150 V	101000=1.500 V
001101=0.825 V	011011=1.175 V	101001 to 111110 = 1.5 V
		111111 = 1.8 V

9.5.23 Mode configuration mode setting 1_1 (MODECFG_1_1, address 27h)

This register contains mode setting 1, part 1 configuration register. This is a READ AND WRITE register.

Table 36. MODECFG_1_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_1	1	R/W	Mode configuration upon falling edge applied on “ON” pin in Mode Setting B: 0: upon valid falling edge applied on “ON” pin, the device will switch back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch) 1: upon valid falling edge applied on “ON” pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_1_ OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 1 0: SW2 Output Voltage = SW2_OUT_1_LSB[4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_1_LSB[4:0] + 1.2 V
4	SW2_OUT_1_ LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 1 (see below).
3				
2				
1				
0				

Table 37. SW2 default output voltage for mode setting 1

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.24 Mode configuration mode setting 1_2 (MODECFG_1_2, address 28h)

This register contains mode setting 1, part 2 configuration register. This is a READ AND WRITE register.

Table 38. MODECFG_1_2 register bit description

Bit	Symbol	Default value	Type	Function
7	LDO1_ OUT_1 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 1 (see below).
6				
5				
4				
3	SW1_EN_1	1	R/W	SW1 Enable Control in mode setting 1: 0: SW1 disabled 1: SW1 enabled
2	SW2_EN_1	1	R/W	SW2 Enable Control in mode setting 1: 0: SW2 disabled 1: SW2 enabled
1	LDO1_EN_1	1	R/W	LDO1 Enable Control in mode setting 1: 0: LDO1 disabled 1: LDO1 enabled
0	LDO2_EN_1	1	R/W	LDO2 Enable Control in mode setting 1: 0: LDO2 disabled 1: LDO2 enabled

Table 39. LDO1 default output voltage for mode setting 1

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9 V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.25 Mode configuration mode setting 1_3 (MODECFG_1_3, address 29h)

This register contains mode setting 1, part 3 configuration register. This is a READ AND WRITE register.

Table 40. MODECFG_1_3 register bit description

Bit	Symbol	Default value	Type	Function
7	WD_TIMER_1 [1:0]	00	R/W	Watchdog timer setting in mode setting 1: 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s 10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s
6				
5	LDO2_OUT_1_OFFSET	0	R/W	LDO2 output voltage offset selection in mode setting 1: 0: LDO2 Output Voltage = LDO2_OUT_1_LSB[4:0] + 0 V 1: LDO2 Output Voltage = LDO2_OUT_1_LSB[4:0] + 1.2 V
4	LDO2_OUT_1_LSB [4:0]	01100	R/W	LDO2 default output voltage for mode setting 1 (see below)
3				
2				
1				
0				

Table 41. LDO2 default output voltage for mode setting 1

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.26 Mode configuration mode setting 2_0 (MODECFG_2_0, address 2Ah)

This register contains mode setting 2, part 0 configuration register. This is a READ AND WRITE register.

Table 42. MODECFG_2_0 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	EN_MODE_ SEL_BY_PIN_2	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 2 0: mode control by internal I^2C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored. 1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^2C register bits, MODE0_I2C and MODE1_I2C
5	SW1_OUT_2 [5:0]	011100	R/W	SW1 output voltage for mode setting 2 (see below).
4				
3				
2				
1				
0				

Table 43. SW1 output voltage for Mode Setting 2

000000=0.500 V	001110=0.850 V	011100=1.200 V **(default)**
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V
000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V	100010=1.350 V
000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V

Table 43. SW1 output voltage for Mode Setting 2*...continued*

001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V
001100=0.800 V	011010=1.150 V	101000=1.500 V
001101=0.825 V	011011=1.175 V	101001 to 111110 = 1.5 V
		111111 = 1.8 V

9.5.27 Mode configuration mode setting 2_1 (MODECFG_2_1, address 2Bh)

This register contains mode setting 2, part 1 configuration register. This is a READ AND WRITE register.

Table 44. MODECFG_2_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_2	1	R/W	Mode configuration upon falling edge applied on “ON” pin in Mode setting 2 0: upon valid falling edge applied on “ON” pin, the device will switch back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch) 1: upon valid falling edge applied on “ON” pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_2_OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 2 0: SW2 Output Voltage = SW2_OUT_2_LSB[4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_2_LSB[4:0] + 1.2V
4	SW2_OUT_2_LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 2 (see below)
3				
2				
1				
0				

Table 45. SW2 default output voltage for mode setting 2

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.28 Mode configuration mode setting 2_2 (MODECFG_2_2, address 2Ch)

This register contains mode setting 2, part 2 configuration register. This is a READ AND WRITE register.

Table 46. MODECFG_2_2 register bit description

Bit	Symbol	Default value	Type	Function
7	LDO1_ OUT_2 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 2 (see below).
6				
5				
4				
3	SW1_EN_2	1	R/W	SW1 Enable Control in mode setting 2 0: SW1 disabled 1: SW1 enabled
2	SW2_EN_2	1	R/W	SW2 Enable Control in mode setting 2 0: SW2 disabled 1: SW2 enabled
1	LDO1_EN_2	1	R/W	LDO1 Enable Control in mode setting 2 0: LDO1 disabled 1: LDO1 enabled
0	LDO2_EN_2	1	R/W	LDO2 Enable Control in mode setting 2 0: LDO2 disabled 1: LDO2 enabled

Table 47. LDO1 default output voltage for mode setting 2

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9 V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.29 Mode configuration mode setting 2_3 (MODECFG_2_3, address 2Dh)

This register contains mode setting 2, part 3 configuration register. This is a READ AND WRITE register.

Table 48. MODECFG_2_3 register bit description

Bit	Symbol	Default value	Type	Function
7	WD_TIMER_2 [1:0]	00	R/W	Watchdog timer setting in mode setting 2 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s 10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s
6				
5	LDO2_OUT_2_ OFFSET	0	R/W	LDO2 output voltage offset selection in mode setting 2 0: LDO2 Output Voltage = LDO2_OUT_2_LSB[4:0] + 0 V 1: LDO2 Output Voltage = LDO2_OUT_2_LSB[4:0] + 1.2 V
4	LDO2_OUT_2_ LSB [4:0]	01100	R/W	LDO2 default output voltage for mode setting 2 (see below).
3				
2				

Table 48. MODECFG_2_3 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
1				
0				

Table 49. LDO2 default output voltage for mode setting 2

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.30 Mode configuration mode setting 3_0 (MODECFG_3_0, address 2Eh)

This register contains mode setting 3, part 0 configuration register. This is a READ AND WRITE register.

Table 50. MODECFG_3_0 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	EN_MODE_ SEL_BY_PIN_3	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 3 0: mode control by internal I^2C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored. 1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^2C register bits, MODE0_I2C and MODE1_I2C
5	SW1_OUT_3 [5:0]	011100	R/W	SW1 output voltage for mode setting 3 (see below).
4				
3				
2				
1				
0				

Table 51. SW1 output voltage for mode setting 3

000000=0.500 V	001110=0.850 V	011100=1.200 V **(default)**
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V

Table 51. SW1 output voltage for mode setting 3*...continued*

000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V	100010=1.350 V
000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V
001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V
001100=0.800 V	011010=1.150 V	101000=1.500 V
001101=0.825 V	011011=1.175 V	101001 to 111110 = 1.5 V
		111111 = 1.8 V

9.5.31 Mode configuration mode setting 3_1 (MODECFG_3_1, address 2Fh)

This register contains mode setting 3, part 1 configuration register. This is a READ AND WRITE register.

Table 52. MODECFG_3_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_3	1	R/W	Mode configuration upon falling edge applied on “ON” pin in mode setting 3 0: upon valid falling edge applied on “ON” pin, the device will switch back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch) 1: upon valid falling edge applied on “ON” pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_3_OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 3 0: SW2 Output Voltage = SW2_OUT_3_LSB[4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_3_LSB[4:0] + 1.2 V
4	SW2_OUT_3_LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 3 (see below).
3				
2				
1				
0				

Table 53. SW2 default output voltage for mode setting 3

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V

Table 53. SW2 default output voltage for mode setting 3*...continued*

00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.32 Mode configuration mode setting 3_2 (MODECFG_3_2, address 30h)

This register contains mode setting 3, part 2 configuration register. This is a READ AND WRITE register.

Table 54. MODECFG_3_2 register bit description

Bit	Symbol	Default value	Type	Function
7	LDO1_ OUT_3 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 3 (see below).
6				
5				
4				
3	SW1_EN_3	1	R/W	SW1 Enable Control in mode setting 3 0: SW1 disabled 1: SW1 enabled
2	SW2_EN_3	1	R/W	SW2 Enable Control in mode setting 3 0: SW2 disabled 1: SW2 enabled
1	LDO1_EN_3	1	R/W	LDO1 Enable Control in mode setting 3 0: LDO1 disabled 1: LDO1 enabled
0	LDO2_EN_3	1	R/W	LDO2 Enable Control in mode setting 3 0: LDO2 disabled 1: LDO2 enabled

Table 55. LDO1 default output voltage for mode setting 3

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9 V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.33 Mode configuration mode setting 3_3 (MODECFG_3_3, address 31h)

This register contains mode setting 3, part 3 configuration register. This is a READ AND WRITE register.

Table 56. MODECFG_3_3 register bit description

Bit	Symbol	Default value	Type	Function
7	WD_TIMER_3 [1:0]	00	R/W	Watchdog timer setting in mode setting 3 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s
6				

Table 56. MODECFG_3_3 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s
5	LDO2_OUT_3_OFFSET	0	R/W	LDO2 output voltage offset selection in mode setting D 0: LDO2 Output Voltage = LDO2_OUT_3_LSB[4:0] + 0 V 1: LDO2 Output Voltage = LDO2_OUT_3_LSB[4:0] + 1.2 V
4	LDO2_OUT_3_LSB [4:0]	01100	R/W	LDO2 default output voltage for mode setting 3 (see below)
3				
2				
1				
0				

Table 57. LDO2 default output voltage for mode setting 3

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.34 RESET reason monitoring (RESET_MONITOR, address 71h)

Register 0x71 is accessible by I^2C. It can be read to see what event caused the CPU power cycling by PMIC.

Table 58. RESET monitor register bit description

Bit	Symbol	Default value	Type	Function
7	ON_FILTERED	1	R	ON pin status; LOW level debounced for 5 ms (HIGH level propagates instantly). Write to this bit has no effect.
6:5	RSVD	0	RO	Reserved bits
4	THM_STDN_DONE	0	RW	PMIC exited thermal shutdown. All registers reset to defaults. Write 1 to clear.
3	RSVD	0	RO	Reserved bit
2	SW_RST_DONE	0	RW	A system reset caused by Software Reset command has occurred. All registers were reset to their defaults. Write 1 to clear.
1	WD_RST_DONE	0	RW	A system reset caused by Watchdog Timer has occurred. Registers were NOT reset to their defaults. Write 1 to clear.

Table 58. RESET monitor register bit description*...continued*

Bit	Symbol	Default value	Type	Function
0	LONG ON_DONE	0	RW	A system reset caused by long ON press has occurred. All registers were reset to their defaults. Write 1 to clear.

10 Limiting values

Table 59. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
Voltage range (with respect to AGND)	VIN		-0.3	20	V
	ASYS, VIN_AUX, VBAT_BKUP		-0.3	6	V
	LX1, LX2		-2	6	V
	SW1_OUT, SW2_OUT		-0.3	6	V
	LDO1, LDO2		-0.3	6	V
	SDA, SCL, MODESEL0, MODESEL1, ON, TS, SYSRSTn, INTB		-0.3	6	V
	PGND to AGND		-0.3	0.3	V
$I_{O(sink)}$	Output sink current	on pins SYSRSTn, INTB, SDA, SCL		5	mA
T_j	Junction temperature		–40	125	°C

11 ESD ratings

Table 60. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	-	2000	V
		Charged device model (CDM)	-	500	V

12 Recommended operating conditions

Table 61. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	Supply Voltage	VIN	3.3	5.5	V
V_{IO}	Input/output voltage	SDA, SCL, MODESEL0, MODESEL1, SYSRSTn	0	3.6	V
T_{amb}	Ambient Temperature		-40	85	°C
T_j	Junction Temperature		-40	125	°C
T_{stg}	Storage Temperature		-55	150	°C
V_{TS}	voltage at TS pin	TS	0	5.0	V

13 Electrical characteristics

Unless otherwise specified, V_{VIN}=5 V, V_{VIN_AUX}=3.8 V, LDO1_OUT=1.8 V, LDO2_OUT=1.8 V. C_{VIN}=2.2 µF/10 V, C_{ASYS}=4.7 µF/10 V, C_{VIN_AUX}=1 µF/10 V, C_{LDO1_OUT}=1 µF/6.3 V, C_{LDO2_OUT}=2.2 µF/6.3 V, C_{SW1_OUT}=10 µF/6.3 V, C_{SW2_OUT}=10 µF/6.3 V, L_{SW1} =2.2 µH, L_{SW2} =2.2 µH, T_{amb}= -40 °C to +85 °C, Typical value at T_{amb}=25 °C

13.1 Top level parameter

Table 62. EC table for Top level

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIN_AUX QUIESCENT CURRENT						
$I_{VIN\_AUX\_NOLOAD1}$	VIN_AUX quiescent Current VIN_AUX=4.5 V SW1, SW2, LDO1, LDO2 enabled, no load. No switching on SW1, SW2. VIN = open	T_J = 25 °C		2.9	4.5	µA
		T_J = 85 °C [1]		4.5	8	
$I_{VIN\_AUX\_NOLOAD2}$[1]	VIN_AUX quiescent Current VIN_AUX = 4.5 V SW1, SW2, LDO1, LDO2 enabled, no load. Switching on SW1, SW2. VIN = open	T_J = 25 °C		3.5	5	µA
		T_J = 85 °C		5.5	11	
$I_{VIN\_AUX\_DISABLE}$[1]	VIN_AUX quiescent Current VIN_AUX = 4.5 V SW1, SW2, LDO1, LDO2 Disabled VIN = open	T_J = 25 °C		750	1200	nA
		T_J = 85 °C		1500	3000	
VIN						
VIN_{UVLO}	VIN Under voltage lock-out	I^2C programmable in 200 mV steps, VIN Falling	2.9		3.5	V
$VIN_{UVLO\ Accuracy}$			-5		+5	%
VIN_{UVLO_HYS}	Hysteresis on VINUVLO			200		mV
VIN_{OVP}		I^2C programmable at 5.5 V or 6 V, VIN Rising	5.5		6.0	V
$VIN_{OVP\ Accuracy}$	Input over- voltage protection threshold		-3.5		+3.5	%
$VIN_{OVP\ Hysteresis}$		VIN Falling		100		mV
$t_{DGL(VINOVP)}$ [1]	Input over-voltage reaction time	VIN: 5 V → 7 V, 1 V/µs		1.5	3	µs
VIN Current Limit	Input current limit	VIN_ILIM [2:0] = 000	74	85	98	mA
		VIN_ILIM [2:0] = 010	370	425	489	
ASYS						

Table 62. EC table for Top level*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ASYS\_UVLO\_RISING}$		ASYS in rising		2.8		V
$V_{ASYS\_UVLO\_FALLING}$		ASYS in falling		2.7		V
		By MTP		2.4		
$\%V_{ASYS\_UVLO\_FALLING}$	ASYS UVLO Accuracy		-3.5		+3.5	%
$V_{ASYS\_UVLO\_HYS}$	ASYS UVLO Hysteresis	400 mV for 2.4 V falling threshold		100 or 400		mV
$T_{ASYS\_SW\_DELAY}$		Time when ASYS voltage is switched between VIN and VIN_AUX		0.5		ms
$V_{ASYS\_PREWARNING}$	ASYS Pre-Warning Threshold Accuracy	ASYS falling, I^2C programmable		3.3 3.4 3.5 3.6		V
$\%V_{ASYS\_PREWARNING}$	ASYS Pre-Warning Threshold Accuracy		-4		+4	%
$V_{ASYS\_PREWARNING\_HYS}$	ASYS Pre-warning Threshold Hysteresis			100		mV
VBAT_BKUP						
VBAT_BKUP UVLO		VBAT_BKUP falling edge		1.9		V
VBAT_BKUP UVLO Accuracy			-5		5	%
VBAT_BKUP UVLO Hysteresis				100		mV
PROTECTION[1]						
$T_{WARNING}$	Pre-warning temperature	2-bit programmable, T_WARNING [1:0]		75 80 85 90		°C
$T_{WARNING\_HYS}$	Pre-warning threshold Hysteresis			20		°C
T_{SHDN}	Thermal shutdown	3-bit programmable,THEM_ SHDN [2:0], in 5 °C steps		95 to 125		°C
T_{SHDN_HYS}	Thermal shutdown Hysteresis			20		°C
WATCHDOG & SAFETY TIMER						
T_{WD_TIMER} Range	Watchdog Timer	When enabled via I^2C Programming	-15%	Disable 16 32 64	+15%	s

Table 62. EC table for Top level*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER UP/DOWN SEQUENCE TIMING[1]						
$T_{PWUP\_DLY\_INI}$	Power up Initial delay	Time from ON signal asserts to the first output rail reaches 90 % of its nominal value		2		ms
$T_{PWDN\_DLY\_INTERVAL}$	Power down interval delay	Delay between power rail		2		ms
$T_{PWUP\_DLY\_INTERVAL}$	Power up interval delay	For power up: this is the time from previous voltage rail reaches 90 % of its nominal value to the time when the following voltage rail reaches its 90 % nominal value For power down: this is the time from the previous voltage rail starts falling to the time the following rail starts falling		1		ms

[1] Guaranteed by design and characterization; not tested in production.

13.2 BUCK1 (SW1)

Table 63. EC table for BUCK1 (SW1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN(SW1)}$	Input voltage range for CORE BUCK	Input is PSYS1, guaranteed by design	2.5		5.5	V
$I_{OUT(SW1)\ MAX}$	Max Output Current	Over V_{PSYS1}, guaranteed by design	250			mA
V_{SW1} Range	Output range for CORE BUCK	I^2C programmable from 0.5 V to 1.5 V in 25 mV/step, a fixed 1.8 V	0.5		1.5	V
V_{SW1_OUT} Accuracy	CORE BUCK DC Output Accuracy	Over full V_{PSYS1}, $I_{OUT(SW1)}$, -40 °C ≤ T_{amb} ≤ +85 °C, for all V_{SW1_OUT} except for 500 mV and 1.8 V	-3		+3	%
		Over full V_{PSYS1}, $I_{OUT(SW1)}$, -40 °C ≤ T_{amb} ≤ +85 °C, for only V_{SW1_OUT} =1.8 V	-3.5		+3.5	
		Over full V_{PSYS1}, $I_{OUT(SW1)}$, -40 °C ≤ T_{amb} ≤ +85 °C, for only V_{SW1_OUT} =0.5 V	-4		+4	
ΔV_{SW1} / ΔV_{PSYS1}	DC Line regulation	$V_{SW1(NOM)}$+0.5 V < V_{PSYS1} < 5.5 V, $I_{OUT(SW1)}$ = 250 mA		0.15		%/V
ΔV_{SW1} / $\Delta I_{OUT(SW1)}$	DC Load regulation	0 mA < $I_{OUT(SW1)}$ < 250 mA		0.008		%/mA
$T_{ON\ (SW1)}$		-40 °C ≤ T_{amb} ≤ +85 °C [1]	110	240	350	ns
$I_{IN(SW1)}$[1]	Quiescent current	SW1 enabled, $I_{OUT(SW1)}$ = 0, no switching		700		nA
Inductor value	L			2.2		µH
$R_{DSON(SW1)}$[1]	High Side P-FET R_{DSON}	V_{PSYS1}=5 V		500	900	mΩ
	Low Side N-FET R_{DSON}	V_{PSYS1}=5 V		250	450	
$R_{STDN(SW1)}$	SW1 Output Active Discharge Resistance			50		Ω
$I_{LIM(SW1)}$	Internal Peak Current Limit	Cycle by cycle peak current limit	700	950	1200	mA
$t_{ONMIN(SW1)}$	Minimum On-Time			50		ns
$t_{OFFMIN(SW1)}$	Minimum-Off Time			10		ns
$t_{SSTART(SW1)}$	Soft-start time	V_{SW1OUT}=1.2 V		1.2		ms
Efficiency[1]	V_{PSYS1}=5 V, V_{SW1OUT}=1.5 V	@I_{OUT}=10 µA		> 76		%
		@I_{OUT}=100 µA		> 84		%
		@I_{OUT}=65 mA		> 86		%

Table 63. EC table for BUCK1 (SW1)*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		@I_{OUT}=125 mA		> 86		%
		@I_{OUT}=250 mA		> 84		%

[1] Guaranteed by design and characterization; not tested in production.

13.3 BUCK2 (SW2)

Table 64. EC table for BUCK2 (SW2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN(SW2)}$	Input voltage range for SW2	Input is V_{PSYS2}	2.5		5.5	V
$I_{OUT(SW2)MAX}$	Maximum Output Current	Over V_{PSYS2}	500			mA
V_{SW2_RANGE}	Output range for SW2	I^2C programmable, 25 mV/step	1.5		2.1	V
			2.7		3.3	
$V_{SW2\_Accuracy}$	SW2 DC Output Accuracy	Over full V_{PSYS2}, $I_{OUT(SW2)}$, T_{amb}=room temp	-2		2	%
		Over full V_{PSYS2}, $I_{OUT(SW2)}$, temperature range	-3		3	%
ΔV_{SW2} / ΔV_{PSYS2}	DC Line regulation	$V_{SW2OUT(NOM)}$+0.5 V < V_{PSYS2} < 5.5 V, $I_{OUT(SW1)}$ = 500 mA		0.15		%/V
ΔV_{SW2} / $\Delta I_{OUT(SW2)}$	DC Load regulation	0 mA < $I_{OUT(SW1)}$ < 500 mA		0.008		%/mA
$T_{ON\ (SW2)}$			250	360	490	ns
IIN(SW2)[1]	Quiescent current	SW2 enabled, $I_{OUT(SW2)}$ = 0, no switching		700		nA
Inductor value	L			2.2		µH
$R_{DSON(SW2)}$[1]	High Side P-FET RDSON	V_{PSYS2} = 5 V		250	450	mΩ
	Low Side N-FET RDSON	V_{PSYS2} = 5 V		125	250	
$R_{STDN(SW2)}$	SW2 Output Active Discharge Resistance			50		Ω
$I_{LIM(SW2)}$	Peak Current Limit	Cycle by cycle peak current limit	900	1300	1800	mA
$t_{ONMIN(SW2)}$	Min. On Time			50		ns
$t_{OFFMIN(SW2)}$	Max On Time			10		ns
$t_{SSTART(SW2)}$	Softstart time	V_{SW2OUT}=1.8 V		1.8		ms
Efficiency[1]	V_{PSYS2}5 V V_{SW2OUT} = 1.8 V	@I_{OUT}=10 µA		> 78		%
		@I_{OUT}=100 µA		> 87		
		@I_{OUT}=125 mA		> 88		
		@I_{OUT}=250 mA		> 88		
		@I_{OUT}=500 mA		> 86		

[1] Guaranteed by design and characterization; not tested in production.

13.4 LDO1 (Always-on LDO)

Table 65. EC table for LDO1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN_LDO1}	Input voltage range for Always- On LDO	Whichever is higher between VBAT_BKUP and ASYS	2.0		5.5	V
$I_{OUT\_LDO1\_MAX}$	Maximum Output DC Current		1			mA
$I_{OUT\_LDO1\_LIMIT}$	Internal Current Limit	LDO1_OUT = GND	1.4	3.3	7.0	mA
V_{LDO1_OUT} Range	LDO1 nominal output voltage	I^2C Programmable, 25 mV/step	1.700		1.900	V
V_{LDO1_OUT} Accuracy	LDO1 Output Voltage Accuracy	Over V_{IN_LDO1}, I_{OUT}= 0 to 1 mA	-3		+3	%
ΔV_{LDO1_OUT} / ($V_{LDO1\_OUT(NOM)}$ x ΔV_{IN_LDO1})	DC Line regulation	$V_{LDO1\_OUT(NOM)}$+0.5 V < V_{IN_LDO1} < 5 V, I_{OUT}= 1 mA		1		%/V
ΔV_{LDO1_OUT} / ($V_{LDO1\_OUT(NOM)}$ x ΔV x ΔI_{OUT})	DC Load regulation	0 mA < I_{OUT} < 1 mA		1		%/mA
Power Supply Rejection Ratio (PSRR) [1]				40		dB
$I_{IN(LDO1)}$	Quiescent current	I_{OUT} =0 mA		94		nA
$V_{DROPOUT(LDO1)}$ [1] [2]	Dropout Voltage	I_{OUT}=1 mA			200	mV
$R_{STDN(LDO1)}$	LDO1 Output Active Discharge Resistance			50		Ω

[1] Guaranteed by design and characterization; not tested in production.
[2] Dropout voltage is defined as the input-to-output difference in the predefined load when the output is below 100 mV to the nominal regulation voltage.

13.5 LDO2 (System LDO)

Table 66. EC table for LDO2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN_LDO2}	Input voltage range	ASYS	2.5		5.5	V
$I_{OUT\_LDO2\_MAX}$	Maximum Output Current		250			mA
$I_{OUT\_LDO2\_LIMIT}$[1]	Internal Current Limit	LDO2_OUT = GND	300	450	600	mA
V_{LDO2_OUT} Range	LDO2 output voltage range	programmable 25mV steps	1.5		2.1	V
			2.7		3.3	
V_{LDO2_OUT} Accuracy	LDO2 Output Accuracy	Over V_{IN_LDO2}, I_{OUT}, temperature	-3.5		3.5	%
ΔV_{LDO2_OUT} / ($V_{LDO2\_OUT(NOM)}$ x ΔV_{IN_LDO2})	DC Line regulation	$V_{LDO2\_OUT(NOM)}$+0.5 V < V_{IN_LDO2} < 5.5 V, I_{OUT} = 250 mA		0.35		%/V
ΔV_{LDO2_OUT} / ($V_{LDO2\_OUT(NOM)}$ x ΔI_{OUT})	DC Load regulation	0 mA < I_{OUT} < 250 mA		0.0065		%/mA
PSRR[1]	Power Supply Rejection Ratio			40		dB
$I_{IN(LDO2)}$	Quiescent current	I_{OUT} = 0 mA		450		nA
$V_{DROPOUT(LDO2)}$[2]	Dropout Voltage	I_{OUT} = 100 mA			150	mV
$R_{STDN(LDO2)}$	LDO2 Output Active Discharge Resistance			150		Ω

[1] Guaranteed by design and characterization; not tested in production.
[2] Dropout voltage is defined as the input-to-output difference in the predefined load when the output is below 100mV to the nominal regulation voltage.

13.6 I²C Interface and Logic I/O

Table 67. EC table for I²C and Logic

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SERIAL INTERFACE (SCL & SDA)						
V_{PULLUP} Range[1]	Pullup Voltage Range		1.5		3.6	V
F_{I2C}	I²C Clock frequency	On SCL	0		1000	kHz
V_{IH}	HIGH-level Input voltage		1.5			V
V_{IL}	LOW-level Input voltage				0.5	V
V_{hys}	Hysteresis of Schmitt trigger inputs		0.01			V
V_{OL}	LOW-level output voltage at 3 mA sink current		0		0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; Standard and Fast modes	3			mA
		V_{OL} = 0.6 V; Fast mode	6			mA
I_{IL}	LOW-level input current	Pin voltage: 0.1xVpullup to 0.9x Vpullup max	-10		10	µA
C_I	Capacitance of IO pin				10	pF
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26			µs
t_{LOW}	LOW period of I²C clock	Fast mode plus	0.5			µs
t_{HIGH}	HIGH period of I²C clock	Fast mode plus	0.26			µs
$t_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26			µs
$t_{HD,DAT}$	Data Hold time	Fast mode plus	0			µs
$t_{SU,DAT}$	Data Setup time	Fast mode plus	50			ns
t_r	Rise time of I2C_SCL and I2C_SDA signals	Fast mode plus			120	ns
t_f	Fall time of I2C_SCL and I2C_SDA signals	Fast mode plus			120	ns
$t_{SU,STO}$	Setup time for STOP condition	Fast mode plus	0.26			µs
t_{BUF}	Bus free time between STOP and START condition	Fast mode plus	0.5			µs
$t_{VD,DAT}$	Data valid time	Fast mode plus			0.45	µs
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode plus			0.45	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter		0		50	ns

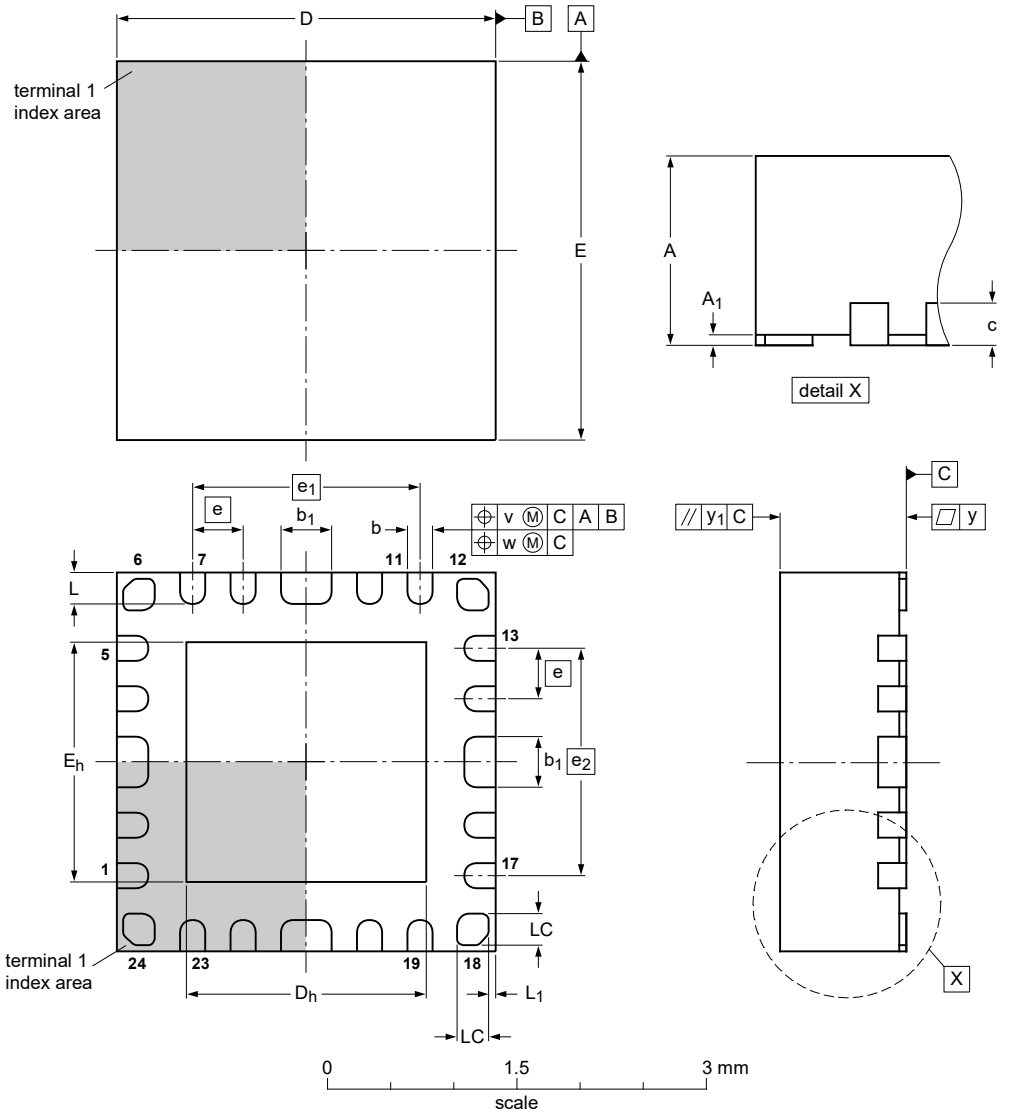
Table 67. EC table for I^2C and Logic*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MODESEL0/MODESEL1						
V_{IH1}	Logic Input HIGH Threshold		1.5			V
V_{IL1}	Logic Input LOW Threshold				0.4	V
I_{LK1}	Logic Pin Leakage Current	Pulled up to 5.0 V		0.1	1	µA
$t_{debounce\_1}$	Debounce time for MODESEL0, MODESEL1			1		µs
ON						
V_{IH2}	Logic Input HIGH Threshold	Note: ON pin internally pulled up, no external pullup voltage needed.	70 % * VIN_AUX			V
V_{IL2}	Logic Input LOW Threshold				0.4	V
$t_{debounce}$	Debounce time for ON	To initiate the default power-up sequence		200		µs
SYSRSTn, INTB						
V_{OL1}	LOW-level output voltage at 1 mA sink current				0.5	V
I_{LK2}	Logic Pin Leakage Current	Pulled up to 5.0 V		0.01	0.1	µA
$V_{PULLUP1}$	Minimum Supply Voltage for valid Open-drain signal		1.5			V

[1] Guaranteed by design and characterization; not tested in production.

14 Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3 x 3 x 0.85 mm **SOT905-1**



DIMENSIONS (mm are the original dimensions)

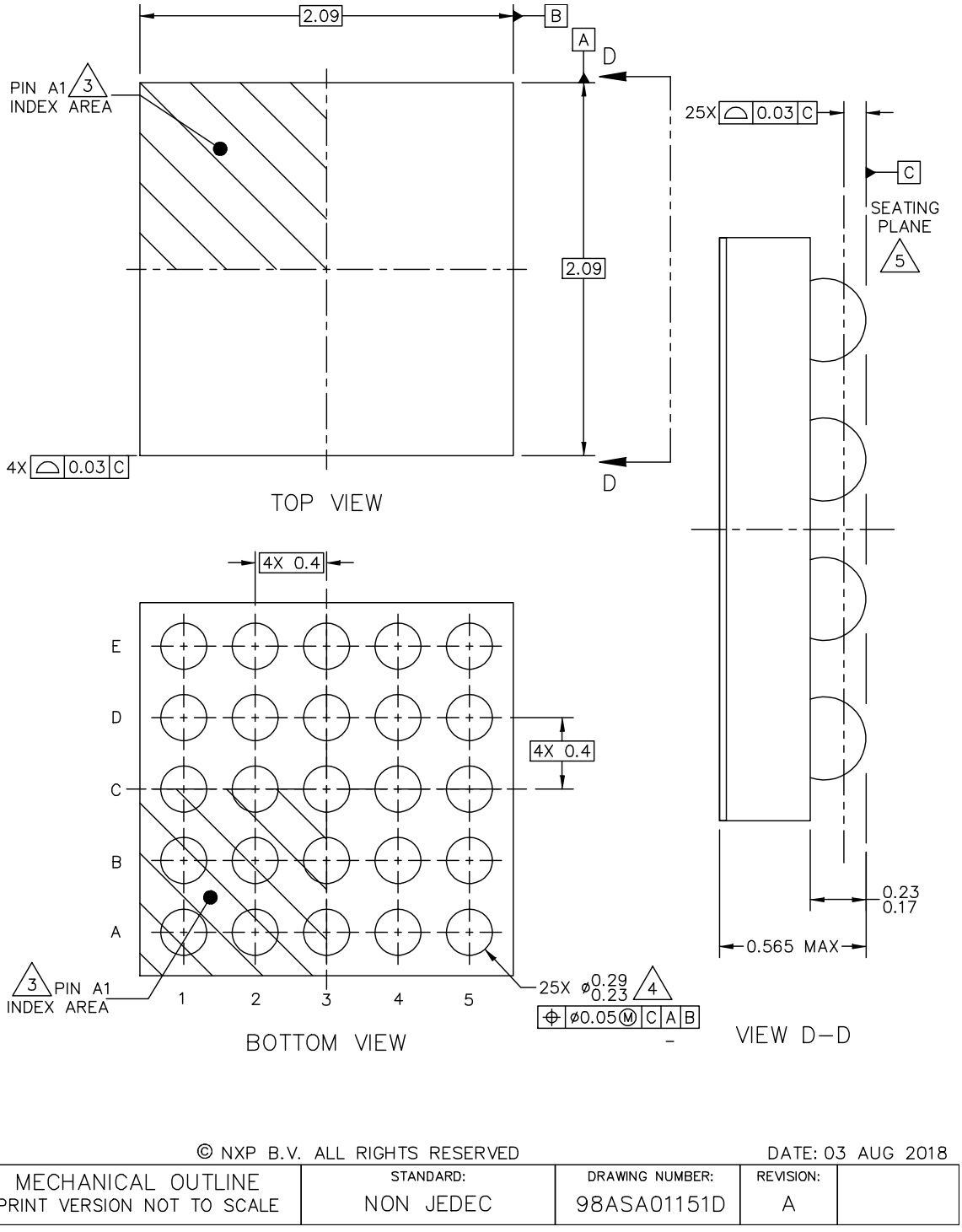
UNIT	A(1) max	A_1	b	b_1	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	L_1	LC	v	w	y	y_1
mm	1	0.05 0.00	0.25 0.15	0.45 0.35	0.2	3.1 2.9	2.05 1.75	3.1 2.9	2.05 1.75	0.4	1.8	1.8	0.35 0.15	0.1 0.0	0.3 0.2	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT905-1	- - -	- - -	- - -			~~06-03-13~~ 06-03-31

Figure 9. Package outline SOT905-1 (HVQFN24)



DATE: 03 AUG 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01151D	REVISION: A	

Figure 10. Package outline SOT1401-4 (WLCSP25) (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

DATE: 03 AUG 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01151D	REVISION: A	

Figure 11. Package outline SOT1401-4 (WLCSP25) (2 of 2)

15 Packing information

15.1 SOT905-1 HVQFN24; reel dry pack, SMD, 7" Q2 standard product orientation ordering code (12NC) ending 547

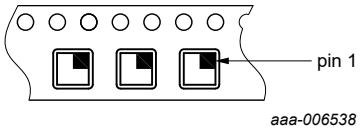
15.1.1 Dimensions and quantities

Table 68. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box
178 × 12	1400	1

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

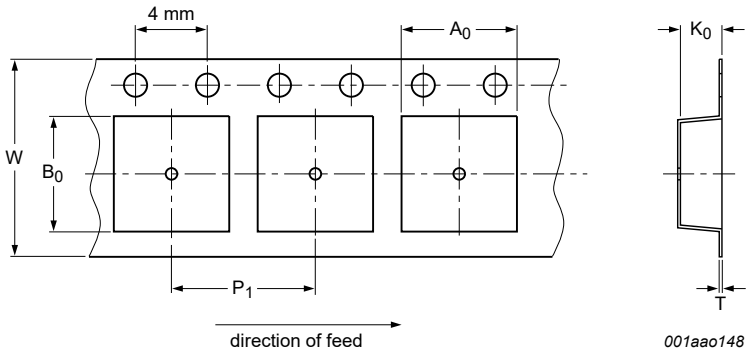
15.1.2 Product orientation



Pin 1 is in quadrant 2.

Figure 12. Product orientation in carrier tape

15.1.3 Carrier tape dimensions



Not drawn to scale.

Figure 13. Carrier tape dimensions

Table 69. Carrier tape dimensions

In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
3.30 ± 0.1	3.30 ± 0.1	1.10 ± 0.1	0.30 ± 0.5	8.0 ± 0.1	12 +.3/-.0

15.2 SOT1401-4 WLCSP25; reel dry pack, SMD, 7" Q1 standard product orientation ordering code (12NC) ending 012

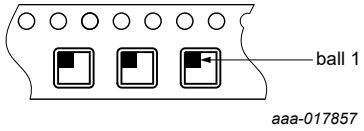
15.2.1 Dimensions and quantities

Table 70. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box
180 × 8	3000	1

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

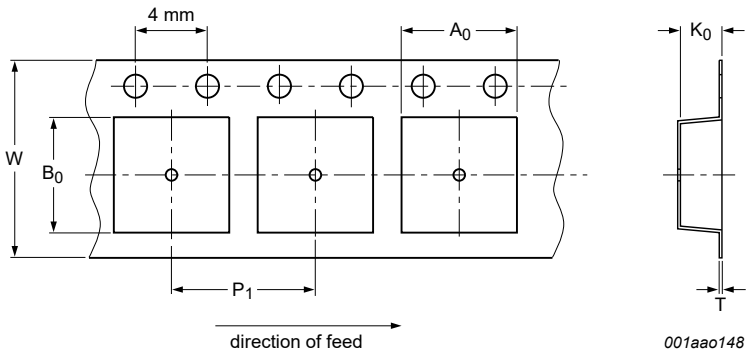
15.2.2 Product orientation



Ball 1 is in quadrant 1.

Figure 14. Product orientation in carrier tape

15.2.3 Carrier tape dimensions



Not drawn to scale.

Figure 15. Carrier tape dimensions

Table 71. Carrier tape dimensions

In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
2.27 ± 0.05	2.27 ± 0.05	0.67 ± 0.05	0.25 ± 0.02	4.0 ± 0.10	8 +0.30/-0.10

16 Revision history

Table 72. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9421 v.1.0	20231016	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com

Date of release: 16 October 2023
Document identifier: PCA9421