PCA9420

Power management IC for low-power microcontroller applications

Rev. 4.2 — 26 July 2023   **Product data sheet**

1 General description

The PCA9420 is a highly integrated Power Management IC (PMIC), targeted to provide a full power management solution for low-power microcontroller applications or other similar applications.

The device consists of a linear battery charger capable of charging up to 315 mA current. It has an I^2C programmable Constant Current (CC) and Constant Voltage (CV) values for flexible configuration. Various built-in protection features such as input overvoltage protection, overcurrent protection, thermal protection, etc. are also provided for safe battery charging. It also features JEITA-compliant charging.

The device also integrates two step-down (buck) DC-DC converters which have I^2C programmable output voltage. Both buck regulators have integrated high-side and low-side switches and related control circuitry, to minimize the external component counts; a Pulse-Frequency Modulation (PFM) approach is utilized to achieve better efficiency under light load condition. Other protection features such as overcurrent protection, under-voltage lockout (UVLO), etc., are also provided. By default, the input for these regulators is powered by either VIN or VBAT, whichever is greater.

In addition, two on-chip LDO regulators are provided to power up various voltage rails in the system.

Other features such as Fm+ I^2C-bus interface, chip enable, interrupt signal, etc. are also provided.

The chip is offered in 2.09 mm x 2.09 mm, 5 x 5 bump, 0.4 mm pitch WLCSP package; and 3 mm x 3 mm, 24-pin QFN package.

2 Features and benefits

- Linear battery charger for charging single cell li-ion battery
  - 20 V tolerance on VIN pin
  - Programmable input OVP (5.5 V or 6 V)
  - Programmable constant current (up to 315 mA) and pre-charge low voltage current threshold
  - Programmable constant voltage regulation
  - Programmable automatic recharge voltage and termination current threshold
  - Built-in protection features such as input OVP, battery SCP, thermal protection
  - JEITA compliant
  - Battery attached detection
  - Over-temperature protection
- Two step-down DC-DC converters
  - Very low quiescent current
  - Programmable output voltage
  - SW1: core buck converter, 0.5 V to 1.5 V output, 25 mV/step, and a fixed 1.8 V, up to 250 mA
  - SW2: system buck converter, 1.5 V to 2.1 V/2.7 V to 3.3 V output, 25 mV/step, up to 500 mA
  - Low-power mode for extra power saving
- Two LDOs
  - Programmable output voltage regulation
  - LDO1: always-on LDO, 1.70 V to 1.90 V output, 25 mV/step, up to 1 mA

    – LDO2: system LDO, 1.5 V to 2.1 V/2.7 V to 3.3 V output, 25 mV/step, up to 250 mA
- 1 MHz I²C-bus target interface
- -40 °C to +85 °C ambient temperature range
- Offered in 5 x 5 bump-array WLCSP and 24-pin QFN package

3 Applications

- Low power microcontroller application

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	NXP processor	Package		
			Name	**Description**	**Version**
PCA9420BS	420	i.MX RT5xx/i.MX RT6xx	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3 x 3 x 0.85 mm	SOT905-1
PCA9420UK	9420	i.MX RT5xx/i.MX RT6xx	WLCSP25	wafer level chip-scale package, 25 terminals, 0.4 mm pitch, 2.09 mm x 2.09 mm x 0.525 mm body	SOT1401-4
PCA9420KUK	9420	NXH3670/NXH3675	WLCSP25	wafer level chip-scale package, 25 terminals, 0.4 mm pitch, 2.09 mm x 2.09 mm x 0.525 mm body	SOT1401-4

4.1 Ordering options

Table 2. Ordering options

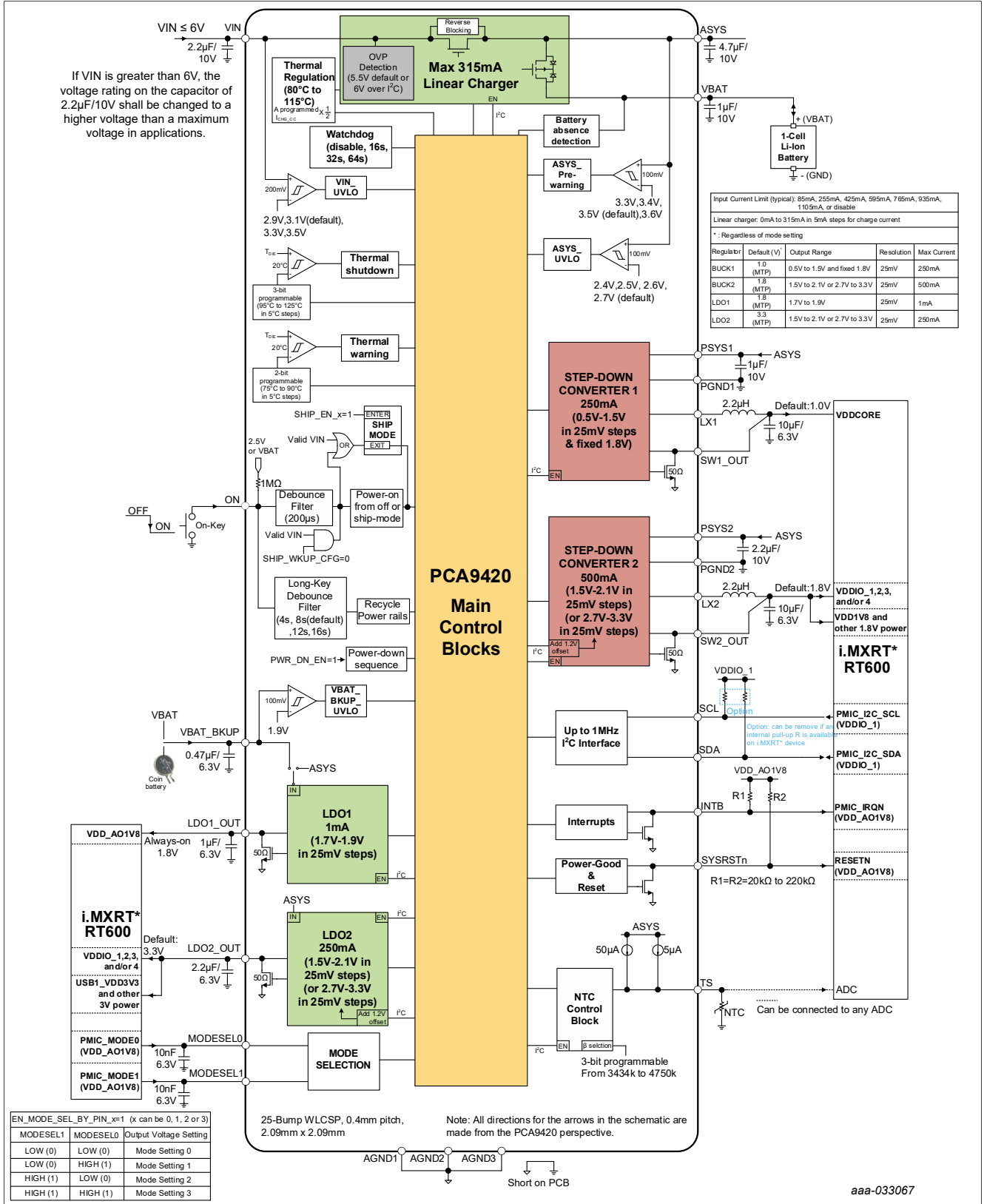| Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range (T$_{amb}$)
PCA9420BS	PCA9420BSAZ	HVQFN24	REEL 7" Q2 NDP	1400	-40 °C to +85 °C
PCA9420UK	PCA9420UKZ	WLCSP25	REEL 7" Q1 DP CHIPS	3000	-40 °C to +85 °C
PCA9420KUK	PCA9420KUKZ	WLCSP25	REEL 7" Q1 DP CHIPS	3000	-40 °C to +85 °C

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5 Simplified block diagram

Figure 1. Simplified block diagram

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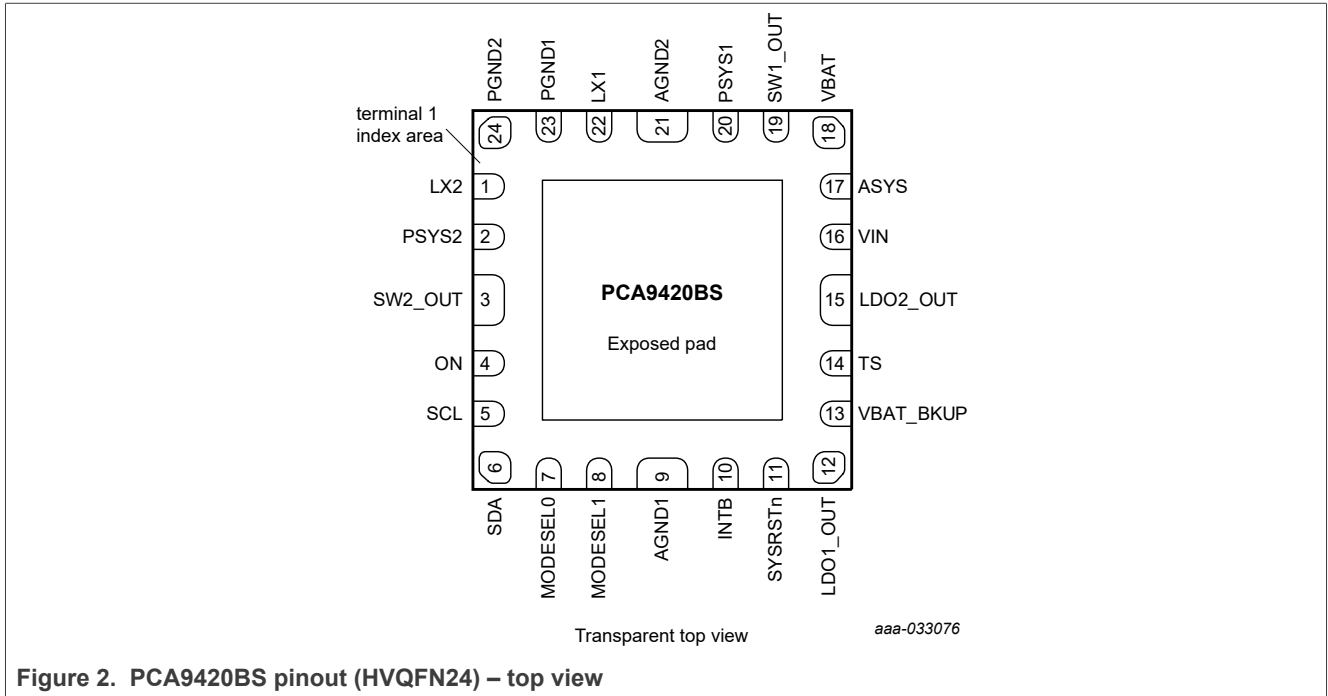# 6 Pinning information

6.1 Pinning
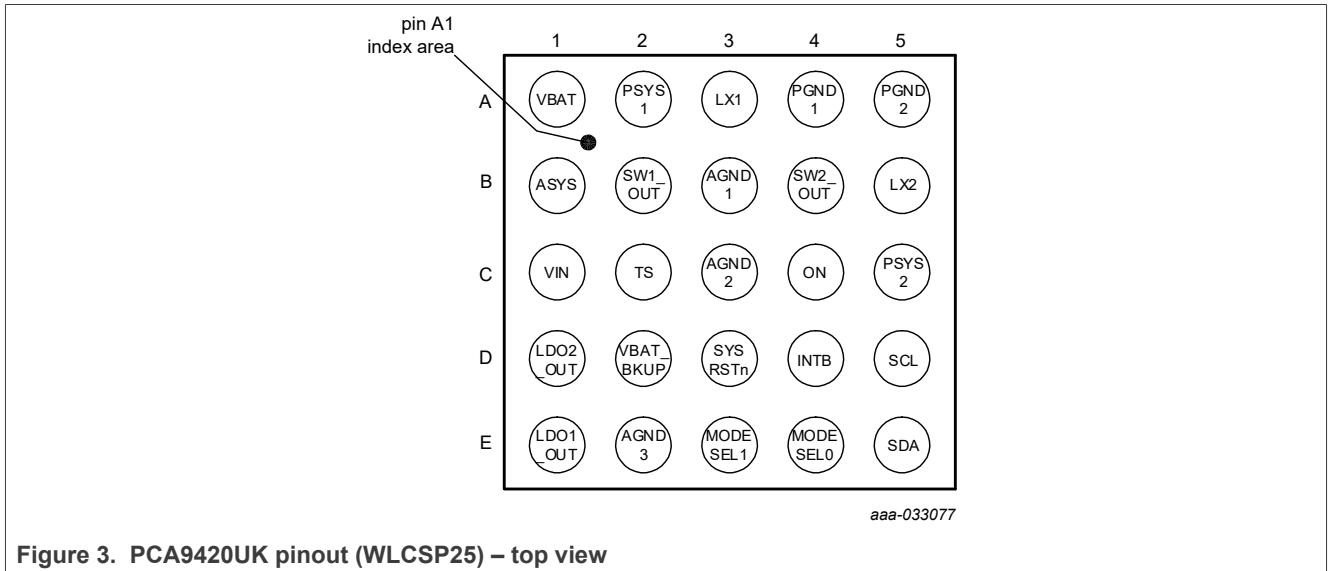

Figure 2. PCA9420BS pinout (HVQFN24) – top view

Figure 3. PCA9420UK pinout (WLCSP25) – top view

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Pin Type	Description
	HVQFN24	WLCSP25		
INPUT SUPPLY				
VIN	16	C1	P	Input supply voltage. Bypass with a 2.2 µF/10 V ceramic capacitor. If VIN is greater than 6 V, the voltage rating shall be changed to a higher voltage than the maximum voltage in applications.
ASYS	17	B1	P	Bypass output of VIN and input supply voltage for LDO2 and linear charger, connect with a typical 4.7 µF or 10 µF/10 V decoupling capacitor.
VBAT_BKUP	13	D2	P	Backup battery input voltage. LDO1 is powered by the greater of ASYS or VAT_BKUP. If a back-up battery with a coin cell is not connected, connect the pin to VBAT power domain. Connect with a typical 0.47 µF/6.3 V decoupling capacitor.
LINEAR CHARGER				
VBAT	18	A1	P	Battery (+) connection point. A typical 1 µF/10 V decoupling capacitor should be connected between VBAT to system ground.
TS	14	C2	I	Battery temperature sensing pin. An external thermistor is connected between TS pin and system ground. If the pin is not used, leave the pin open.
BUCK1 STEP_DOWN CONVERTER (SW1)				
PSYS1	20	A2	P	Input supply for SW1. Bypass with a typical 1 µF/10 V ceramic capacitor. Connect to ASYS power domain as short as possible in the system.
LX1	22	A3	P	Switching node for SW1. Connect to a 2.2 µH inductor. If the pin is not used, leave the pin open.
SW1_OUT	19	B2	I	Feedback pin. Bypass with a 10 µF/6.3 V ceramic capacitor. If the pin is not used, tie to PSYS1.
PGND1	23	A4	P	Power ground for buck 1 (SW1). Connect ground nodes of two bypass capacitors for PSYS1 and SW1_OUT as close to PGND1 pin as possible in the system.
BUCK2 STEP_DOWN CONVERTER (SW2)				
PSYS2	2	C5	P	Input supply for SW2. Bypass with a typical 2.2 µF/10 V ceramic capacitor. Connect to ASYS power domain as short as possible in the system.
LX2	1	B5	P	Switching node for SW2. Connect to a 2.2 µH inductor. If the pin is not used, leave the pin open.
SW2_OUT	3	B4	I	Feedback pin. Bypass with a 10 µF/6.3 V ceramic capacitor. If the pin is not used, tie to PSYS2.
PGND2	24	A5	P	Power ground for buck 2 (SW2). Connect ground nodes of two bypass capacitors for PSYS2 and SW2_OUT as close to PGND2 pin as possible in the system.
LOW_DROPOUT REGULATORS (LDO1 and LDO2)				

Table 3. Pin description...*continued*

Symbol	Pin		Pin Type	Description
	HVQFN24	WLCSP25		
LDO1_OUT	12	E1	P	LDO1 output. It is always-ON supply. The input supply is a higher voltage between ASYS and VBAT_BKUP. Bypass with a 1 µF/6.3 V ceramic capacitor.
LDO2_OUT	15	D1	P	LDO2 output. The input supply is ASYS. Bypass with a 2.2 µF/6.3 V ceramic capacitor.
LOGIC INPUTS				
ON	4	C4	I	ON Pin with an internal pull-up resistor, 1 MΩ typ, to either 2.5 V or VBAT. Refer to Section 8.5 for more details.
MODESEL0	7	E4	I	Mode selection input pin #1. Place a 10 nF/6.3 V capacitor for noise rejection.
MODESEL1	8	E3	I	Mode selection input pin #2. Place a 10 nF/6.3 V capacitor for noise rejection.
LOGIC OUTPUTS				
INTB	10	D4	O	Interrupt output, Open-drain type. Place a pull-up resistor from 20 kΩ to 220 kΩ to a system I/O supply rail.
SYSRSTn	11	D3	O	Reset output for external MCU, Open-drain type. Place a pull-up resistor from 20 kΩ to 220 kΩ to a system I/O supply rail.
SERIAL I^{2}C INTERFACE				
SCL	5	D5	I	I^{2}C Interface clock pin. Place a pull-up resistor between 2.2 kΩ and 10 kΩ to a system I/O supply rail. If the pin is not used, leave the pin open.
SDA	6	E5	I/O	I^{2}C Interface data pin. Place a pull-up resistor between 2.2 kΩ and 10 kΩ to a system I/O supply rail. If the pin is not used, leave the pin open.
DEVICE GROUND				
AGND1	9	B3	P	Analog ground. It shall be connected to system ground through a via. Do not connect AGND1 and AGND2 to PGND1 or PGND2 on the top PCB layer in the system.
AGND2	21	C3	P	
AGND3		E2	P	
	Exposed Pad			Exposed pad. Connect to system ground

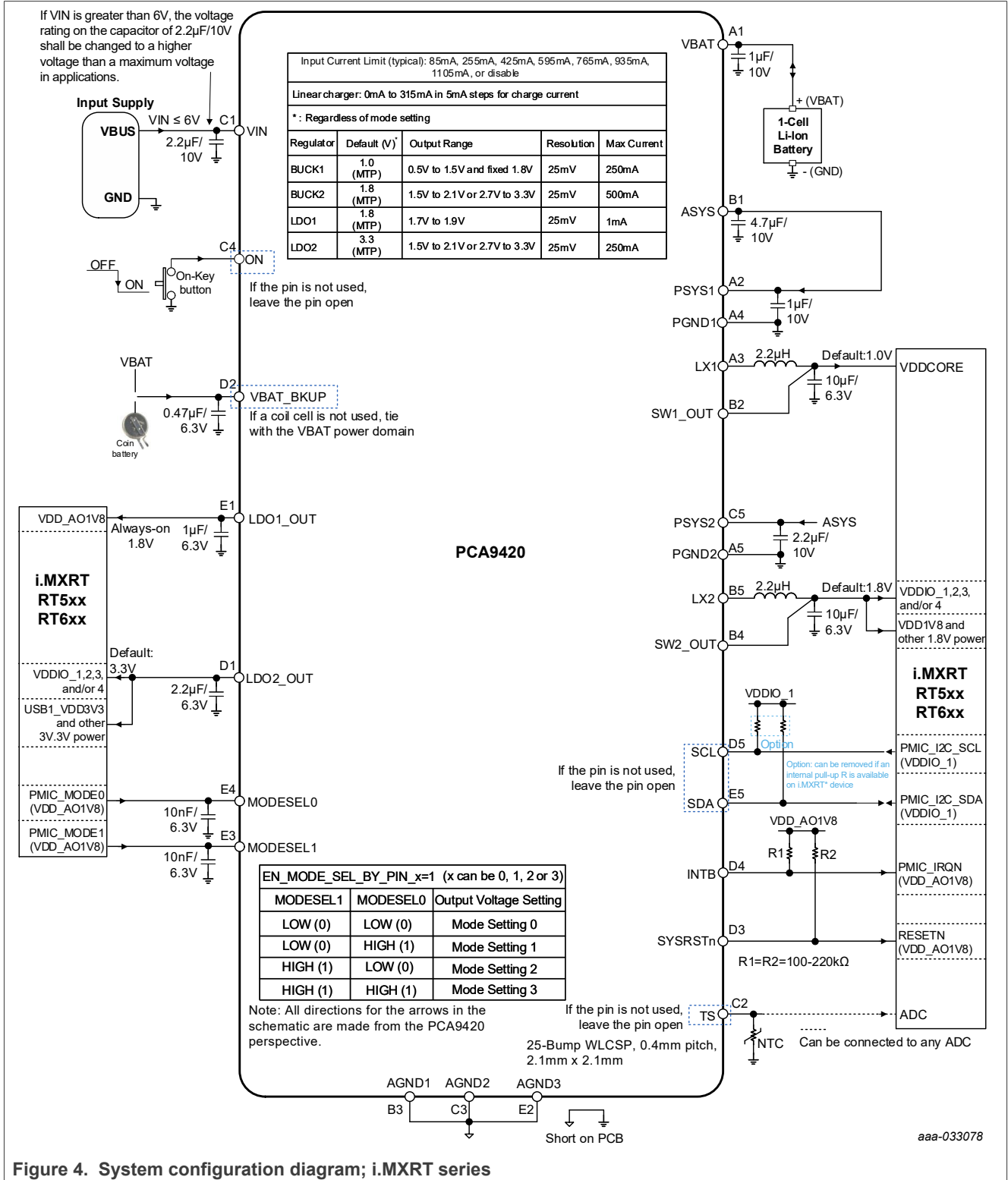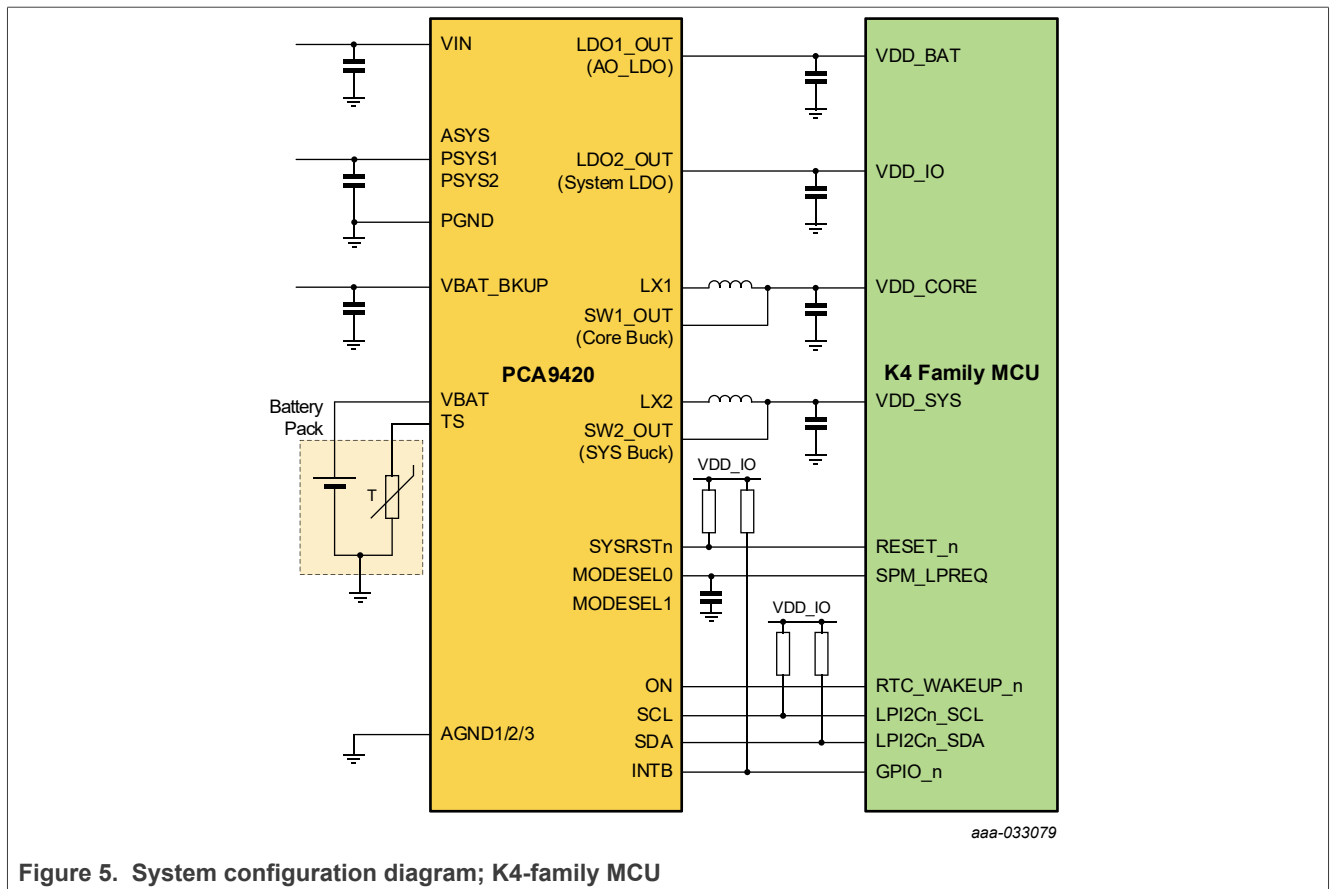P = Power, I = Input, I/O = input/output

7 System configuration diagram

Figure 4. System configuration diagram; i.MXRT series

Input Current Limit (typical): 85mA, 255mA, 425mA, 595mA, 765mA, 935mA, 1105mA, or disable

Linear charger: 0mA to 315mA in 5mA steps for charge current

* : Regardless of mode setting

Regulator	Default (V)*	Output Range	Resolution	Max Current
BUCK1	1.0 (MTP)	0.5V to 1.5V and fixed 1.8V	25mV	250mA
BUCK2	1.8 (MTP)	1.5V to 2.1V or 2.7V to 3.3V	25mV	500mA
LDO1	1.8 (MTP)	1.7V to 1.9V	25mV	1mA
LDO2	3.3 (MTP)	1.5V to 2.1V or 2.7V to 3.3V	25mV	250mA

EN_MODE_SEL_BY_PIN_x=1 (x can be 0, 1, 2 or 3)

MODESEL1	MODESEL0	Output Voltage Setting
LOW (0)	LOW (0)	Mode Setting 0
LOW (0)	HIGH (1)	Mode Setting 1
HIGH (1)	LOW (0)	Mode Setting 2
HIGH (1)	HIGH (1)	Mode Setting 3

Note: All directions for the arrows in the schematic are made from the PCA9420 perspective.

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Figure 5. System configuration diagram; K4-family MCU

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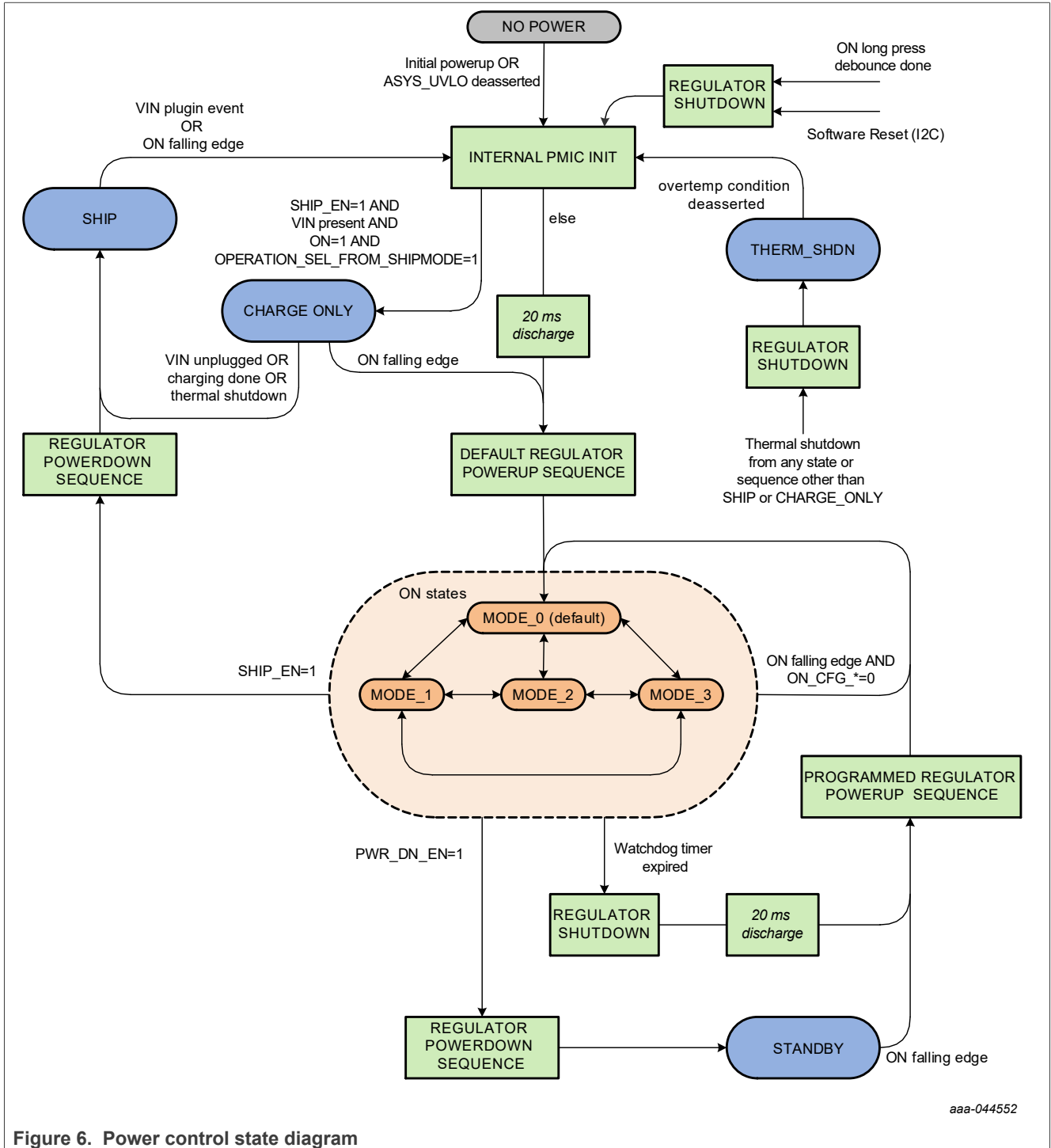# 8 Functional description

8.1 Power control state diagram

Figure 6. Power control state diagram

8.2 VIN

The VIN pin serves as the input power for ASYS and VBAT and has the following functions implemented:

- An I²C undervoltage lockout protection threshold (VIN_UVLO_SEL)
- An I²C programmable input current limiting threshold (falling, VIN_ILIM_SEL [2:0]) which can be disabled. When the VIN_ILIM threshold is reached, the VIN current clamps at that VIN_ILIM_SEL level. This current limiting only applies to VIN
- 20 V tolerance on VIN pin
- An I²C programmable overvoltage protection threshold (rising, VIN_OVP_SEL)

8.2.1 VIN_ILIM and VSYS/VBAT interaction cases

The following describe potential use cases where the behavior of VSYS & the Battery Charger change according to the VIN_ILIM event.

8.2.1.1 Case 0: Battery charger in attach detection sequence & VIN current < VIN_ILIM

The sum of VSYS current (ISYS) and VBAT current (IBAT) in the attach detection sequence is lower than VIN_ILIM current threshold; current clamping does not occur and VSYS voltage follows VIN.

8.2.1.2 Case 1: Battery charger active & VIN current < VIN_LIM

The sum of ISYS and IBAT (battery charging profile ongoing) is lower than VIN_ILIM current threshold; current clamping does not occur and VSYS voltage follows VIN.

8.2.1.3 Case 2: Battery charger active & VIN current increases above VIN_LIM (ISYS < VIN_ILIM)

The sum of an increasing ISYS and IBAT is greater than VIN_ILIM, causing the following events:

- VIN current is clamped to VIN_ILIM while battery charging current continues
- This produces a ramp down in VSYS
- When VSYS is equal to VBAT, charger resets and stops charging.
- The current demand from VSYS is now lower than VIN_ILIM and VSYS is restores to VIN, causing VSYS to rise again. When VSYS > VBAT+100mV, charger automatically restarts from its initial state but may not reach the next charging sequence (pre-charge or fast charge) depending on if the VIN_ILIM threshold is reached. This cycle repeats every 300 ms as described in the battery attached detection sequence.

8.2.1.4 Case 3: Battery charger active & VIN current decreasing below VIN_LIM (ISYS < VIN_ILIM)

With starting conditions from Case 2 now the sum of a decreasing ISYS and IBAT is lower than VIN_ILIM and since VSYS > VBAT+100mV charger automatically restarts from its initial state and goes to the next charging sequence as long as VIN_ILIM is not reached.

8.2.1.5 Case 4: VIN current increasing above VIN_LIM and Battery supplemental mode activation (ISYS > VIN_ILIM)

ISYS current increases until VIN_ILIM is triggered. VIN current is then clamped to VIN_ILIM, producing a ramp down in VSYS. When VSYS < VBAT is reached, a current path from VBAT to VSYS is enabled (Battery supplemental mode activation) to provide the needed current as VIN is limited. PMIC continues to operate this way until ISYS demand drops below VIN_ILIM, and goes back to one of the previous cases.

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8.3 ASYS

The ASYS pin serves as the input power pin for PSYS1, PSYS2 and LDO2. Internally by default it's powered by either VIN or VBAT, whichever is greater. The internal ASYS input selection circuit ensures a seamless transition when its input source changes from VIN to VBAT, or vice versa.

Through I²C register setting selection (ASYS_INPUT_SEL [1:0]), the user also has the option to choose the ASYS input source. However, upon power cycling and/or chip reset, the ASYS input source goes back to the default setting (option 1 below).

SYS_INPUT_SEL [1:0]

1. 2b'00: From either VBAT or VIN, whichever is greater (default setting);
2. 2b'01: From VBAT only;
3. 2b'10: From VIN only;
4. 2b'11: Disconnect from VBAT or VIN (not a normal operation condition, for INTERNAL test purposes only).

An I²C programmable pre-warning ASYS voltage threshold (ASYS_PRE_WARNING [1:0]) can also be used to indicate when ASYS voltage drops below the ASYS pre-warning threshold voltage, which triggers an interrupt event.

If any peripheral regulators are connected to ASYS node, the ASYS node follows a VIN voltage up to a programmed OVP threshold (either 5.5 V or 6 V) with a various voltage difference depending on a load current.

8.4 VBAT_BKUP (back-up battery input)

Internally, the input power source for LDO1 is provided by either VBAT_BKUP or ASYS, whichever is greater. When a coin cell battery (or similar battery) is used in the system as a backup battery, it can be connected to VBAT_BKUP; thus the LDO1 is powered by either ASYS or the backup battery. When no such backup battery is used, the VBAT_BKUP pin should always be connected to VBAT.

8.5 ON

The ON pin has the following functions implemented:

1. ON pin has internal 1 MΩ pullup resistor to either 2.5 V or VBAT depending on VBAT and VIN voltages:
   - When VIN is present (5 V): If VBAT is less than 3.8 V (typical), ON is pulled up to 2.5 V (typical) and if VBAT is greater than 3.8 V (typical), it is pulled to VBAT.
   - When VIN is not present (0 V): ON pin follows VBAT.

Falling edge (filtered after deglitching time, 200 μs typ), active-LOW signal enables the chip and starts the power-up sequence from STANDBY state. If the device is already in the middle of power-up or power-down sequence, the falling edge applied on the ON pin is ignored by the chip.

1. Long press (duration time, 4 s, 8 s, 12 s or 16 s, is programmable via I²C, ON_GLT_LONG [1:0]). If the logic low signal is applied continuously over a programmed duration, the chip gets reset and recycles all power rails to their default values
2. Also, in mode setting 0, 1, 2, or 3, an I²C bit "ON_CFG_x" (x=0, 1, 2, or 3) is reserved; by setting its value to either 0 or 1, the user can configure whether a mode setting switches back to Mode Setting 0 or not, upon a valid falling edge detected from "ON" pin. Refer to ON_CFG_x bit description in the relation registers for more details.
3. The filtered falling edge on the ON pin resets the bit of EN_MODE_SEL_BY_PIN_X to the default value, 0, at 22h register. The status of the ON pin is available in reset monitor register (address 0x71, bit [7]).

8.6 TS

With the temperature sensing pin, the external thermistor (NTC) is connected between the TS pin and ground. The thermistor may be included in the battery pack to monitor the battery pack temperature, or it may be an additional component user chooses to have on the board level to monitor the temperature at a chosen area.

The voltage at TS pin is monitored, and the user can enable the feature through I^{2}C-bus interface (NTC_EN) to implement JEITA compliant charging at a safe temperature. Per JEITA standard, there are four temperature threshold settings:

1. Cold threshold (T1, 0 °C)
2. Cool threshold (T2, 10 °C)
3. Warm threshold (T3, 45 °C)
4. Hot threshold (T4, 60 °C)

Each of the above temperature thresholds represents a voltage threshold. When the monitored temperature, T, falls into a different temperature zone, the charger should adjust the charging method accordingly:

1. T > T4 or T < T1, i.e., when the temperature is in a "cold" or "hot" zone, charging is suspended, as well as the safety timer;
2. T1 < T < T2, charging current is reduced by 50 % of the programmed current level;
3. T2 < T < T3, normal charging;
4. T3 < T < T4, the CV mode regulating voltage should be set as VBAT_REG [5:0] – ΔVBAT_REG(HOT), 140 mV typical

To disable this function, set NTC_EN to "0".

8.7 Mode setting

When the MCU operates in different modes such as overdrive run mode or low power mode, it may require the power supply to operate in different settings accordingly (for example, enable/disable of each rail, output voltage of each rail, etc.) to achieve a better performance and efficiency.

On the PCA9420, there are four modes of registers representing Mode Setting 0/1/2/3 to accommodate such requirements from MCU, where Mode Setting A is the default mode setting (i.e., the initial mode setting upon initial power up). Depending on the user's preference, switching among different mode settings can be controlled by either the external signal (ON pin), external pins (MODESEL0/1) or I^{2}C.

Within each mode setting, the user can program the follow parameters providing great flexibility to accommodate different MCU operation modes:

1. Enable/disable of the four output voltage rails
2. Voltage setting of the four output voltage rails
3. Ship mode enable/disable
4. Watchdog timer setting
5. Mode control selection (EN_MODE_SEL_BY_PIN_x, x=0, 1, 2, or 3)

EN_MODE_SEL_BY_PIN_x = 0: under current mode setting, mode setting switch is controlled by internal I^{2}C register bits MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored.

EN_MODE_SEL_BY_PIN_x = 1: under current mode setting, mode setting switch is controlled by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^{2}C register bits MODE0_I2C and MODE1_I2C.

1. Mode setting switches back to Mode Setting A triggered by ON pin falling edge. Refer to register description for "ON_CFG_x" bit for more details.

In the event of switching from one mode setting (initial mode setting) to another mode setting (target mode setting):

1. If one output rail remains enabled in both initial mode setting and target mode setting but with different output voltage in each setting, such voltage transition should happen when the mode setting switch command (from either internal I^{2}C setting or external signal) is received;

2. If there are output rails which may be enabled or disabled from initial mode setting to target mode setting, then always make sure these rails which change from disabled to enabled take higher priority over rails which change from enabled to disabled, i.e., make sure all the rails change from disabled status to enabled status (reaches 90 % of its target value) first, and then start to disable these rails, changing from enable status to disable status.

8.8 Mode selection by external pins (MODESEL0, MODESEL1)

Up on initial power-up, PCA9420 enters its default setting (Mode Setting 0). While operating under Mode Setting 0, by default the I^{2}C register bit, EN_MODE_SEL_BY_PIN_0, is set to "0", and the external signal applied on the MODESEL0 and MODESEL1 pins are ignored. Only when the user sets EN_MODE_SEL_BY_PIN_0 to "1", can the mode control on the chip be programmed via MODESEL0 and MODESEL1 pin signal settings. The MODESEL0 and MODESEL1 pins are not allowed to change while a mode change is in progress.

When EN_MODE_SEL_BY_PIN_x (x=0, 1, 2, or 3) bits are set to "1", MCU should satisfy the following MODESEL signal conditions:

• No less than 5 μs pulse on each MODESEL signal.

• No more than 0.5 μs delay between MODESEL pins when transit from different modes.

In order to avoid impacting mode transition when there is disturbance in MODESELS pins (EN_MODE_SEL_BY_PIN_x =1), it is proposed to implement one of the following designs:

• Hardware: Adding 10 nF capacitors to remove noise injection on MODESEL pins.

• Software: Send software reset command after wake up from ship mode to reset MODESEL pins. (There is a register 0x71, accessible by I^{2}C; SHIP_EXIT_DONE status indicates device wake up from ship mode, refer to Table 76.)

Table 4. Mode selection by external pins (MODESEL0, MODESEL1)

MODESEL1 pin voltage level	MODESEL0 pin voltage level	All Settings from
LOW (0)	LOW (0)	Mode Setting 0
LOW (0)	HIGH (1)	Mode Setting 1
HIGH (1)	LOW (0)	Mode Setting 2
HIGH (1)	HIGH (1)	Mode Setting 3

8.9 SYSRSTn

The SYSRSTn is implemented as an open-drain output signal. It is used as an output of "power-good" indication as well as to reset the microcontroller system.

The SYSRSTn signal is held from high to low under one of following conditions:

1. When any of the *enabled* voltage rail output voltage drops below 90 % (typ) of its target value.

2. When any of the *enabled* voltage rail output voltage goes above 110 % (typ) of its target value

If any of the voltage rail is disabled by the user (by setting the corresponding enable bit in I^{2}C register in each mode setting, i.e., LDO1_EN_x, LDO2_EN_x, SW1_EN_x, SW2_EN_x), the SYSRSTn signal should NOT assert (stays high) under such scenario.

This also applies during the power-up/power-down sequence events, i.e., during power- up or power-down event, the SYSRSTn signal should assert when any of the enabled rail has not reaches the 90 % to 110 % of its target value. In other words, the SYSRSTn = 0 (low) needs to remain at such state until all enabled rails reach 90 % of the target values.

Once the condition that caused the SYSRSTn signal to go low is removed, then the SYSRSTn should refresh accordingly.

Meanwhile, during the voltage change on-the-fly, this could be caused by:

1. Mode setting remains the same, but the user chooses to change one or some of the enabled output rail voltage by programming its output voltage I^2C register setting
2. Mode setting changes by setting different values on MODESEL0/MODESEL1 pins or MODE0_I2C/ MODE1_I2C bits, and it causes one or some of the output rail voltage change

In such case, the SYSRSTn signal does NOT assert when any of the ***enabled*** voltage rail output voltage is in the middle of the transition from initial output voltage level to target level.

8.10 SHIP mode

PCA9420 features a "SHIP mode", in which the chip provides the lowest quiescent consumption. Ship mode is designed to operate only from VBAT. Ship mode should not be entered when both VIN and VBAT are present.

To enter the SHIP mode, set the bit of SHIP_EN_x (x can be 0, 1, 2 or 3) in each Mode register to 1. Once the bit is set to 1, the ship mode immediately takes place regardless of any operation under any mode setting. It means that the SHIP mode has a higher priority over any conditions and operations.

Upon request to enter the ship mode while the device is running in active mode, a power-down sequence should take place first and then enter the ship mode. **Once the device enters ship mode, all the I^2C register values are reset to their default setting.**

To exit ship mode, one of the following conditions must be satisfied:

1. ON pin falling edge (filtered) applied, less than the long-press duration of time
2. A valid VIN attached. For the VIN attached plugin event, depending on OPERATION_SEL_FROM_SHIPMODE bit setting, there are two possible operations as described below:
   a. OPERATION_SEL_FROM_SHIPMODE=0, upon VIN attached, the chip enables the charging process, as well as start the power-up sequence for LDO1/LDO2/SW1/SW2 per the setting
   b. OPERATION_SEL_FROM_SHIPMODE=1, upon VIN attached, the chip enables the charging process, LDO1/LDO2/SW1/SW2 remains in shutdown mode and the chip enables only the power-up sequence upon ON pin falling edge signal.

8.11 Watchdog timer

PCA9420 provides an on-chip watchdog timer, the duration of this watchdog can be programmed via I^2C register setting (WD_TIMER_x [1:0] in each mode configuration registers), or disabled if needed in each mode setting.

Upon initial enable, the watchdog timer starts counting. If the watchdog timer expires before reset, an interrupt signal is issued (WD_TIMER). Depending on the I^2C register setting (nEN_CHG_IN_WATCHDOG), the following action is also taken:

1. nEN_CHG_IN_WATCHDOG = 0: when the watchdog timer expires, the following operations are expected.
   • The SYSRSTn signal asserted (high to low)
   • Charging is continued based on battery condition

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- All settings for LDO1/LDO2/SW1/SW2 set to Mode 0 settings
2. nEN_CHG_IN_WATCHDOG=1: when the watchdog timer expires, the following operations are expected.
   - The SYSRSTn signal asserted (high to low)
   - Charging is suspended
   - All settings for LDO1/LDO2/SW1/SW2 set to Mode 0 settings

The following events reset the watchdog timer:

1. When WD_TIMER_CLR bit is set to 3b'001 at 0Dh register
2. When the device changes the mode settings

8.12 Regulators

There are four regulators on PCA9420, which include two buck regulators and two LDOs. Table 5 shows the outline for each regulator:

Table 5. Regulator summary

Regulator name	Output regulation voltage range	Adjustable resolution	Max output current
SW1 (Core Buck)	0.5 V to 1.5 V and a fixed 1.8 V	25 mV/step	Up to 250 mA
SW2 (System Buck)	1.5 V to 2.1 V or 2.7 V to 3.3 V	25 mV/step	Up to 500 mA
LDO1 (Always-on LDO)	1.7 V to 1.9 V	25 mV/step	Up to 1 mA
LDO2 (System LDO)	1.5 V to 2.1 V or 2.7 V to 3.3 V	25 mV/step	Up to 250 mA

For each rail, its output target voltage can be set independently in mode setting 0, 1, 2 or 3. User can also choose to switch among any of the mode settings.

8.12.1 Enable/disable and active discharge

Enable/disable: Each rail can be enabled/disabled via I^2C register setting independently in each mode setting.

Active discharge: Additionally, there is an active discharge resistor on each rail, and the user can choose to enable/disable such feature through I^2C register setting, so that when the output rail is disabled, it can quickly discharge the output voltage to ground. In addition, the active discharge is also enabled during voltage step down. This can be disabled by MTP bit.

If the active discharge bleeding resistor is enabled AND there is a change of the Buck regulators' output voltage to a lower value (i.e. from 0.9 V to 0.75 V) there could be a small voltage peak of 5 % higher than the initial voltage (for 10 μs) during the transition. If this behavior is not desired, the bleeding resistor can be disabled (nEN_SW1_BLEED = 1 or nEN_SW2_BLEED = 1) but with the effect of a potentially longer transition to the new voltage of the buck regulator output

8.12.2 Power-good indication

There is an output voltage comparator for each rail, comparing the actual output voltage against 90 % and 110 % of its target value; when the actual voltage is between 90 % and 110 % of its target value, the read-only related bits in I^2C register, Regulator Status_1 (address: 20h) are updated accordingly to report the output voltage status (Power-good Indication). These comparators can be enabled/disabled by setting I^2C register bit, PG_EN. A corresponding interrupt is triggered if unmasked. During steady state, only 90 % threshold is monitored.

The power-good indication is shown as "not good", and refreshes upon the completion of any of the following events:

1. During the power-up sequence stage

2. During power-down sequence stage
3. During the on-the-fly change of output voltage

8.12.3 Power-up/down sequence and on-the-fly voltage change

Power-up sequence

The device initiates the default power-up sequence in three different conditions.

Condition 1) The device is off with no any power supply (No valid VIN and No battery with 2.7 V or above attached). In this condition, two signals below are able to start the default power-up sequence.

• A valid VIN supply on VIN pin
• A voltage on ASYS higher than ASYS_UVLO, a 2.8 V typical

Condition 2) The device stays off by enabling SHIPMODE or in SHIP mode with a battery ≥ 2.8 V attached. In this condition, two signals are able to start the default power-up sequence.

• A valid VIN supply on VIN pin
• A falling edge on ON key over a 200 µs

Condition 3) The device stays off by enabling PWR_DN_EN bit setting to 1 with a battery ≥ 2.8 V attached. In this condition, only one signal is able to start the default power-up sequence.

• A falling edge on ON key over a 200 µs

Condition 4) The device stays at VIN OVP condition with no any valid supply attached at VBAT. In result, all enabled power rails have been off. The following condition re-initiates the power-up sequence.

• The VIN goes below its VIN OVP hysteresis (typ 100 mV)

The power-up sequence by ON key=Low over the debounce time is described as shown in Figure 7.

For the power-up sequence, the chip can set the default sequence per the customer requirement at factory setting (i.e. MTP option), from one of the 64 options. Once the chip enters the power-down stage, the power-down sequence is implemented as the reverse of the power-up sequence (i.e., first up, last down).
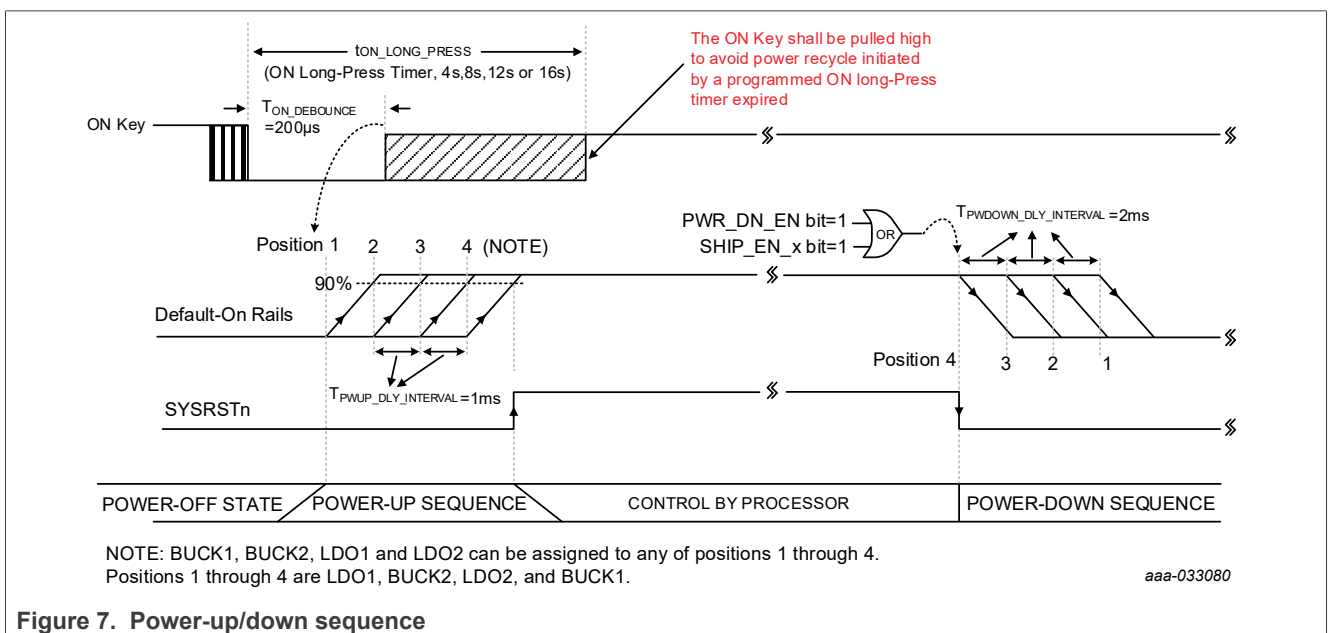

NOTE: BUCK1, BUCK2, LDO1 and LDO2 can be assigned to any of positions 1 through 4.
Positions 1 through 4 are LDO1, BUCK2, LDO2, and BUCK1.

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Figure 7. Power-up/down sequence

On-the-fly output voltage change sequence

On-the-fly output voltage change is defined as the following: for any output rail, its output voltage changes from one level (initial level) to another level (target level). Note this assumes the output rail is always enabled before and after the on-the-fly change transition. It does not include the case when any output rail is changed from disabled state to enabled state, or vice versa.

If a user prefers to change any rail voltage on-the-fly, depending on the scenarios listed below, the chip behavior is described as follows:

1. While the chip remains in its current operation mode, and the user programs the output voltage setting I^2C register value or enables/disables any or some of output voltage rail(s), the chip simply executes the I^2C command

2. While the user chooses to switch modes, i.e. change mode between any of the two mode settings among Mode 0/1/2/3, and if this involves on-the-fly voltage change for one or some output rails, such change should occur simultaneously when the chip switches from initial mode to the target mode.

CAUTION: The user should not send an I^2C command related to changing the setting of the output rails during the power up/down or mode setting change process.

8.12.4 BUCK1 (SW1, core buck regulator)

The SW1 supplies the core power.

Its output voltage can be programmed via I^2C from 0.5 V to 1.5 V at 25 mV step and a fixed 1.8 V, which is capable of providing up to 250 mA loading. The application circuit uses typical 2.2 µH inductor and 10 µF/6.3 V output capacitor.

8.12.5 BUCK2 (SW2, system buck regulator)

The SW2 output voltage can be programmed via I^2C register from 1.5 V to 2.1 V, or from 2.7 V to 3.3 V in both at 25 mV/step and is capable of providing up to 500 mA loading. The application circuit uses a 2.2 µH inductor and 10 µF output capacitor.

In SW2, a pass-through mode is implemented. When its input (ASYS) is close to the output voltage (within typical 200 mV), the SW2 enters the pass-through mode operation; the high-side switch is fully turned on and the low-side switch is turned off, and the output voltage can be calculated as input voltage – (RDSON*I_{LOAD}), where RDSON is the on-resistance of the high-side switch, and the I_{LOAD} refers to the load current. When the input voltage rises again, so that the voltage different between input and output crosses the typical 250 mV threshold, the SW2 exits the pass-through mode and re- enters the normal switching mode operation.

While SW2 operates in pass-through mode, protection features such as over-current protection are also implemented as well.
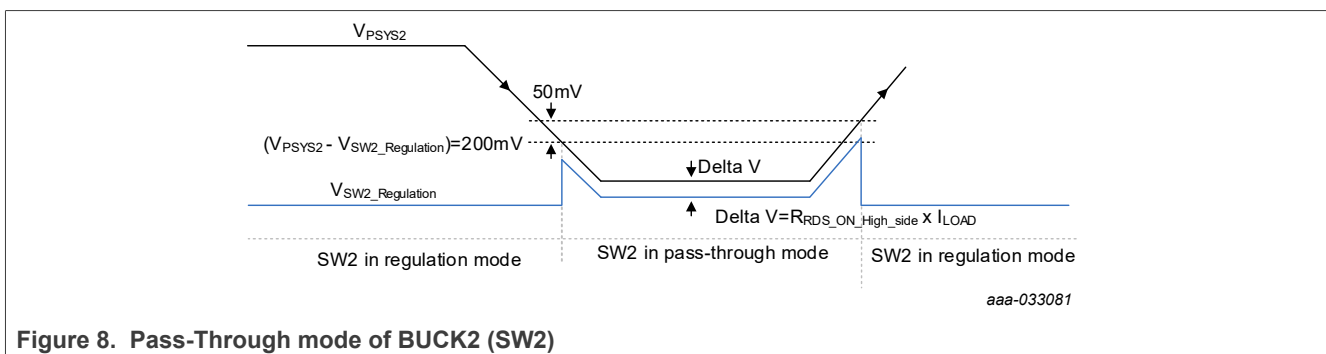

Figure 8. Pass-Through mode of BUCK2 (SW2)

8.12.6 LDO1 (always-on LDO)

The LDO1 (Always-on LDO) output can be programmed from 1.7 V to 1.9 V at 25 mV step, depending on the system requirements (selectable through I^{2}C register). Typically, a 1 µF/6.3 V MLCC output capacitor providing at least 1 mA loading capability is needed.

LDO1 operates based on the principle of hysteretic on/off regulation. The LDO1 output voltage is generated from a frequent activation/deactivation of the output stage connecting VBAT to the LDO1 output depending on the programmed output voltage for LDO1. The ripple frequency and amplitude are dependent on the load current and external capacitance. The greater the load current, the higher the on/off activation of this output stage to ensure LDO1 stays within the defined output voltage accuracy specified in the electrical specification section. LDO1 is powered by the greater of ASYS or VBAT_BKUP.

SW_RST event does not shut down LDO1, but sets LDO1 to default value. Watchdog Reset does not shut down LDO1, but changes LDO1 to Mode 0 setting. SHIP mode/ Hardware Reset (ON Long Press) shuts down LDO1 and recycles power up to default output voltage.

8.12.7 LDO2 (system LDO)

The LDO2 (system LDO) output can be programmed via the I^{2}C register from 1.5 V to 2.1 V, or 2.7 V to 3.3 V at 25 mV/step. Typically, a 2.2 µF/6.3 V MLCC output capacitor providing at least 250 mA loading current is needed.

8.13 Linear battery charger

The battery charger is a linear charger. Its charging is done through a linear switch with the following output protections:

- If VIN is not present and ASYS is supplied by VBAT, there is no current limiting on that power path
- Reverse current protection
  - (triggers when ASYS < VBAT+ VINBAT_HEADROOM*)
- JEITA compliant charging current limiting
  - (a function of programmed threshold and battery temperature)
- VBAT short circuit protection
  - Short circuit output voltage threshold: (typ 0.8 V with 80 mV hysteresis)
  - Maximum output sourcing current during "short circuit" detection ~ 13 mA (VIN2BAT_HEADROOM = 100 mV, typical)

If the battery voltage is below the V_{BAT_LOW} threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of pre-charge current (ICHG_LOW) can be programmed through I^{2}C register setting. This feature is useful when there is a load connected directly across the battery (at VBAT pin) "stealing" the battery current. The pre-charge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. Once the battery voltage has charged to the V_{BAT_LOW} threshold, fast charge is initiated and a programmed fast charge current (I_{CHG_CC}) is applied. The fast charge constant current is programmed using I^{2}C register. The constant current provides the bulk of the charge. Power dissipation in the device is greatest in fast charge with a lower battery voltage.

If the device reaches a programmed thermal regulation threshold temperature (defined by the configuration on the THM_REG bit fields on the CHG_CNTL7 register) from 85 °C to 115 °C in 5 °C steps, the device enters thermal regulation. This is indicated by the TREG_STATUS bit field on the CHG_STATUS_1 register. Thermal regulation increases the safe-charging-timer period by 2x and reduces the charge current in half (if the initial current is 5 mA, it remains unchanged) to keep the temperature from rising any further when battery charger works in constant current charging mode, or at a reduced regulated voltage when battery charger works in constant voltage charging mode.

Figure 9 shows the charging profile with a dead battery condition. Once the cell has charged to the regulation voltage (V_{BAT_REG}) the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold (I_{CHG_TOPOFF}).

CHG_LOCK [4:0] bits on Battery charger control_0 (CHG_CTL0, address 10h) register should be set to '10101' to be able to perform I^{2}C "write" command. Otherwise, when "write" command is performed on the 'locked registers', it keeps the present register value.

8.13.1 Battery charging management

Battery charging management supports typical constant current/constant voltage charging profile for single cell Li-Ion battery, as well as pre-qualification (dead battery, low battery), top-off mode, etc.; JEITA and thermal regulation compliant.

In PCA9420, there is an initial stage in the charger operation which sources I_{CHG_DEAD} current into VBAT and compares the voltage to 1.9 V level.

- If the voltage is higher than this threshold, the charger immediately proceeds to the next state (pre-charge/ I_{CHG_LOW} current).
- Otherwise, there is a timer running for 5...40s (I^{2}C programmable) called ICHG_DEAD_TIMER, bits [7:6] in register 0x14 chg_ctl4. If the timer expires, the battery doesn't accept charge and is detected as a short.

ICHG_DEAD_CURRENT is sourced by the charger and is I^{2}C programmable.

The dead charge fault timer can assert an interrupt (bit [6] (ICHG_DEAD_TIMER_INT_MASK) from Sub_INT1_Mask register 05h), and the software can make the final decision. If left masked, the charger always proceeds to the next stage. This is the default PCA9420 operation. If the interrupt was enabled and has triggered, the charger is disabled.
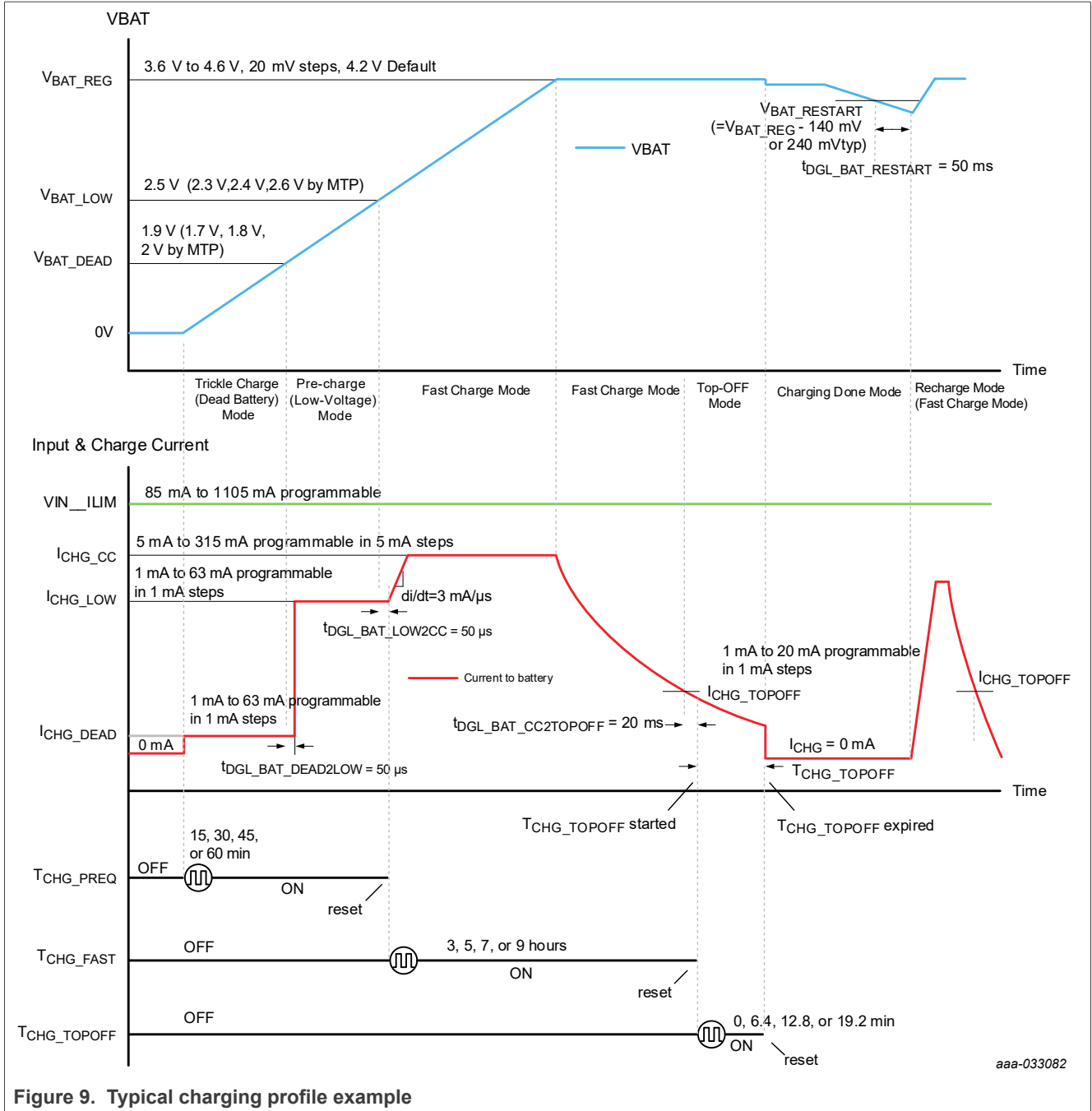
Figure 9. Typical charging profile example

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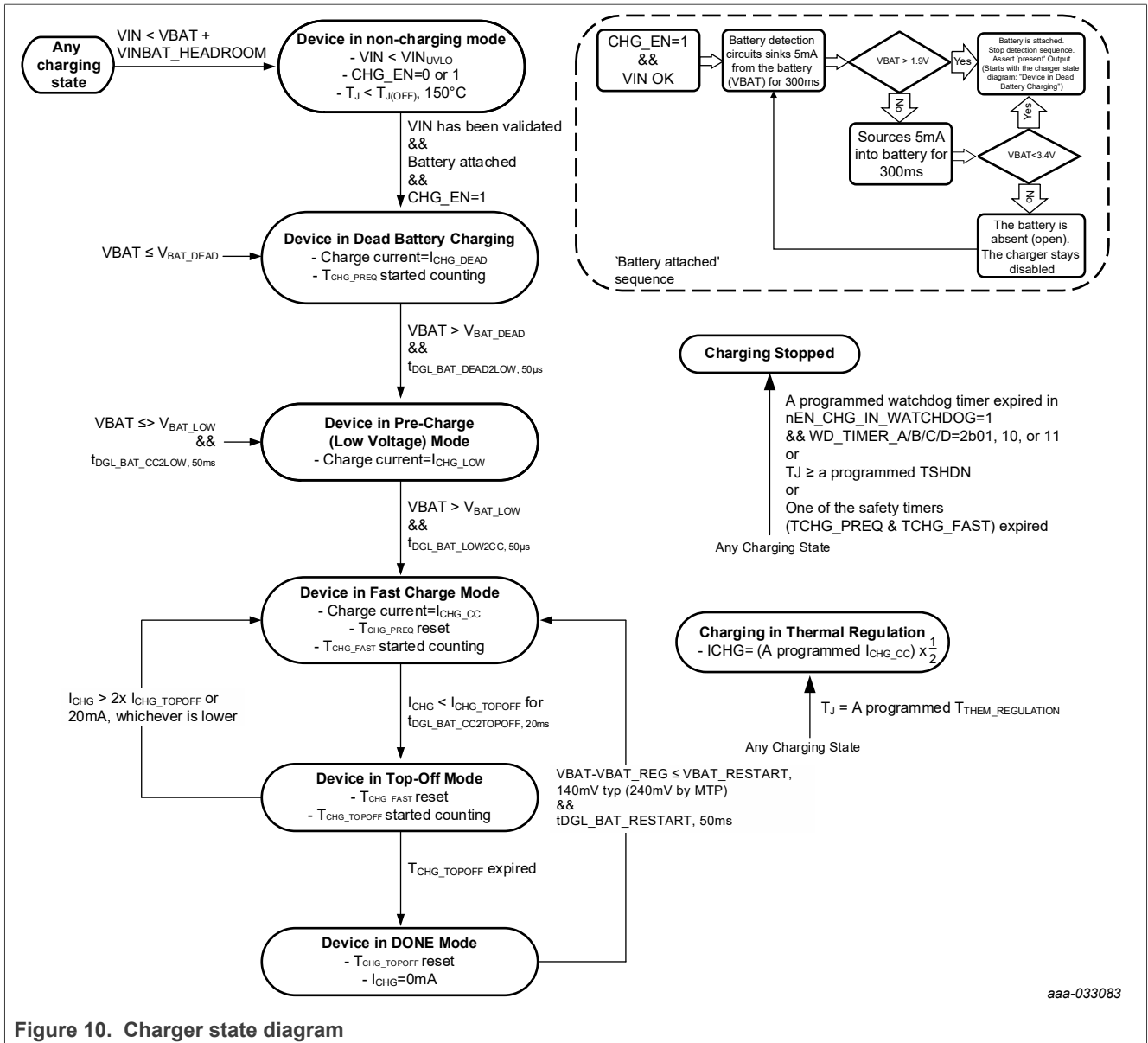
Figure 10. Charger state diagram

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8.13.2 Battery temperature sensing and JEITA-compliant charging profile

Figure 11. Operation over TS bias voltage for JEITA
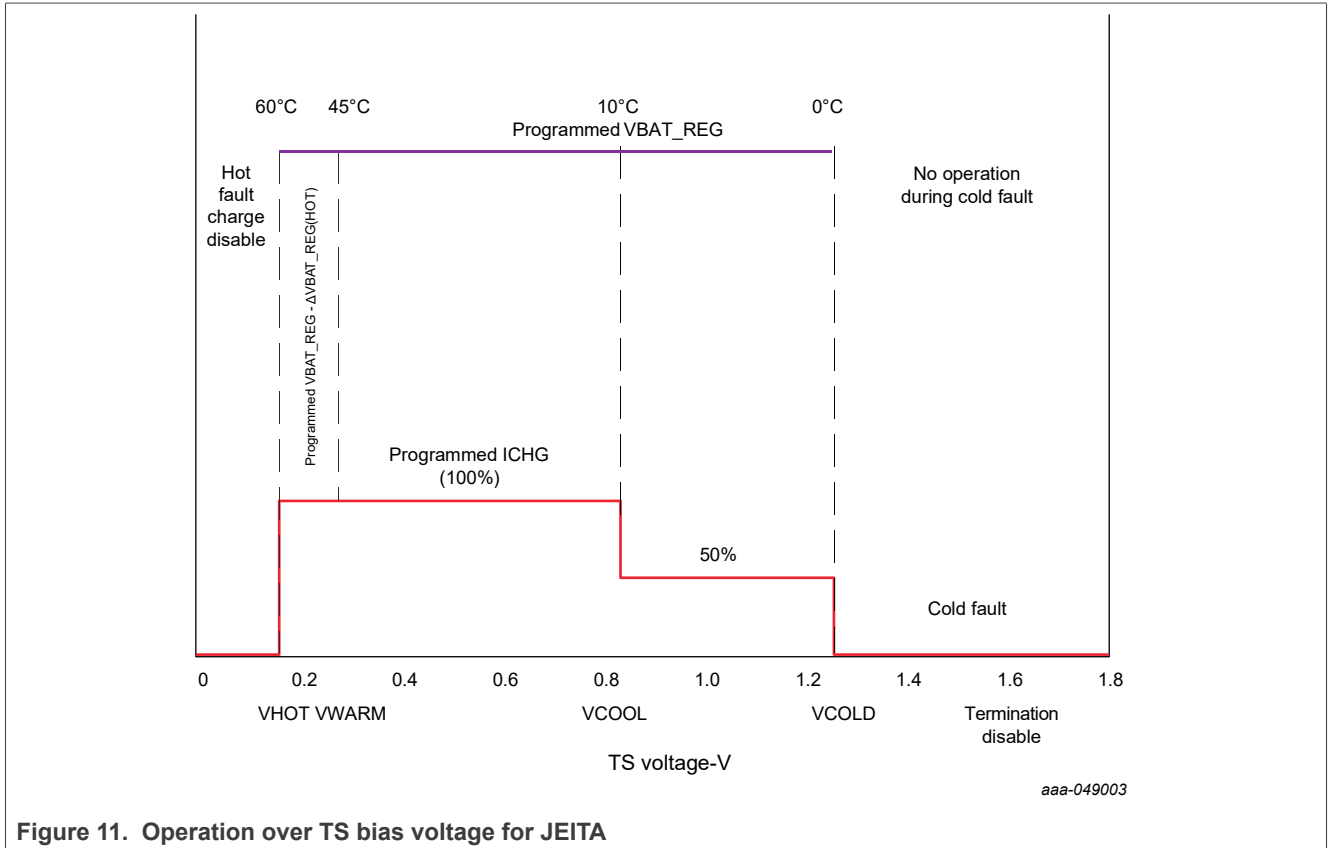
Please refer to Section 8.6 for more details

8.13.3 Battery attach detection

The device has a unique battery detection scheme with two comparators, 1.9 V and 3.4 V. When the detection scheme is executed, a 5 mA current sink is activated to determine battery presence by detecting the fall threshold, $V_{BAT\_DET\_LOW}$, 1.9 V typ. In addition, a 5 mA current source is used to detect battery voltage whether it stays above the threshold, $V_{BAT\_DET\_UP}$, 3.4 V. If both conditions are met, absence of battery is declared.

Battery detection sequence steps:

1. VBAT Sources 5 mA current to the PMIC Battery Detection Circuit.
2. If VBAT voltage is above 1.9 V, the battery is present. Stop the detect sequence, assert the "present" output.
3. Else if VBAT voltage is below 1.9 V, source 5 mA from PMIC into VBAT pin.
4. If VBAT voltage is below 3.4 V, the battery is present. Stop the detect sequence, assert the "present" output.
5. Else if VBAT voltage is above 3.4 V, the battery is absent (open). The charger stays disabled.
   NOTE: The battery detect source and sink are separate dedicated circuits; 5 mA is a constant, not programmable. The reset source is recorded on the "Reset monitor" register (address 0x71h)

For more details, see Figure 10.

8.13.4 Low-battery/dead-battery (pre-qualification) charging

If the battery is detected and VBAT < VBAT_LOW, the charger initiates pre-charging using a predefined (I^2C register) current.

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When it is under the dead-battery condition, the charging current I_{CHG_DEAD} is programmed by ICHG_DEAD [5:0]; and when it is under the low-battery condition, the charging current I_{CHG_LOW} is programmed by ICHG_LOW [5:0]. When $V_{BAT} \geq V_{BAT\_LOW}$, the charger moves to the next state, fast charging mode.

8.13.5 Constant current charging/constant voltage charging (fast charging) and termination

When $V_{BAT} \geq V_{BAT\_LOW}$, the charger enters Fast Charge Mode (Constant Current). In this state, the battery voltage VBAT continues to rise, while the battery is being charged with the current set by ICHG_CC [5:0], until VBAT reaches the maximum allowable voltage set by VBAT_REG [5:0].

At this time, the charger enters the Constant Voltage (CV) mode. While operating in the CV mode, the voltage is still regulated at the level set by VBAT_REG [5:0], and the charging current continues to decrease.

When the charging current drops below the top-off current threshold, set by ICHG_TOPOFF [5:0], the charger enters TOPOFF mode, and upon expiration of TOPOFF timer (set by T_TOPOFF [1:0]), the charger enters DONE mode.

8.13.6 Charger safety timers

Two sets of charging safety timers are implemented on PCA9420. These timers ensure the charging is terminated if the charging time is longer than its predefined limit (programmed via I^2C registers) at given states:

- Pre-qualification timer, set by ICHG_PREQ_TIMER [1:0], 15 min to 60 min
- Fast charge timer, set by ICHG_FAST_TIMER [1:0], 3 hr to 9 hr

8.13.7 Recharging

While in DONE mode, if the voltage of VBAT stays below (a programmed VBAT_REG – 140 mV or 240 mV) over the deglitch time ($t_{DGL\_BAT\_RESTART}$), 50 ms the battery charger resumes back to Constant Current (CC) Mode.

8.13.8 Starting a new charge cycle

When a VIN plug in, VBAT attached, or CHG_EN are set to "1", the device initializes a new charging process.

8.14 Hardware and software reset

Please refer to description for ON pin for the hardware reset function by a long time ON key pressed. The "software reset" is achieved by setting "1" to SW_RST bit in I^2C register. If the user writes a "1" to this bit, it resets all other I^2C register bits to their default setting; this bit is cleared and reset back to "0" as well.

8.15 Device level protection features

The device contains several protection features at both the complete IC level and have a reaction at each of the functional blocks (linear charger, DC-DC converters, LDOs). There are additional protection mechanisms at the functional block level, but those are already documented on its respective functional description section.

Table 6. Device level protection features

Condition	Triggering point	Protection reaction				
		Overall Device state	**Linear charger**	**DC-DC converters**	**LDOs**	**Register contents**
VIN undervoltage	VIN < VIN_UVLO	Operational	Disabled	Remain operational although might deliver a reduced output voltage (due to low VIN)	Remain operational although might deliver a reduced output voltage (due to low VIN)	Maintained. Interrupt triggered, status reported.
VIN overcurrent (ILIM)	VIN current is > VIN_ILIM	Limit input current to VIN_ILIM setting	Remain operational	Remain operational	Remain operational	Maintained unless reset happened; Interrupt and status reported.

Table 6. Device level protection features...*continued*

Condition	Triggering point	Protection reaction				
		Overall Device state	**Linear charger**	**DC-DC converters**	**LDOs**	**Register contents**
ASYS undervoltage	ASYS < ASYS_UVLO	RESET	RESET state if ASYS < VINBAT_HEADROOM	Turned off, restarted in initial state when condition goes away	Turned off, restarted in initial state when condition goes away	Reset to their default value
IC overtemperature	Chip temperature > THM_REG	RESET	RESET state	Turned off, restarted in initial state when condition goes away	Turned off , restarted in initial state when condition goes away	Reset to their default value. Status available in register 0x71.
Watchdog timer expiration	Watchdog counter > WD_Timer_0 setting	Operational	Depends on the value of n EN_CHG_IN_WATCHDOG bit	Set to mode 0	Set to mode 0	Maintained. Status available in register 0x71.

9 I^{2}C-bus interface and register

The PCA9420 implements an I^{2}C-bus target interface to communicate with the host system. The interface supports Fast Mode plus Fm+ with up to 1 Mbit/s. A detailed description of the I^{2}C-bus specification is given in [UM10204, Rev. 06, 4 April 2014](#) ," I^{2}C-bus specification and user manual".

Features such as clock-stretching and 10-bit target address are not supported; general call is supported by default but can be disabled via metal option. Auto increment with address wrap-around is supported as well.

9.1 I^{2}C target address

Following a START condition, the bus controller must send the target address followed by a read or write operation. The target address of the PCA9420 is shown below:

Table 7. I^{2}C target address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	0	0	1	0/1
Fixed	Fixed	Fixed	MTP option	Fixed	Fixed	Fixed	R/W

Bit 4 should be reserved as MTP option, with its default value set as "0" but can be trimmed to "1" when needed.

9.2 General call and device ID addresses

The device implements two different addresses for general call and device ID.

9.3 Register type

There are four register types used on the device:

- Read and Write (R/W)
- Read Only (R)
- Write Only (W)
- Write and Clear (W/C)

For Write and Clear (W/C), a write to a register with a bit-mask specifies which interrupts to clear.

For example, if the status register shows 8'b0000_1001 as an interrupt status (i.e. interrupt [0] and interrupt [3] are both set), user may write 8'b0000_1000, meaning the intent is to only clear interrupt [3] (but interrupt [0] should NOT be "cleared"). If the intent is to clear both interrupts, then the user could write back 8'b0000_1001.

9.4 Register map

Table 8. Register map

Address (Hex)	Register Name	Description	Type	Reset Value (Binary)
System Control Registers				
00	Device Information, DEV_INFO	Device ID, revision	R	0000 0001
01	Top Level Interrupt Status, TOP_INT	Top level interrupt event status	R/C	0000 0000
02	Sub Level Interrupt_0, SUB_INT0	Sub-level interrupt indication_0	W/C	0000 0000
03	Sub Level Interrupt_0 Mask, SUB_INT0_ MASK	Sub-level interrupt mask for SUB_INT0	R/W	0011 1111
04	Sub Level Interrupt_1, SUB_INT1	Sub-level interrupt indication_1	W/C	0000 0000
05	Sub Level Interrupt_1 Mask, SUB_INT1_ MASK	Sub-level interrupt mask for SUB_INT1	R/W	0111 1111
06	Sub Level Interrupt_2, SUB_INT2	Sub-level interrupt indication_2	W/C	0000 0000
07	Sub Level Interrupt_2 Mask, SUB_INT2_ MASK	Sub-level interrupt mask for SUB_INT2	R/W	1111 1111
08	RSVD	Reserved	R/W	0000 0000
09	Top Level Control_0, TOP_CNTL0	Top level system control_0	R/W	0100 0001
0A	Top Level Control_1, TOP_CNTL1	Top level system control_1	R/W	1000 1001
0B	Top Level Control_2, TOP_CNTL2	Top level system control_2	R/W	1100 1110
0C	Top Level Control_3, TOP_CNTL3	Top level system control_3	R/W	0000 0001
0D	Top Level Control_4, TOP_CNTL4	Top level system control_4	W	0000 0000
0E – 0F	RSVD	Reserved		
Battery Charger Control				
10	Battery Charger Control_0, CHG_CNTL0	Battery charger control register_0	R/W	0000 0011
11	Battery Charger Control_1, CHG_CNTL1	Battery charger control register_1	R/W	0000 1000
12	Battery Charger Control_2, CHG_CNTL2	Battery charger control register_2	R/W	0000 0100
13	Battery Charger Control_3, CHG_CNTL3	Battery charger control register_3	R/W	0000 1000
14	Battery Charger Control_4, CHG_CNTL4	Battery charger control register_4	R/W	0000 0100
15	Battery Charger Control_5, CHG_CNTL5	Battery charger control register_5	R/W	0001 1110
16	Battery Charger Control_6, CHG_CNTL6	Battery charger control register_6	R/W	1001 0101
17	Battery Charger Control_7, CHG_CNTL7	Battery charger control register_7	R/W	0010 0100
18	Battery Charger Status_0, CHG_ STATUS_0	Battery charger status indication_0	R	0001 0000
19	Battery Charger Status_1, CHG_ STATUS_1	Battery charger status indication_1	R	0000 0000
1A	Battery Charger Status_2, CHG_ STATUS_2	Battery charger status indication_2	R	0111 1000
1B	Battery Charger Status_3, CHG_ STATUS_3	Battery charger status indication_3	R	0000 0000
1C – 1F	RSVD	Reserved		
Regulator Control				
20	Regulator Status, REG_STATUS	Regulators status indication	R	0000 0000
21	Active Discharge Control, ACT_ DISCHARGE_CNTL_1	Active Discharge control register	R/W	0000 0000

Table 8. Register map...*continued*

Address (Hex)	Register Name	Description	Type	Reset Value (Binary)
22	Mode Configuration Mode Setting 0_0, MODECFG_0_0	Mode configuration settings for Mode 0_0	R/W	0001 0100
23	Mode Configuration Mode Setting 0_1, MODECFG_0_1	Mode configuration settings for Mode 0_1	R/W	0000 1100
24	Mode Configuration Mode Setting 0_2, MODECFG_0_2	Mode configuration settings for Mode 0_2	R/W	0100 1111
25	Mode Configuration Mode Setting 0_3, MODECFG_0_3	Mode configuration settings for Mode 0_3	R/W	0011 1001
26	Mode Configuration Mode Setting 1_0, MODECFG_1_0	Mode configuration settings for Mode 1_0	R/W	0001 1100
27	Mode Configuration Mode Setting 1_1, MODECFG_1_1	Mode configuration settings for Mode 1_1	R/W	0100 1100
28	Mode Configuration Mode Setting 1_2, MODECFG_1_2	Mode configuration settings for Mode 1_2	R/W	0100 1111
29	Mode Configuration Mode Setting 1_3, MODECFG_1_3	Mode configuration settings for Mode 1_3	R/W	0000 1100
2A	Mode Configuration Mode Setting 2_0, MODECFG_2_0	Mode configuration settings for Mode 2_0	R/W	0001 1100
2B	Mode Configuration Mode Setting 2_1, MODECFG_2_1	Mode configuration settings for Mode 2_1	R/W	0100 1100
2C	Mode Configuration Mode Setting 2_2, MODECFG_2_2	Mode configuration settings for Mode 2_2	R/W	0100 1111
2D	Mode Configuration Mode Setting 2_3, MODECFG_2_3	Mode configuration settings for Mode 2_3	R/W	0000 1100
2E	Mode Configuration Mode Setting 3_0, MODECFG_3_0	Mode configuration settings for Mode 3_0	R/W	0001 1100
2F	Mode Configuration Mode Setting 3_1, MODECFG_3_1	Mode configuration settings for Mode 3_1	R/W	0100 1100
30	Mode Configuration Mode Setting 3_2, MODECFG_3_2	Mode configuration settings for Mode 3_2	R/W	0100 1111
31	Mode Configuration Mode Setting 3_3, MODECFG_3_3	Mode configuration settings for Mode 3_3	R/W	0000 1100
71	Reset monitor	Reset reason monitor	R RO R/W	1000 0000

9.5 Register description

9.5.1 Device information (DEV_INFO, address 00h)

The device identification code stores a unique identifier for each version and/or revision of device, so that the connected MCU recognizes it automatically.

This is a READ ONLY register.

Table 9. DEV_INFO register bit description

Bit	Symbol	Default value	Type	Function
7	DEV_ID [4]	0	R	Device ID
6	DEV_ID [3]	0	R	
5	DEV_ID [2]	0	R	

Table 9. DEV_INFO register bit description...*continued*

Bit	Symbol	Default value	Type	Function
4	DEV_ID [1]	0	R	
3	DEV_ID [0]	0	R	
2	DEV_REV [2]	0	R	Device revision
1	DEV_REV [1]	0	R	
0	DEV_REV [0]	1	R	

9.5.2 Top level interrupt status (TOP_INT, address 01h)

The top-level interrupt register contains flags indicating various top level interrupt events as indicated below. An event latches and only its first occurrence triggers the interrupt signal INTB (if it is not being masked). Reoccurring events do not change the flag's status or trigger an additional interrupt. If multiple interrupt events happen, its corresponding interrupt bits in the related registers are "triggered", however, the INTB signal is only triggered upon the first interrupt event.

The interrupt event reporting on the device is structured in a two-layer configuration. The interrupt events are grouped as (1) system level; (2) charger block; (3) buck regulator block; (4) LDO block. When any interrupt event is triggered, based on which mode it falls into, the related bit for that mode in TOP_INT flags "1". Any of the related bits in TOP_INT only change back to 0 when all the interrupt events in its affiliated mode have been cleared.

This is READ Only register.

Table 10. TOP_INT register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R	Reserved bit
6	RSVD	0	R	Reserved bit
5	RSVD	0	R	Reserved bit
4	RSVD	0	R	Reserved bit
3	SYS_INT	0	R	System level interrupt event trigger indication from events reflected on Sub level interrupt_0 register. 0: no system level interrupt event triggered 1: system level interrupt event triggered
2	CHG_INT	0	R	Linear battery charger block interrupt event trigger indication 0: no linear battery charger block interrupt event triggered 1: linear battery charger block interrupt event triggered
1	SW_INT	0	R	Buck regulator blocks (SW1, SW2) interrupt event trigger indication 0: no interrupt event on SW1 and/or SW2 blocks triggered 1: interrupt event on SW1 and/or SW2 blocks triggered
0	LDO_INT	0	R	LDO block (LDO1, LDO2) interrupt event trigger indication 0: no interrupt event on LDO1 and/or LDO2 blocks triggered 1: interrupt event on LDO1 and/or LDO2 blocks triggered

9.5.3 Sub level interrupt_0 (SUB_INT0, address 02h)

The sub-level interrupt register contains flags indicating the second-tier interrupt event. For this register, it contains system level related interrupt events. Any of the interrupt sources of this register trigger the SYS_INT bit on the TOP_INT register as long as they are unmasked on the Sub_INT0_Mask register.

This is WRITE AND CLEAR register.

Table 11. Sub_INT0 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	W/C	Reserved bit
6	RSVD	0	W/C	Reserved bit
5	ON_PUSH_INT	0	W/C	ON falling edge longer than 5 ms happened
4	TEMP_ PREWARNING	0	W/C	Die temperature pre-warning interrupt 1: die temp ≥ TWARNING 0: die temp < TWARNING. TWARNING threshold is configured by T_ WARNING [1:0]
3	THEM_SHDN	0	W/C	Thermal shutdown interrupt 0: thermal shutdown is not triggered 1: die temp ≥ TSHDN (set in THEM_SHDN [2:0], thermal shutdown is triggered
2	ASYS_ PREWARNING	0	W/C	ASYS Pre-Warning Voltage Interrupt 0: ASYS voltage does NOT fall below the threshold set in ASYS_ PREWARNING [1:0] 1: ASYS voltage falls below the threshold set in ASYS_PREWARNING [1:0]
1	WD_TIMER	0	W/C	Watchdog Timer Expiration Interrupt 0: The watchdog timer expiration has not happened since the last time this bit was cleared. 1: The watchdog timer expiration has happened since the last time this bit was cleared.
0	IN_PWR	0	W/C	Input Voltage Interrupt 0: The IN_PWR bit has not changed since the last time this bit was cleared. 1: The IN_PWR bit has changed since the last time this bit was cleared.

9.5.4 Sub level interrupt_0 mask (Sub_INT0_Mask, address 03h)

This is a READ AND WRITE register.

Table 12. Sub_INT0_Mask bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5	ON_PUSH_INT_MASK	1	R/W	ON Key falling interrupt mask bit 0: Not Masked 1: Masked

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Table 12. Sub_INT0_Mask bit description*...continued*

Bit	Symbol	Default value	Type	Function
4	TEMP_PREWARNING_MASK	1	R/W	Die temp pre-warning interrupt mask bit 0: Not Masked 1: Masked
3	THEM_SHDN_MASK	1	R/W	Thermal shutdown interrupt mask bit 0: Not Masked 1: Masked
2	ASYS_PREWARNING_MASK	1	R/W	ASYS Pre-Warning Voltage Interrupt Mask bit 0: Not Masked 1: Masked
1	WD_TIMER_MASK	1	R/W	Watchdog Timer Expiration Interrupt Mask bit 0: Not Masked 1: Masked
0	IN_PWR_MASK	1	R/W	Input Voltage Interrupt Mask bit 0: Not Masked 1: Masked

9.5.5 Sub level interrupt_1 (Sub_INT1, address 04h)

The sub-level interrupt register contains flags indicating the second-tier interrupt event. For this register, it contains battery charger related interrupt events. Any of the interrupt sources of this register trigger the CHG_INT bit on the TOP_INT register as long as they are unmasked on the Sub_INT1_Mask register.

This is WRITE AND CLEAR register.

Table 13. Sub_INT1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	W/C	Reserved bit
6	ICHG_DEAD_TIMER_INT	0	W/C	Dead charge timer expiration Interrupt 0: The dead charge timer expiration has not happened since last time this bit was cleared 1: The dead charge timer expiration has happened since last time this bit was cleared For more details, see Figure 10
5	VIN_ILIM	0	W/C	Input Current Limit Interrupt 0: no Input current limit has been triggered since the last time this bit is cleared; 1: input current limit event is triggered since last time this bit is cleared.
4	ICHG_FAST_TIMER	0	W/C	Fast Charging Timer Expiration Interrupt 0: The fast charging timer expiration has not happened since the last time this bit was cleared. 1: The fast charging timer expiration has happened since the last time this bit was cleared.
3	ICHG_PREQ_TIMER	0	W/C	Pre-qualification Charging Timer Expiration Interrupt 0: The pre-qual charging timer expiration has not happened since the last time this bit was cleared.

Table 13. Sub_INT1 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				1: The pre-qual charging timer expiration has happened since the last time this bit was cleared.
2	BATTERY_DETECTION	0	W/C	Battery presence Interrupt 0: The VBAT_DET_OK bit has not changed since the last time this bit was cleared. 1: The VBAT_DET_OK bit has changed since the last time this bit was cleared.
1	VBAT	0	W/C	Battery Interrupt 0: The VBAT_OK bit has not changed since the last time this bit was cleared. 1: The VBAT_OK bit has changed since the last time this bit was cleared.
0	CHG_OK	0	W/C	Charger Status Interrupt 0: The CHG_OK bit has not changed since the last time this bit was cleared. 1: The CHG_OK bit has changed since the last time this bit was cleared

9.5.6 Sub level interrupt_1 mask (Sub_INT1_Mask, address 05h)

This is a READ AND WRITE register.

Table 14. Sub_INT1_Mask register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ICHG_DEAD_TIMER_INT_MASK	1	R/W	Dead charge timer Interrupt Mask bit 0: Not Masked 1: Masked
5	VIN_ILIM_MASK	1	R/W	Input Current Limit Interrupt Mask bit 0: Not Masked 1: Masked
4	ICHG_FAST_TIMER_MASK	1	R/W	Fast Charging Timer Expiration Interrupt Mask bit 0: Not Masked 1: Masked
3	ICHG_PREQ_TIMER_MASK	1	R/W	Pre-qual Charging Timer Expiration Interrupt Mask bit 0: Not Masked 1: Masked
2	BATTERY_DETECTION_MASK	1	R/W	Battery presence Interrupt Mask bit 0: Not Masked 1: Masked
1	VBAT_MASK	1	R/W	Battery Interrupt Mask bit 0: Not Masked 1: Masked
0	CHG_OK_MASK	1	R/W	Charger Interrupt Mask bit 0: Not Masked

Table 14. Sub_INT1_Mask register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				1: Masked

9.5.7 Sub level interrupt_2 (Sub_INT2, address 06h)

The sub-level interrupt register contains flags indicating the second-tier interrupt event. For this register, it contains LDO1/LDO2, SW1/SW2 related interrupt events reflected on the SW_INT and LDO_INT bits on the TOP_INT register as long as they are unmasked on the Sub_INT2_Mask register.

This is WRITE AND CLEAR register.

Table 15. Sub_INT2 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	W/C	Reserved bit
6	RSVD	0	W/C	Reserved bit
5	RSVD	0	W/C	Reserved bit
4	RSVD	0	W/C	Reserved bit
3	VOUTSW1	0	W/C	SW1 Output Voltage Interrupt 0: The VOUTSW1_OK bit has not changed since the last time this bit was cleared. 1: The VOUTSW1_OK bit has changed since the last time this bit was cleared.
2	VOUTSW2	0	W/C	SW2 Output Voltage Interrupt 0: The VOUTSW2_OK bit has not changed since the last time this bit was cleared. 1: The VOUTSW2_OK bit has changed since the last time this bit was cleared.
1	VOUTLDO1	0	W/C	LDO1 Output Voltage Interrupt 0: The VOUTLDO1_OK bit has not changed since the last time this bit was cleared. 1: The VOUTLDO1_OK bit has changed since the last time this bit was cleared.
0	VOUTLDO2	0	W/C	LDO2 Output Voltage Interrupt 0: The VOUTLDO2_OK bit has not changed since the last time this bit was cleared. 1: The VOUTLDO2_OK bit has changed since the last time this bit was cleared.

9.5.8 Sub level interrupt_2 mask (Sub_INT2_Mask, address 07h)

This is a READ AND WRITE register.

Table 16. Sub_INT2_Mask register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	1	R/W	Reserved bit
6	RSVD	1	R/W	Reserved bit
5	RSVD	1	R/W	Reserved bit

Table 16. Sub_INT2_Mask register bit description...*continued*

Bit	Symbol	Default value	Type	Function
4	RSVD	1	R/W	Reserved bit
3	VOUTSW1 _MASK	1	R/W	VOUTSW1 Voltage Interrupt Mask bit 0: Not Masked 1: Masked
2	VOUTSW2 _MASK	1	R/W	VOUTSW2 Voltage Interrupt Mask bit 0: Not Masked 1: Masked
1	VOUTLDO1 _MASK	1	R/W	VOUTLDO1 Voltage Interrupt Mask bit 0: Not Masked 1: Masked
0	VOUTLDO2_MASK	1	R/W	VOUTLDO2 Voltage Interrupt Mask bit 0: Not Masked 1: Masked

08h register: Reserved

9.5.9 Top level control_0 (TOP_CTL0, address 09h)

This register contains various configuration bits for top level related functions, part 0. This is a READ AND WRITE register.

Table 17. TOP_CNTL0 register bit description

Bit	Symbol	Default value	Type	Function
7:5	VIN_ILIM_SEL [2:0]	010	R/W	VIN input current limit selection: (min/typ/max) 000: 74 mA/85 mA/98 mA, (another default setting by MTP) 001: 222 mA/255 mA/293 mA 010: 370 mA/425 mA/489 mA (default setting) 011: 517 mA/595 mA/684 mA 100: 665 mA/765 mA/880 mA 101: 813 mA/935 mA/1075 mA 110: 961 mA/1105 mA/1271 mA 111: Input current limit disabled Note: VIN_ILIM_SEL [1] is the only bit that is MTP configurable
4	OPERATION_SEL_ FROM_SHIPMODE	0	R/W	Ship mode wakeup configuration setting 0: upon VIN plug in, the chip enables the battery charging process, AND starts the power-up sequence for LDO1/LDO2/ SW1/SW2 per the setting 1: upon VIN plug in, the chip enables the charging process, LDO1/LDO2/SW1/SW2 remains in shutdown mode and the chip enables only the power-up sequence upon ON pin falling edge Note: This bit is MTP configurable
3	PWR_DN_EN[1]	0	R/W	Power-down Sequence Enable 0: Do not start power-down sequence 1: Start power-down sequence
2	nEN_CHG_IN_ WATCHDOG	0	R/W	Configure operations in a programmed watchdog timer expired 0: When the programmed watchdog timer expires, the following operations take place.

Table 17. TOP_CNTL0 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				• SYSRSTn signal asserts (high to low) • Charging is continued • LDO1/LDO2/SW1/SW2 enters the mode 0 setting 1: When the programmed watchdog timer expires, the following operations take place. • SYSRSTn signal asserts (high to low) • Charging is disabled • LDO1/LDO2/SW1/SW2 enters the mode 0 setting
1	RSVD	0	R/W	Reserved bit
0	PGood_EN	1	R/W	LDO1, LDO2, SW1, SW2 Output Voltage Status Indication 0: Output voltage power-good comparators are disabled. This also sets "VOUTSW1 _OK", "VOUTSW2 _OK", "VOUTLDO1_OK" and "VOUTLDO2 _OK" bits to 0 1: Output voltage power-good comparators are enabled

[1]   A valid VIN does not generate the initial power-up sequence if all power rails have been turned off by setting PWR_DN_EN to 1. The use of PWR_DN_EN bit is prohibited to be used in any application that requires power-up sequence by both VIN and ON key.

The use of SHIP_EN_x (x can be 0, 1, 2 &3) is recommended for the application.

9.5.10 Top level control_1 (TOP_CTL1, address 0Ah)

This register contains various configuration bits for top level related functions, part 1. This is a READ AND WRITE register.

Table 18. TOP_CNTL1 register bit description

Bit	Symbol	Default value	Type	Function
7 6	ASYS_PREWARNING [1:0]	10	R/W	ASYS Program a pre-warning voltage threshold on ASYS 00: 3.3 V 01: 3.4 V 10: 3.5 V 11: 3.6 V
5 4	ASYS_INPUT_SEL [1:0]	00	R/W	ASYS input source selection 00: ASYS is powered by either VBAT or VIN (VIN has higher priority over VBAT if both are presented but only when VIN>VBAT) 01: ASYS is powered by VBAT only 10: ASYS is powered by VIN only 11: ASYS is disconnected to either VBAT or VIN (for internal testing purpose only)
3	RSVD	1	R/W	Reserved bit
2	VIN_OVP_SEL	0	R/W	VIN over-voltage protection threshold (rising) selection 0: 5.50 V 1: 6.0 V **Note: The current default value for VIN_OVP_SEL is set at 5.5 V, but it should be MTP programmable**
1 0	VIN_UVLO_SEL [1:0]	01	R/W	Program an under-voltage lockout threshold (falling) on VIN 00: 2.9 V 01: 3.1 V

Table 18. TOP_CNTL1 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				10: 3.3 V 11: 3.5 V

9.5.11 Top level control_2 (TOP_CTL2, address 0Bh)

This register contains various configuration bits for top level related functions, part 2. This is a READ AND WRITE register.

Table 19. TOP_CNTL2 register bit description

Bit	Symbol	Default value	Type	Function
7 6	ASYS_UVLO_SEL [1:0]	11	R/W	Program a UVLO threshold on ASYS 00: 2.4 V 01: 2.5 V 10: 2.6 V 11: 2.7 V
5	RSVD	0	R/W	Reserved bit
4 3 2	THEM_SHDN [2:0]	011	R/W	Program a thermal shutdown threshold, TSHDN, in rising(hysteresis with 20°C) 000: 95 °C 001: 100 °C 010: 105 °C 011: 110 °C 100: 115 °C 101: 120 °C 110: 125 °C 111: reserved
1 0	DIE_TEMP_WARNING [1:0]	10	R/W	Program a Die temperature warning threshold 00: 75 °C 01: 80 °C 10: 85 °C 11: 90 °C

9.5.12 Top level control_3 (TOP_CTL3, address 0Ch)

This register contains various configuration bits for top level related functions, part 3. This is a READ AND WRITE register.

Table 20. TOP_CNTL3 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5	RSVD	0	R/W	Reserved bit
4	MODE1_I2C	0	R/W	Depending on EN_MODE_SEL_BY_PIN_x (x="0", or "1", or "2", or "3") bit setting, the chip mode control is set by either the I²C bit MODE1_I2 C/ MODE0_I2C value, or the signal applied on external MODESEL1/
3	MODE0_I2C	0	R/W	

Table 20. TOP_CNTL3 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				MODESEL1 pins. Refer to EN_MODE_SEL_BY_PIN description for more details. With EN_MODE_SEL_BY_PIN=0, the mode selection is determined by the following: [MODE1_I2C: MODE0_I2C] = 00, mode 0 setting [MODE1_I2C: MODE0_I2C] = 01, mode 1 setting [MODE1_I2C: MODE0_I2C] = 10, mode 2 setting [MODE1_I2C: MODE0_I2C] = 11, mode 3 setting
2	SW_RST	0	W/C	Chip software reset bit. If user writes a "1" to this bit, it resets all other I^{2}C register bit to its default setting and cycles the regulator outputs, and meanwhile, this bit clears and resets back to "0" as well.
1 0	ON_GLT_LONG [1:0]	01	R/W	Program a long glitch timer on ON key 00: 4 s 01: 8 s 10: 12 s 11: 16 s Note: 2-bit MTP should be reserved to change the default setting

9.5.13 Top level control_4 (TOP_CTL4, address 0Dh)

This register contains various configuration bits for top level related functions, part 4. This is a WRITE ONLY register.

Table 21. TOP_CNTL4 register bit description

Bit	Symbol	Default value	Type	Function
7 6 5 4 3	RSVD	00000	W	Reserved bit
2 1 0	WD_TIMER_CLR [2:0]	000	W	Watchdog Timer Reset. 001: When written 001 to WD_TIMER_CLR [2:0], the watchdog timer is reset. All other values: when written to WD_TIMER_CLR [2:0], watchdog timer remains unaffected.

9.5.14 Battery charger control_0 (CHG_CTL0, address 10h)

This register stores the linear battery charge related control registers, part 0. This is a READ AND WRITE register.

Table 22. CHG_CNTL0 register bit description

Bit	Symbol	Default value	Type	Function
7 6 5	CHG_LOCK [4:0]	00000	R/W	Critical charger related setting lock. CHG_LOCK [4:0] = 10101, these registers which are labeled as "locked by CHG_LOCK" can be accessed to perform I^{2}C "write" command.

Table 22. CHG_CNTL0 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
4 3				CHGN_LOCK [4:0] ≠ 10101, these registers which are labeled as "locked by CHG_LOCK" can NOT be accessed to perform I^{2}C "write" command. In such case when "write" command is performed on these locked registers, it keeps the present register value.
2	NTC_EN	0	R/W	Enable TS pin external thermistor (NTC) control in charger 0: Disable Thermistor (NTC) control in charger 1: Enable Thermistor (NTC) control in charger
1	CHG_TIMER_EN	1	R/W	Enable the fast charge timer and pre-qual timer 0: Disable both fast charge timer and pre-qual timer 1: Enable both fast charge timer and pre-qual timer
0	CHG_EN	1	R/W	Enable the linear battery charger 0: Disable charger 1: Enable charger **Note: The default value for this bit should be MTP programmable**

9.5.15 Battery charger control_1 (CHG_CTL1, address 11h)

This register stores the linear battery charge related control registers, part 1.

This is a READ AND WRITE register, **and this register is locked by CHG_LOCK**.

Table 23. CHG_CNTL1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5 4 3 2 1 0	ICHG_CC [5:0]	001000	R/W	Program a fast charge current **Note: The current default value for ICHG_CC [5:0] is set at 40 mA, but it should be MTP programmable.**

Table 24. Linear battery charger constant current (CC) setting

00h: 0 mA	10h: 80 mA	20h: 160 mA	30h: 240 mA
01h: 5 mA	11h: 85 mA	21h: 165 mA	31h: 245 mA
02h: 10 mA	12h: 90 mA	22h: 170 mA	32h: 250 mA
03h: 15 mA	13h: 95 mA	23h: 175 mA	33h: 255 mA
04h: 20 mA	14h: 100 mA	24h: 180 mA	34h: 260 mA
05h: 25 mA	15h: 105 mA	25h: 185 mA	35h: 265 mA
06h: 30 mA	16h: 110 mA	26h: 190 mA	36h: 270 mA
07h: 35 mA	17h: 115 mA	27h: 195 mA	37h: 275 mA
08h: 40 mA **(default)**	18h: 120 mA	28h: 200 mA	38h: 280 mA

Table 24. Linear battery charger constant current (CC) setting...*continued*

09h: 45 mA	19h: 125 mA	29h: 205 mA	39h: 285 mA
0Ah: 50 mA	1Ah: 130 mA	2Ah: 210 mA	3Ah: 290 mA
0Bh: 55 mA	1Bh: 135 mA	2Bh: 215 mA	3Bh: 295 mA
0Ch: 60 mA	1Ch: 140 mA	2Ch: 220 mA	3Ch: 300 mA
0Dh: 65 mA	1Dh: 145 mA	2Dh: 225 mA	3Dh: 305 mA
0Eh: 70 mA	1Eh: 150 mA	2Eh: 230 mA	3Eh: 310 mA
0Fh: 75 mA	1Fh: 155 mA	2Fh: 235 mA	3Fh: 315 mA

9.5.16 Battery charger control_2 (CHG_CTL2, address 12h)

This register stores the present status of chip, part 2, linear battery charger related status. This is a READ AND WRITE register, **and this register is locked by CHG_LOCK**.

Table 25. CHG_CNTL2 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5	ICHG_TOPOFF [5:0]	000100b	R/W	Program a top-off current
4				**Note: The current default value for ICHG_TOPOFF [5:0] is set at 4 mA, but it should be MTP programmable.**
3				
2				
1				
0				

Table 26. Linear battery charger top-off charge current setting

00h: 0mA	10h: 16mA	20h: 32mA	30h: 48mA
01h: 1mA	11h: 17mA	21h: 33mA	31h: 49mA
02h: 2mA	12h: 18mA	22h: 34mA	32h: 50mA
03h: 3mA	13h: 19mA	23h: 35mA	33h: 51mA
04h: 4mA **(default)**	14h: 20mA	24h: 36mA	34h: 52mA
05h: 5mA	15h: 21mA	25h: 37mA	35h: 53mA
06h: 6mA	16h: 22mA	26h: 38mA	36h: 54mA
07h: 7mA	17h: 23mA	27h: 39mA	37h: 55mA
08h: 8mA	18h: 24mA	28h: 40mA	38h: 56mA
09h: 9mA	19h: 25mA	29h: 41mA	39h: 57mA
0Ah: 10mA	1Ah: 26mA	2Ah: 42mA	3Ah: 58mA
0Bh: 11mA	1Bh: 27mA	2Bh: 43mA	3Bh: 59mA
0Ch: 12mA	1Ch: 28mA	2Ch: 44mA	3Ch: 60mA
0Dh: 13mA	1Dh: 29mA	2Dh: 45mA	3Dh: 61mA

Table 26. Linear battery charger top-off charge current setting...*continued*

0Eh: 14mA	1Eh: 30mA	2Eh: 46mA	3Eh: 62mA
0Fh: 15mA	1Fh: 31mA	2Fh: 47mA	3Fh: 63mA

9.5.17 Battery charger control_3 (CHG_CTL3, address 13h)

This register stores the present status of chip, part 3, linear battery charger related status. This is a READ AND WRITE register, **and this register is locked by CHG_LOCK**.

Table 27. CHG_CNTL3 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5:0	ICHG_LOW [5:0]	001000	R/W	Program a pre-charge (Low battery charge current) Note: Current value set in ICHG_LOW [5:0] should NOT be higher than the value set in ICHG_CC [5:0]. **Note: The current default value for ICHG_LOW [5:0] is set at 8 mA, ICHG_LOW [4:3] should be MTP programmable. For MTP options, ICHG_LOW can only selected from 0 mA, 8 mA, 16 mA, 24 mA**

Table 28. Low battery charge current setting

00h: 0 mA	10h: 16 mA	20h: 32 mA	30h: 48 mA
01h: 1 mA	11h: 17 mA	21h: 33 mA	31h: 49 mA
02h: 2 mA	12h: 18 mA	22h: 34 mA	32h: 50 mA
03h: 3 mA	13h: 19 mA	23h: 35 mA	33h: 51 mA
04h: 4 mA	14h: 20 mA	24h: 36 mA	34h: 52 mA
05h: 5 mA	15h: 21 mA	25h: 37 mA	35h: 53 mA
06h: 6 mA	16h: 22 mA	26h: 38 mA	36h: 54 mA
07h: 7 mA	17h: 23 mA	27h: 39 mA	37h: 55 mA
08h: 8 mA **(default)**	18h: 24 mA	28h: 40 mA	38h: 56 mA
09h: 9 mA	19h: 25 mA	29h: 41 mA	39h: 57 mA
0Ah: 10 mA	1Ah: 26 mA	2Ah: 42 mA	3Ah: 58 mA
0Bh: 11 mA	1Bh: 27 mA	2Bh: 43 mA	3Bh: 59 mA
0Ch: 12 mA	1Ch: 28 mA	2Ch: 44 mA	3Ch: 60 mA
0Dh: 13 mA	1Dh: 29 mA	2Dh: 45 mA	3Dh: 61 mA
0Eh: 14 mA	1Eh: 30 mA	2Eh: 46 mA	3Eh: 62 mA
0Fh: 15 mA	1Fh: 31 mA	2Fh: 47 mA	3Fh: 63 mA

9.5.18 Battery charger control_4 (CHG_CTL4, address 14h)

This register stores the present status of chip, part 4, linear battery charger related status. This is a READ AND WRITE register, **and this register is locked by CHG_LOCK**.

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Table 29. CHG_CNTL4 register bit description

Bit	Symbol	Default value	Type	Function
7:6	ICHG_DEAD_TIMER [7:6]	0	R/W	Program a Dead charge timer Note: The current default value for ICHG_DEAD_TIMER [7:6] is set at 5 sec. For more details, see Figure 10
5 4 3 2 1 0	ICHG_DEAD [5:0]	000100	R/W	Program a Dead battery charge current Note: Current value set in ICHG_DEAD [5:0] should **NOT** be greater than the value set in ICHG_LOW [5:0]. **Note: The current default value for ICHG_DEAD [5:0] is set at 4 mA, ICHG_DEAD [2] and ICHG_DEAD [4] should be MTP programmable.**

Table 30. Dead charge timer setting

Bit7	Bit6	Timer
0	0	5 sec
0	1	10 sec
1	0	20 sec
1	1	40 sec

Table 31. Dead battery charge current setting

00h: 0 mA	10h: 16 mA	20h: 32 mA	30h: 48 mA
01h: 1 mA	11h: 17 mA	21h: 33 mA	31h: 49 mA
02h: 2 mA	12h: 18 mA	22h: 34 mA	32h: 50 mA
03h: 3 mA	13h: 19 mA	23h: 35 mA	33h: 51 mA
04h: 4 mA **(default)**	14h: 20 mA	24h: 36 mA	34h: 52 mA
05h: 5 mA	15h: 21 mA	25h: 37 mA	35h: 53 mA
06h: 6 mA	16h: 22 mA	26h: 38 mA	36h: 54 mA
07h: 7 mA	17h: 23 mA	27h: 39 mA	37h: 55 mA
08h: 8 mA	18h: 24 mA	28h: 40 mA	38h: 56 mA
09h: 9 mA	19h: 25 mA	29h: 41 mA	39h: 57 mA
0Ah: 10 mA	1Ah: 26 mA	2Ah: 42 mA	3Ah: 58 mA
0Bh: 11 mA	1Bh: 27 mA	2Bh: 43 mA	3Bh: 59 mA
0Ch: 12 mA	1Ch: 28 mA	2Ch: 44 mA	3Ch: 60 mA
0Dh: 13 mA	1Dh: 29 mA	2Dh: 45 mA	3Dh: 61 mA
0Eh: 14 mA	1Eh: 30 mA	2Eh: 46 mA	3Eh: 62 mA
0Fh: 15 mA	1Fh: 31 mA	2Fh: 47 mA	3Fh: 63 mA

9.5.19 Battery charger control_5 (CHG_CTL5, address 15h)

This register stores the present status of chip, part 5, linear battery charger related status. This is a READ AND WRITE register, **and this register is locked by CHG_LOCK**.

Table 32. CHG_CNTL5 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	VBAT_RESTART	0	R/W	Program a threshold for recharge 0: 140 mV below a programmed V_{BAT_REG} 1: 240 mV below a programmed V_{BAT_REG} **Note: The default value should be 1-bit MTP programmable.**
5 4 3 2 1 0	VBAT_REG [5:0]	011110	R/W	Program a battery regulation voltage, V_{BAT_REG} **Note: The current default value for VBAT_REG [5:0] is set at 4.20 V, but it should be MTP programmable.**

Table 33. VBATREG, linear battery charger regulated battery voltage setting

00h: 3.60 V	10h: 3.92 V	20h: 4.24 V	30h: 4.56 V
01h: 3.62 V	11h: 3.94 V	21h: 4.26 V	31h: 4.58 V
02h: 3.64 V	12h: 3.96 V	22h: 4.28 V	32h: 4.60 V
03h: 3.66 V	13h: 3.98 V	23h: 4.30 V	33 to 3Fh: 4.60 V
04h: 3.68 V	14h: 4.00 V	24h: 4.32 V	
05h: 3.70 V	15h: 4.02 V	25h: 4.34 V	
06h: 3.72 V	16h: 4.04 V	26h: 4.36 V	
07h: 3.74 V	17h: 4.06 V	27h: 4.38 V	
08h: 3.76 V	18h: 4.08 V	28h: 4.40 V	
09h: 3.78 V	19h: 4.10 V	29h: 4.42 V	
0Ah: 3.80 V	1Ah: 4.12 V	2Ah: 4.44 V	
0Bh: 3.82 V	1Bh: 4.14 V	2Bh: 4.46 V	
0Ch: 3.84 V	1Ch: 4.16 V	2Ch: 4.48 V	
0Dh: 3.86 V	1Dh: 4.18 V	2Dh: 4.50 V	
0Eh: 3.88 V	1Eh: 4.20 V **(default)**	2Eh: 4.52 V	
0Fh: 3.90 V	1Fh: 4.22 V	2Fh: 4.54 V	

9.5.20 Battery charger control_6 (CHG_CTL6, address 16h)

This register stores the present status of chip, part 7, linear battery charger related status. This is a READ AND WRITE register, and this register is locked by CHG_LOCK.

Table 34. CHG_CNTL6 register bit description

Bit	Symbol	Default value	Type	Function
7	NTC_RES_SEL	1	R/W	External thermistor typical resistance selection (NTC thermistor bias current selection) 0: 100 kΩ (I = 5 µA) 1: 10 kΩ (I = 50 µA)
6	TIMER_2X	0	R/W	Charging Safety Timer Extension 0: Both pre-qual and fast charge timer duration keeps as the values set in ICHG_PREQ_TIMER [1:0] and ICHG_FAST_TIMER [1:0] 1: Both pre-qual and fast charge timer duration is extended to 2x of the values set in ICHG_PREQ_TIMER [1:0] and ICHG_FAST_TIMER [1:0]
5 4	ICHG_FAST_ TIMER [1:0]	01	R/W	Linear battery charger fast charge timer setting 00: 3 hr 01: 5 hr 10: 7 hr 11: 9 hr
3 2	ICHG_PREQ_ TIMER [1:0]	01	R/W	Linear battery charger pre-qualification charge timer setting 00: 15 min 01: 30 min 10: 45 min 11: 60 min
1 0	T_TOPOFF [1:0]	01	R/W	TOPOFF Timer setting 00: 0 min 01: 6.4 min 10: 12.8 min 11: 19.2 min

9.5.21 Battery charger control_7 (CHG_CTL7, address 17h)

This register stores the present status of chip, part 7, linear battery charger related status. This is a READ AND WRITE register.

Table 35. CHG_CNTL7 register bit description

Bit	Symbol	Default value	Type	Function
7:5	NTC_BETA_SEL [2:0]	001	R/W	Set the thermistor beta value selection (see below)
4	RSVD	0	R/W	Reserved bit
3	RSVD	0	R/W	Reserved bit
2 1 0	THM_REG [2:0]	100	R/W	Thermal regulation threshold setting (see below)

Table 36. Set the thermistor beta value selection (Thermistor beta values below are defined for (25/85°C) range)

000: 3434k	010: 3934k	100: 4100k	110: 4543k
001: 3610k	011: 3950k	101: 4311k	111: 4750k

Table 37. Thermal regulation threshold setting

000: 80 °C	010: 90 °C	100: 100 °C	110: 110 °C
001: 85 °C	011: 95 °C	101: 105 °C	111: 115 °C

9.5.22 Battery charger status_0 (CHG_STATUS_0, address 18h)

This register stores the present status of the linear battery charger, part 0. This is a READ ONLY register. The status of this register is only valid when VIN_ILIM condition is not reached.

Table 38. CHG_STATUS_0 register bit description

Bit	Symbol	Default value	Type	Function
7	VBAT_DET_OK	0	R	VBAT Detection Status 0: No valid battery attachment detected 1: Battery attachment detected
6	VBAT_OK	0	R	(Only valid with VBAT_DET_OK = 1) VBAT status, refer to BAT_DETAIL_STATUS [2:0] for more details 0: the battery is invalid/missing, or charger reset is active, i.e. BAT_DETAIL_STATUS [2:0] = 0b000, 0b111 1: the battery is OK. i.e. BAT_DETAIL_STATUS [2:0] = 0b001, 0b010, 0b011, 0b100, 0b101
5	IN_PWR_OK	0	R	IN_PWR (input power) status, refer to IN_PWR_STATUS [1:0] for more details 0: Input power voltages are invalid. i.e. IN_PWR_STATUS [1:0] ≠ 0b11 1: Input power voltages are valid. i.e. IN_PWR_STATUS [1:0] = 0b11
4	CHG_OK	1	R	Charger status 0: The charger has suspended due to the following conditions: TS_DETAIL_STATUS [2:0] = 001'b or 100'b; or SFTY_TIMER_STATUS [1:0] ≠ 00'b 1: The charger is OK
3	RSVD	0	R	Reserved bit
2	RSVD	0	R	Reserved bit
1	RSVD	0	R	Reserved bit
0	RSVD	0	R	Reserved bit

9.5.23 Battery charger status_1 (CHG_STATUS_1, address 19h)

This register stores the present status of the linear battery charger, part 1. This is a READ ONLY register. The status of this register is only valid when VIN_ILIM condition is not reached.

Table 39. CHG_STATUS_1 register bit description

Bit	Symbol	Default value	Type	Function
7 6	IN_PWR_STATUS	00	R	VIN and ASYS charger input power Status 00: Input power is invalid. VIN<VIN_UVLO 01: Input power is invalid. ASYS< VBAT+VINBAT_HEADROOM and VIN>VIN_UVLO 10: Input power is invalid. VIN>VIN_OVP 11: Input power is valid. VIN>VIN_UVLO, ASYS>VBAT+VINBAT_HEADROOM, VIN<VIN_OVP

Table 39. CHG_STATUS_1 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
5	RSVD	0	R	Reserved bit
4	TREG_STATUS	0	R	Temperature Regulation Loop Status 0: Die junction temperature is less than the threshold set by THM_REG and the full charge current limit is available. 1: Die junction temperature is greater than the threshold set by THM_REG, and the charge current limit may be folding back to reduce power dissipation.
3	RSVD	0	R	Reserved bit
2	RSVD	0	R	Reserved bit
1	RSVD	0	R	Reserved bit
0	RSVD	0	R	Reserved bit

9.5.24 Battery charger status_2 (CHG_STATUS_2, address 1Ah)

This register stores the present status of the linear battery charger, part 2.

This is a READ ONLY register. The status of this register is only valid when IN_PWR_OK = 1. The status of this register is only valid when VIN_ILIM condition is not reached.

Table 40. CHG_STATUS_2 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R	Reserved bit
6 5 4	BAT_DETAIL_STATUS [2:0]	111	R	Battery conditions in details 000: Battery missing, not attached 001: Battery detection in-progress 010: $VBAT < V_{BAT\_DEAD}$ 011: $V_{BAT\_DEAD} < VBAT < V_{BAT\_LOW}$ 100: $V_{BAT\_LOW} < VBAT < (V_{BAT\_REG} - V_{BAT\_RESTART})$ 101: $VBAT > (V_{BAT\_REG} - V_{BAT\_RESTART})$ 110: reserved 111: battery charger is in reset
3	RSVD	0	R	Reserved bit
2 1 0	BAT_CHG_STATUS [2:0]	000	R	Charge conditions in details: 000: Charger in Idle State 001: Charger in Dead-Battery State 010: Charger in Low-Battery State 011-100: Charger in Fast Charging state in either CC or CV 101: Charger in Top-off State 110: Charger in Done State 111: Reserved

9.5.25 Battery charger status_3 (CHG_STATUS_3, address 1Bh)

This register stores the present status of the linear battery charger, part 3. This is a READ ONLY register. The status of this register is only valid when VIN_ILIM condition is not reached.

Table 41. CHG_STATUS_3 register bit description

Bit	Symbol	Default value	Type	Function
7	TS_STATUS	0	R	0: TS_DETAIL_STATUS [2:0] = 000. Battery temp is normal, no impact on normal charging. 1: TS_DETAIL_STATUS [2:0] ≠ 000.
6 5 4	TS_DETAIL_STATUS [2:0]	000	R	000: Battery Temperature Nominal, T2 ≤ T ≤ T3 001: Battery Temperature is Cold, T < T1 010: Battery Temperature is Cool, T1 ≤ T < T2 011: Battery Temperature is Warm, T3 < T ≤ T4 100: Battery Temperature is Hot, T > T4
3	RSVD	0	R	Reserved bit
2	CHIP_TEMP_STATUS	0	R	Chip Temp Status: 0: Thermal regulation not activated 1: Thermal regulation activated
1 0	SFTY_TIMER_STATUS [1:0]	00	R	00: Safety Timers having No Effect on Battery Charging 01: Pre-qual Timer expires, battery charging suspended 10: Fast Timer expires, battery Charging suspended 11: Battery short test fails, battery charging suspended

1Ch to 1Fh registers: Reserved

9.5.26 Regulator status (REG_STATUS, address 20h)

This register stores the present status of the SW1, SW2, LDO1, LDO2. This is a READ ONLY register.

Table 42. REG_STATUS register bit description

Bit	Symbol	Default value	Type	Function
7	VOUTSW1 _OK	0	R	SW1 VOUT "Power-good" Status 0: VOUT_SW1 is not OK, i.e., VOUTSW1 / VOUTSW1(nominal) ≤ 90 % or VOUTSW1 / VOUTSW1(nominal) ≥ 110 % 1: VOUT_SW1 is OK, i.e., 110 % > VOUTSW1 / VOUTSW1(nominal) > 90 %
6	VOUTSW2 _OK	0	R	SW2 VOUT "Power-good" Status 0: VOUT_SW2 is not OK, i.e., VOUTSW2 / VOUTSW2(nominal) ≤ 90 % or VOUTSW2 / VOUTSW2(nominal) ≥ 110 % 1: VOUT_SW2 is OK, i.e., 110 % > VOUTSW2 / VOUTSW2(nominal) > 90 %
5	VOUTLDO1 _OK	0	R	LDO1VOUT "Power-good" Status 0: VOUTLDO1 is not OK, i.e., VOUTLDO1 / VOUTLDO1 (nominal) ≤ 90 % or VOUT LDO1 / VOUT LDO1 (nominal) ≥ 110 % 1: VOUTLDO1 is OK, i.e., 110 % > VOUTLDO1 / VOUTLDO1 (nominal) > 90 %
4	VOUTLDO2_OK	0	R	LDO2VOUT "Power-good" Status 0: VOUTLDO2 is not OK, i.e., VOUTLDO2 / VOUTLDO2 (nominal) ≤ 90 % or VOUTLDO2 / VOUTLDO2 (nominal) ≥ 110 % 1: VOUTLDO2 is OK, i.e., 110 % > VOUTLDO2 / VOUTLDO2 (nominal) > 90 %
3	RSVD	0	R	Reserved bit

Table 42. REG_STATUS register bit description...*continued*

Bit	Symbol	Default value	Type	Function
2	RSVD	0	R	Reserved bit
1	RSVD	0	R	Reserved bit
0	RSVD	0	R	Reserved bit

9.5.27 Active Discharge Regulator control (ACT_DISCHARGE_CNTL, address 21h)

This register stores the control functions of the SW1, SW2, LDO1, LDO2. This is a READ AND WRITE register.

Table 43. ACT_DISCHARGE_CNTL register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	RSVD	0	R/W	Reserved bit
5	RSVD	0	R/W	Reserved bit
4	RSVD	0	R/W	Reserved bit
3	nEN_SW1_BLEED	0	R/W	SW1 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor
2	nEN_SW2_BLEED	0	R/W	SW2 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor
1	nEN_LDO1_BLEED	0	R/W	LDO1 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor
0	nEN_LDO2_BLEED	0	R/W	LDO2 Output Active Discharge Turn-on Control in the regulator disabled 0: Enable output discharge bleeding resistor 1: Disable Output discharge bleeding resistor

9.5.28 Mode configuration mode setting 0_0 (MODECFG_0_0, address 22h)

This register contains mode setting 0, part 0 configuration register. This is a READ AND WRITE register.

Table 44. MODECFG_0_0 register bit description

Bit	Symbol	Default value	Type	Function
7	SHIP_EN_0	0	R/W	Ship mode enable/disable in mode setting 0 0: Device is NOT set in ship mode 1: Device is set in ship mode
6	EN_MODE_SEL_BY_PIN_0	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 0: 0: mode control by internal I^{2}C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored. 1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^{2}C register bits, MODE0_I2C and MODE1_I2C

Table 44. MODECFG_0_0 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				[1-bit MTP to set default value]
5 4 3 2 1 0	SW1_OUT_0 [5:0]	010100	R/W	SW1 output voltage for mode setting 0 (see below). **[Note: The default value for SW1 _OUT_0[5:0] is set at 1.00 V, but it should be MTP programmable.]**

Table 45. SW1 output voltage for Mode Setting 0

000000=0.500 V	001110=0.850 V	011100=1.200 V
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V
000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V **(default)**	100010=1.350 V
000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V
001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V
001100=0.800 V	011010=1.150 V	101000=1.500 V
001101=0.825 V	011011=1.175 V	101001 to 111110=1.5 V
		111111 = 1.8 V

9.5.29 Mode configuration mode setting 0_1 (MODECFG_0_1, address 23h)

This register contains mode setting A, part 1 configuration register. This is a READ AND WRITE register.

Table 46. MODECFG _0_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_0	0	R/W	Mode configuration upon falling edge applied on "ON" pin in Mode Setting 0: 0: upon valid falling edge applied on "ON" pin, the device switches back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch) 1: upon valid falling edge applied on "ON" pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_0_OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 0

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Table 46. MODECFG_0_1 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				0: SW2 Output Voltage = SW2_OUT_0_LSB [4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_0_LSB [4:0] + 1.2 V
4 3 2 1 0	SW2_OUT_0_LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 0 (see below). **Note: The default value for SW2_OUT_A_LSB [4:0] is set at 1.8 V, but it should be MTP programmable.**

Table 47. SW2 default output voltage for mode setting 0

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.30 Mode configuration mode setting 0_2 (MODECFG_0_2, address 24h)

This register contains mode setting 0, part 2 configuration register. This is a READ AND WRITE register.

Table 48. MODECFG_0_2 register bit description

Bit	Symbol	Default value	Type	Function
7 6 5 4	LDO1_OUT_0 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 0 (see below). **Note: The default value for LDO1_OUT_0 [3:0] is set at 1.8V, but it should be MTP programmable.**
3	SW1_EN_0	1	R/W	SW1 Enable Control in mode setting 0: 0: SW1 disabled 1: SW1 enabled **Note: reserve 1-bit MTP to set its default value**
2	SW2_EN_0	1	R/W	SW2 Enable Control in mode setting 0: 0: SW2 disabled 1: SW2 enabled **Note: reserve 1-bit MTP to set its default value**
1	LDO1_EN_0	1	R/W	LDO1 Enable Control in mode setting 0: 0: LDO1 disabled 1: LDO1 enabled

Table 48. MODECFG_0_2 register bit description...*continued*

Bit	Symbol	Default value	Type	Function
				Note: reserve 1-bit MTP to set its default value
0	LDO2_EN_0	1	R/W	LDO2 Enable Control in mode setting 0: 0: LDO2 disabled 1: LDO2 enabled **Note: reserve 1-bit MTP to set its default value**

Table 49. LDO1 default output voltage for mode setting 0

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.31 Mode configuration mode setting 0_3 (MODECFG_0_3, address 25h)

This register contains mode setting 0, part 3 configuration register. This is a READ AND WRITE register.

Table 50. MODECFG_0_3 register bit description

Bit	Symbol	Default value	Type	Function
7 6	WD_TIMER_0 [1:0]	00	R/W	Watchdog timer setting in mode setting 0: 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s 10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s **[2-bit MTP to set default value]**
5	LDO2_OUT_0_OFFSET	1	R/W	LDO2 output voltage offset selection in mode setting 0: 0: LDO2 Output Voltage = LDO2_OUT_0_LSB[4:0] + 0 V 1: LDO2 Output Voltage = LDO2_OUT_0_LSB[4:0] + 1.2 V **[1-bit MTP to set default value]**
4 3 2 1 0	LDO2_OUT_0_LSB [4:0]	11001	R/W	LDO2 default output voltage for mode setting 0 (see below). **Note: The default value for LDO2_OUT_0_LSB [4:0] is set at 3.3 V, but it should be MTP programmable.**

Table 51. LDO2 default output voltage for mode setting 0

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V

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Table 51. LDO2 default output voltage for mode setting 0...*continued*

00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V **(default)**
01000=1.700 V	10001=1.925 V	

9.5.32 Mode configuration mode setting 1_0 (MODECFG_1_0, address 26h)

This register contains mode setting 1, part 0 configuration register. This is a READ AND WRITE register.

Table 52. MODECFG_1_0 register bit description

Bit	Symbol	Default value	Type	Function
7	SHIP_EN_1	0	R/W	Ship mode enable/disable in mode setting 1 0: Device is NOT set in ship mode 1: Device is set in ship mode
6	EN_MODE_SEL_BY_PIN_1	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 1: 0: mode control by internal I^{2}C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored. 1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^{2}C register bits, MODE0_I2C and MODE1_I2C
5 4 3 2 1 0	SW1_OUT_1 [5:0]	011100	R/W	SW1 output voltage for mode setting 1 (see below).

Table 53. SW1 output voltage for Mode Setting 1

000000=0.500 V	001110=0.850 V	011100=1.200 V **(default)**
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V
000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V	100010=1.350 V
000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V
001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V
001100=0.800 V	011010=1.150 V	101000=1.500 V

Table 53. SW1 output voltage for Mode Setting 1...*continued*

001101=0.825 V	011011=1.175 V	101001 to 111110 = 1.5 V
		111111 = 1.8 V

9.5.33 Mode configuration mode setting 1_1 (MODECFG_1_1, address 27h)

This register contains mode setting 1, part 1 configuration register. This is a READ AND WRITE register.

Table 54. MODECFG_1_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_1	1	R/W	Mode configuration upon falling edge applied on "ON" pin in Mode Setting B: 0: upon valid falling edge applied on "ON" pin, the device switches back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch) 1: upon valid falling edge applied on "ON" pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_1_OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 1 0: SW2 Output Voltage = SW2_OUT_1_LSB[4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_1_LSB[4:0] + 1.2 V
4 3 2 1 0	SW2_OUT_1_LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 1 (see below).

Table 55. SW2 default output voltage for mode setting 1

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.34 Mode configuration mode setting 1_2 (MODECFG_1_2, address 28h)

This register contains mode setting 1, part 2 configuration register. This is a READ AND WRITE register.

Table 56. MODECFG_1_2 register bit description

Bit	Symbol	Default value	Type	Function
7 6 5 4	LDO1_ OUT_1 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 1 (see below).
3	SW1_EN_1	1	R/W	SW1 Enable Control in mode setting 1: 0: SW1 disabled 1: SW1 enabled
2	SW2_EN_1	1	R/W	SW2 Enable Control in mode setting 1: 0: SW2 disabled 1: SW2 enabled
1	LDO1_EN_1	1	R/W	LDO1 Enable Control in mode setting 1: 0: LDO1 disabled 1: LDO1 enabled
0	LDO2_EN_1	1	R/W	LDO2 Enable Control in mode setting 1: 0: LDO2 disabled 1: LDO2 enabled

Table 57. LDO1 default output voltage for mode setting 1

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9 V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.35 Mode configuration mode setting 1_3 (MODECFG_1_3, address 29h)

This register contains mode setting 1, part 3 configuration register. This is a READ AND WRITE register.

Table 58. MODECFG_1_3 register bit description

Bit	Symbol	Default value	Type	Function
7 6	WD_TIMER_1 [1:0]	00	R/W	Watchdog timer setting in mode setting 1: 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s 10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s
5	LDO2_OUT_1_OFFSET	0	R/W	LDO2 output voltage offset selection in mode setting 1: 0: LDO2 Output Voltage = LDO2_OUT_1_LSB[4:0] + 0 V 1: LDO2 Output Voltage = LDO2_OUT_1_LSB[4:0] + 1.2 V
4 3 2 1 0	LDO2_OUT_1_LSB [4:0]	01100	R/W	LDO2 default output voltage for mode setting 1 (see below)

Table 59. LDO2 default output voltage for mode setting 1

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.36 Mode configuration mode setting 2_0 (MODECFG_2_0, address 2Ah)

This register contains mode setting 2, part 0 configuration register. This is a READ AND WRITE register.

Table 60. MODECFG_2_0 register bit description

Bit	Symbol	Default value	Type	Function
7	SHIP_EN_2	0	R/W	Ship mode enable/disable in mode setting 2 0: Device is NOT set in ship mode 1: Device is set in ship mode
6	EN_MODE_SEL_BY_PIN_2	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 2 0: mode control by internal I^{2}C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored. 1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^{2}C register bits, MODE0_I2C and MODE1_I2C
5 4 3 2 1 0	SW1_OUT_2 [5:0]	011100	R/W	SW1 output voltage for mode setting 2 (see below).

Table 61. SW1 output voltage for Mode Setting 2

000000=0.500 V	001110=0.850 V	011100=1.200 V **(default)**
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V
000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V	100010=1.350 V

Table 61. SW1 output voltage for Mode Setting 2...*continued*

000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V
001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V
001100=0.800 V	011010=1.150 V	101000=1.500 V
001101=0.825 V	011011=1.175 V	101001 to 111110 = 1.5 V
		111111 = 1.8 V

9.5.37 Mode configuration mode setting 2_1 (MODECFG_2_1, address 2Bh)

This register contains mode setting 2, part 1 configuration register. This is a READ AND WRITE register.

Table 62. MODECFG_2_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_2	1	R/W	Mode configuration upon falling edge applied on "ON" pin in Mode setting 2 0: upon valid falling edge applied on "ON" pin, the device switches back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch) 1: upon valid falling edge applied on "ON" pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_2_OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 2 0: SW2 Output Voltage = SW2_OUT_2_LSB[4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_2_LSB[4:0] + 1.2V
4 3 2 1 0	SW2_OUT_2_LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 2 (see below)

Table 63. SW2 default output voltage for mode setting 2

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V

Table 63. SW2 default output voltage for mode setting 2...*continued*

00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.38 Mode configuration mode setting 2_2 (MODECFG_2_2, address 2Ch)

This register contains mode setting 2, part 2 configuration register. This is a READ AND WRITE register.

Table 64. MODECFG_2_2 register bit description

Bit	Symbol	Default value	Type	Function
7	LDO1_ OUT_2 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 2 (see below).
6				
5				
4				
3	SW1_EN_2	1	R/W	SW1 Enable Control in mode setting 2 0: SW1 disabled 1: SW1 enabled
2	SW2_EN_2	1	R/W	SW2 Enable Control in mode setting 2 0: SW2 disabled 1: SW2 enabled
1	LDO1_EN_2	1	R/W	LDO1 Enable Control in mode setting 2 0: LDO1 disabled 1: LDO1 enabled
0	LDO2_EN_2	1	R/W	LDO2 Enable Control in mode setting 2 0: LDO2 disabled 1: LDO2 enabled

Table 65. LDO1 default output voltage for mode setting 2

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9 V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.39 Mode configuration mode setting 2_3 (MODECFG_2_3, address 2Dh)

This register contains mode setting 2, part 3 configuration register. This is a READ AND WRITE register.

Table 66. MODECFG_2_3 register bit description

Bit	Symbol	Default value	Type	Function
7	WD_TIMER_2 [1:0]	00	R/W	Watchdog timer setting in mode setting 2 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s 10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s
6				
5	LDO2_OUT_2_ OFFSET	0	R/W	LDO2 output voltage offset selection in mode setting 2 0: LDO2 Output Voltage = LDO2_OUT_2_LSB[4:0] + 0 V

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Table 66. MODECFG_2_3 register bit description*...continued*

Bit	Symbol	Default value	Type	Function
				1: LDO2 Output Voltage = LDO2_OUT_2_LSB[4:0] + 1.2 V
4 3 2 1 0	LDO2_OUT_2_ LSB [4:0]	01100	R/W	LDO2 default output voltage for mode setting 2 (see below).

Table 67. LDO2 default output voltage for mode setting 2

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.40 Mode configuration mode setting 3_0 (MODECFG_3_0, address 2Eh)

This register contains mode setting 3, part 0 configuration register. This is a READ AND WRITE register.

Table 68. MODECFG_3_0 register bit description

Bit	Symbol	Default value	Type	Function
7	SHIP_EN_3	0	R/W	Ship mode enable/disable in mode setting 3 0: Device is NOT set in ship mode 1: Device is set in ship mode
6	EN_MODE_ SEL_BY_PIN_3	0	R/W	MODESEL0/MODESEL1 Control Selection in mode setting 3 0: mode control by internal I^{2}C register bits, MODE0_I2C and/or MODE1_I2C only; signal applied on external MODESEL0/MODESEL1 pins is ignored. 1: mode control by signal applied on external MODESEL0 and/or MODESEL1 pins only, not by internal I^{2}C register bits, MODE0_I2C and MODE1_I2C
5 4 3 2 1 0	SW1_OUT_3 [5:0]	011100	R/W	SW1 output voltage for mode setting 3 (see below).

Table 69. SW1 output voltage for mode setting 3

000000=0.500 V	001110=0.850 V	011100=1.200 V **(default)**
000001=0.525 V	001111=0.875 V	011101=1.225 V
000010=0.550 V	010000=0.900 V	011110=1.250 V
000011=0.575 V	010001=0.925 V	011111=1.275 V
000100=0.600 V	010010=0.950 V	100000=1.300 V
000101=0.625 V	010011=0.975 V	100001=1.325 V
000110=0.650 V	010100=1.000 V	100010=1.350 V
000111=0.675 V	010101=1.025 V	100011=1.375 V
001000=0.700 V	010110=1.050 V	100100=1.400 V
001001=0.725 V	010111=1.075 V	100101=1.425 V
001010=0.750 V	011000=1.100 V	100110=1.450 V
001011=0.775 V	011001=1.125 V	100111=1.475 V
001100=0.800 V	011010=1.150 V	101000=1.500 V
001101=0.825 V	011011=1.175 V	101001 to 111110 = 1.5 V
		111111 = 1.8 V

9.5.41 Mode configuration mode setting 3_1 (MODECFG_3_1, address 2Fh)

This register contains mode setting 3, part 1 configuration register. This is a READ AND WRITE register.

Table 70. MODECFG_3_1 register bit description

Bit	Symbol	Default value	Type	Function
7	RSVD	0	R/W	Reserved bit
6	ON_CFG_3	1	R/W	Mode configuration upon falling edge applied on "ON" pin in mode setting 3 0: upon valid falling edge applied on "ON" pin, the device switches back to mode 0 setting (if the device is currently operating in mode 0 setting, then no mode switch) 1: upon valid falling edge applied on "ON" pin, no mode switch, the device stays in its current mode setting operation
5	SW2_OUT_3_OFFSET	0	R/W	SW2 output voltage offset selection in mode setting 3 0: SW2 Output Voltage = SW2_OUT_3_LSB[4:0] + 0 V 1: SW2 Output Voltage = SW2_OUT_3_LSB[4:0] + 1.2 V
4 3 2 1 0	SW2_OUT_3_LSB [4:0]	01100	R/W	SW2 default output voltage for mode setting 3 (see below).

Table 71. SW2 default output voltage for mode setting 3

00000=1.500 V	01001=1.725 V	10010=1.950 V

Table 71. SW2 default output voltage for mode setting 3...*continued*

00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.42 Mode configuration mode setting 3_2 (MODECFG_3_2, address 30h)

This register contains mode setting 3, part 2 configuration register. This is a READ AND WRITE register.

Table 72. MODECFG_3_2 register bit description

Bit	Symbol	Default value	Type	Function
7 6 5 4	LDO1_ OUT_3 [3:0]	0100	R/W	LDO1 default output voltage for mode setting 3 (see below).
3	SW1_EN_3	1	R/W	SW1 Enable Control in mode setting 3 0: SW1 disabled 1: SW1 enabled
2	SW2_EN_3	1	R/W	SW2 Enable Control in mode setting 3 0: SW2 disabled 1: SW2 enabled
1	LDO1_EN_3	1	R/W	LDO1 Enable Control in mode setting 3 0: LDO1 disabled 1: LDO1 enabled
0	LDO2_EN_3	1	R/W	LDO2 Enable Control in mode setting 3 0: LDO2 disabled 1: LDO2 enabled

Table 73. LDO1 default output voltage for mode setting 3

0000: 1.700 V	0011: 1.775 V	0110: 1.850 V	1001 to 1111:1.9 V
0001: 1.725 V	0100: 1.800 V **(default)**	0111: 1.875 V	
0010: 1.750 V	0101: 1.825 V	1000: 1.900 V	

9.5.43 Mode configuration mode setting 3_3 (MODECFG_3_3, address 31h)

This register contains mode setting 3, part 3 configuration register. This is a READ AND WRITE register.

Table 74. MODECFG_3_3 register bit description

Bit	Symbol	Default value	Type	Function
7 6	WD_TIMER_3 [1:0]	00	R/W	Watchdog timer setting in mode setting 3 00: Watchdog Timer Disabled 01: Watchdog Timer = 16 s 10: Watchdog Timer = 32 s 11: Watchdog Timer = 64 s
5	LDO2_OUT_3_OFFSET	0	R/W	LDO2 output voltage offset selection in mode setting D 0: LDO2 Output Voltage = LDO2_OUT_3_LSB[4:0] + 0 V 1: LDO2 Output Voltage = LDO2_OUT_3_LSB[4:0] + 1.2 V
4 3 2 1 0	LDO2_OUT_3_LSB [4:0]	01100	R/W	LDO2 default output voltage for mode setting 3 (see below)

Table 75. LDO2 default output voltage for mode setting 3

00000=1.500 V	01001=1.725 V	10010=1.950 V
00001=1.525 V	01010=1.750 V	10011=1.975 V
00010=1.550 V	01011=1.775 V	10100=2.000 V
00011=1.575 V	01100=1.800 V **(default)**	10101=2.025 V
00100=1.600 V	01101=1.825 V	10110=2.050 V
00101=1.625 V	01110=1.850 V	10111=2.075 V
00110=1.650 V	01111=1.875 V	11000=2.100 V
00111=1.675 V	10000=1.900 V	11001-11111=2.1 V
01000=1.700 V	10001=1.925 V	

9.5.44 RESET reason monitoring (RESET_MONITOR, address 71h)

Register 0x71 is accessible by I^2C. It can be read to see what event caused the CPU power cycling by PMIC.

Note that SHIP_EXIT_DONE status is stored outside of the ASYS domain, so that it survives the ship mode entry/exit. All other bits are cleared by the ship mode entry/exit, because it cycles the power to the digital core.

Table 76. RESET monitor register bit description

Bit	Symbol	Default value	Type	Function
7	ON_FILTERED	1	R	ON pin status; low level debounced for 5 ms (high level propagates instantly). Write to this bit has no effect.
6:5	RSVD	0	RO	Reserved bits
4	THM_STDN_DONE	0	RW	PMIC exited thermal shutdown. All registers reset to defaults. Write 1 to clear.

Table 76. RESET monitor register bit description...*continued*

Bit	Symbol	Default value	Type	Function
3	SHIP_EXIT_DONE	0	RW	PMIC exited Ship mode. All registers reset to defaults. Write 1 to clear.
2	SW_RST_DONE	0	RW	A system reset caused by Software Reset command has occurred. All registers were reset to their defaults. Write 1 to clear.
1	WD_RST_DONE	0	RW	A system reset caused by Watchdog Timer has occurred. Registers were NOT reset to their defaults. Write 1 to clear.
0	LONG ON_DONE	0	RW	A system reset caused by long ON press has occurred. All registers were reset to their defaults. Write 1 to clear.

10 Limiting values

Table 77. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
Voltage range (with respect to AGND)	VIN		-0.3	20	V
	ASYS, VBAT, VBAT_BKUP		-0.3	6	V
	LX1, LX2		-2	6	V
	SW1_OUT, SW2_OUT		-0.3	6	V
	LDO1, LDO2		-0.3	6	V
	SDA, SCL, MODESEL0, MODESEL1, ON, TS, SYSRSTn, INTB		-0.3	6	V
	PGND to AGND		-0.3	0.3	V
$I_{O(sink)}$	Output sink current	on pins SYSRSTn, INTB, SDA, SCL		5	mA
T_j	Junction temperature		–40	125	°C

11 ESD ratings

Table 78. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	-	2000	V
		Charged device model (CDM)	-	500	V

12 Recommended operating conditions

Table 79. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	Supply Voltage	VIN	3.3	5.5	V
V_{IO}	Input/output voltage	SDA, SCL, MODESEL0, MODESEL1, SYSRSTn	0	3.6	V
T_{amb}	Ambient Temperature		-40	85	°C
T_j	Junction Temperature		-40	125	°C
T_{stg}	Storage Temperature		-55	150	°C
V_{TS}	voltage at TS pin	TS	0	5.0	V

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13 Electrical characteristics

Unless otherwise specified, V_{VIN}=5 V, V_{VBAT}=3.8 V, LDO1_OUT=1.8 V, LDO2_OUT=1.8 V. C_{VIN}=2.2 µF/10 V, C_{ASYS}=4.7 µF/10 V, C_{VBAT}=1 µF/10 V, C_{LDO1_OUT}=1 µF/6.3 V, C_{LDO2_OUT}=2.2 µF/6.3 V, C_{SW1_OUT}=10 µF/6.3 V, C_{SW2_OUT}=10 µF/6.3 V, L_{SW1} =2.2 µH, L_{SW2} =2.2 µH, T_{amb}= -40 °C to +85 °C, Typical value at T_{amb}=25 °C

13.1 Top level parameter

Table 80. EC table for Top level

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT QUIESCENT CURRENT						
$I_{BAT\_NOLOAD1}$	VBAT quiescent Current VBAT=4.5 V SW1, SW2, LDO1, LDO2 enabled, no load. No switching on SW1, SW2. VIN = open, charger disabled	T_J = 25 °C		2.9	4.5	µA
		T_J = 85 °C [1]		4.5	8	
$I_{BAT\_NOLOAD2}$[1]	VBAT quiescent Current VBAT = 4.5 V SW1, SW2, LDO1, LDO2 enabled, no load. Switching on SW1, SW2. VIN = open, charger disabled	T_J = 25 °C		3.5	5	µA
		T_J = 85 °C		5.5	11	
$I_{BAT\_DISABLE}$[1]	VBAT quiescent Current VBAT = 4.5 V SW1, SW2, LDO1, LDO2 Disabled VIN = open, charger disabled	T_J = 25 °C		750	1200	nA
		T_J = 85 °C		1500	3000	
I_{BAT_SHIP}	VBAT quiescent current	VBAT=4.5 V VIN =open, Ship Mode activated at T_J = 25 °C		100	150	nA
VIN						
VIN_{UVLO}	VIN Under voltage lock-out	I²C programmable in 200 mV steps, VIN Falling	2.9		3.5	V
$VIN_{UVLO\ Accuracy}$			-5		+5	%
VIN_{UVLO_HYS}	Hysteresis on VINUVLO			200		mV
VIN_{OVP}		I²C programmable at 5.5 V or 6 V, VIN Rising	5.5		6.0	V
$VIN_{OVP\ Accuracy}$	Input over- voltage protection threshold		-3.5		+3.5	%
$VIN_{OVP\ Hysteresis}$		VIN Falling		100		mV
$t_{DGL(VINOVP)}$[1]	Input over-voltage reaction time	VIN: 5 V → 7 V, 1 V/ µs		1.5	3	µs
VIN Current Limit	Input current limit	VIN_ILIM [2:0] = 000	74	85	98	mA

Table 80. EC table for Top level...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		VIN_ILIM [2:0] = 010	370	425	489	
ASYS						
$V_{ASYS\_UVLO\_RISING}$		ASYS in rising		2.8		V
$V_{ASYS\_UVLO\_FALLING}$		ASYS in falling		2.7		V
		By MTP		2.4		
%$V_{ASYS\_UVLO\_FALLING}$	ASYS UVLO Accuracy		-3.5		+3.5	%
$V_{ASYS\_UVLO\_HYS}$	ASYS UVLO Hysteresis	400 mV for 2.4 V falling threshold		100 or 400		mV
$T_{ASYS\_SW\_DELAY}$		Time when ASYS voltage is switched between VIN and VBAT		0.5		ms
$V_{ASYS\_PREWARNING}$	ASYS Pre-Warning Threshold Accuracy	ASYS falling, I²C programmable		3.3 3.4 3.5 3.6		V
%$V_{ASYS\_PREWARNING}$	ASYS Pre-Warning Threshold Accuracy		-4		+4	%
$V_{ASYS\_PREWARNING\_HYS}$	ASYS Pre-warning Threshold Hysteresis			100		mV
VBAT_BKUP						
VBAT_BKUP UVLO		VBAT_BKUP falling edge		1.9		V
VBAT_BKUP UVLO Accuracy			-5		5	%
VBAT_BKUP UVLO Hysteresis				100		mV
PROTECTION[1]						
$T_{WARNING}$	Pre-warning temperature	2-bit programmable, T_WARNING [1:0]		75 80 85 90		°C
$T_{WARNING\_HYS}$	Pre-warning threshold Hysteresis			20		°C
T_{SHDN}	Thermal shutdown	3-bit programmable,THEM_ SHDN [2:0], in 5 °C steps		95 to 125		°C
T_{SHDN_HYS}	Thermal shutdown Hysteresis			20		°C
WATCHDOG & SAFETY TIMER						
T_{WD_TIMER} Range	Watchdog Timer	When enabled via I²C Programming	-15%	Disable 16	+15%	s

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Table 80. EC table for Top level*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
				32 64		
T_{CHG_PREQ}	Pre-qualification Charging Safety Timer Range	I^2C Programmable, 15 min/step **Note: When under thermal fold- back status, the timer extends by 2x automatically**	-15%	15 30 45 60	+15%	min
T_{CHG_FAST}	Fast (CC and CV) Charging Safety Timer Range	I^2C Programmable, 2hr/step **Note: When under thermal fold- back status, the timer extends by 2x automatically**	-15%	3 5 7 9	+15%	hrs
POWER UP/DOWN SEQUENCE TIMING[1]						
$T_{PWUP\_DLY\_INI}$	Power up Initial delay	Time from ON signal asserts to the first output rail reaches 90 % of its nominal value		2		ms
$T_{PWDN\_DLY\_INTERVAL}$	Power down interval delay	Delay between power rail		2		ms
$T_{PWUP\_DLY\_INTERVAL}$	Power up interval delay	For power-up: this is the time from previous voltage rail reaches 90 % of its nominal value to the time when the following voltage rail reaches its 90 % nominal value For power-down: this is the time from the previous voltage rail starts falling to the time the following rail starts falling		1		ms

[1] Guaranteed by design and characterization; not tested in production.

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13.2 Battery charger

Table 81. EC table for Linear Charger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LINEAR CHARGER						
V_{BAT_REG}	V_{BAT} regulation voltage range	I²C programmable, 20 mV/step	3.60		4.60	V
%V_{BAT_REG}	V_{BAT_REG} Regulation Voltage Accuracy	I_{OUT}=0 mA to 200 mA; VIN= 5 V, T_{amb}=25 °C	-0.75		0.75	%
		I_{OUT}=0 mA to 200 mA; V_{IN}= 5 V, T_{amb}=-40 °C to +85 °C	-1		1	%
I_{CHG_CC}	Constant charging current value	I²C programmable, V_{BAT_REG} > V_{BAT} > V_{BAT_LOW}; V_{IN} = 5 V	5		315	mA
%I_{CHG_CC}	I_{CHG_CC} Accuracy	V_{BAT_REG} > V_{BAT} > V_{BAT_LOW}; V_{IN} = 5 V				
		I_{CHG_CC} > 40 mA	-6		+6	%
		I_{CHG_CC} ≤ 40 mA	-12		+12	%
$\Delta V_{BAT\_REG\,(HOT)}$	V_{BAT_REG} reduction in warm condition	T3 < V_{TS} < T4 in TS enabled	120	140	160	mV
$R_{DS\_ON\_VIN\_TO\_ASYS}$ [1]	R_{DS_ON} between VIN and ASYS	VIN = 5 V at 50 mA		250	360	mΩ
$R_{DS\_ON\_ASYS\_TO\_VBAT}$ [1]	R_{DS_ON} between ASYS and VBAT	VBAT = 3.8 V at 50 mA		130	175	mΩ
DEAD BATTERY IN PRECHARGE MODE						
V_{BAT_DEAD}	Dead battery charge to low battery charge transition threshold	[Note: reserve 2-bit MTP for programmability, 1.7 V/1.8 V/1.9 V/2.0 V]		1.9		V
%V_{BAT_DEAD}	V_{BAT_DEAD} accuracy		-4.5		+4.5	%
$t_{DGL\_BAT\_DEAD2LOW}$	Deglitch time from dead battery charge to low battery charge transition			50		µs
I_{CHG_DEAD}		I²C programmable,1 mA/step	1		63	mA
%I_{CHG_DEAD}	I_{CHG_DEAD} accuracy	V_{BAT} =1 V, I_{CHG_DEAD} =4 mA	-12		+12	%
LOW BATTERY IN PRECHARGE MODE						
V_{BAT_LOW}	Precharge to fast-charge transition threshold	[Note: reserve 2-bit MTP for programmability, 2.3 V/2.4 V/2.5 V/2.6 V]		2.5		V
%V_{BAT_LOW}	V_{BAT_LOW} Accuracy		-3.5		+3.5	%
$t_{DGL\_BAT\_LOW2CC}$	Deglitch time on pre-charge to fast-charge transition			50		µs
I_{CHG_LOW}		I²C programmable,1 mA/step	1		63	mA
%I_{CHG_LOW}	I_{CHG_LOW} Accuracy	V_{BAT} =2 V, I_{CHG_DEAD} =8 mA	-10		+10	%
$t_{DGL\_BAT\_CC2LOW}$	Deglitch time from fast-charge to low battery charge transition			50		ms
TOP-OFF MODE						

Table 81. EC table for Linear Charger...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CHG_TOPOFF}	I_{CHG_TOPOFF} programmed value	I^2C programmable,1 mA/ step	1		63	mA
I_{CHG_TOPOFF} Accuracy		$I_{CHG\_TOPOFF} \geq 8$ mA	-15		+15	%
		$I_{CHG\_TOPOFF} < 8$ mA; test 4 mA only in production	-20		+20	%
$t_{DGL\_BAT\_CC2TOPOFF}$	I_{CHG_TOPOFF} detection deglitch time on fast charging to top-off charging transition			20		ms
RECHARGE MODE						
$V_{BAT\_RESTART}$	Charging restart threshold voltage	When below VBAT_ REG [Note: reserve 1-bit MTP bit to set the typical value, 140 mV or 240 mV]	95	140	165	mV
			185	240	270	
$t_{DGL\_BAT\_RESTART}$	Deglitch time, recharge threshold detected			50		ms
BATTERY PRESENCE DETECTION						
$I_{BAT\_DET\_SINK}$	Sink current during battery detection	V_{IN} = 5 V; Battery absent		5		mA
$t_{DGL(BAT\_DET\_SINK)}$	Deglitch time, for sinking current	V_{IN} = 5 V; Battery absent		300		ms
$I_{BAT\_DET\_SOURCE}$	Source current during battery detection	V_{IN} = 5 V; Battery absent		5		mA
$t_{DGL(BAT\_DET\_SOURCE)}$	Deglitch time, for sourcing current	V_{IN} = 5 V; Battery absent		300		ms
$V_{BAT\_DET\_LOW}$	Battery detection lower threshold	V_{IN} = 5 V; Battery absent [Note: reserve 2-bit MTP for programmability, 1. 7 V/1.8 V/1.9 V/2.0 V]		1.9		V
$V_{BAT\_DET\_UP}$	Battery detection upper threshold	V_{IN} = 5 V; Battery absent [Note: reserve 2-bit MTP for programmability, 3. 2 V/3.3 V/3.4 V/3.5 V]		3.4		V
BATTERY-PACK NTC MONITOR (TS)						
$I_{NTC-10 k}$	NTC thermistor bias current	$V_{TS} <$ ASYS-200 mV	44 (-12 %)	50	56 (+12 %)	µA
$I_{NTC-DIS-10 k}$	10 k NTC bias current when charging is disabled	$V_{TS} <$ ASYS-200 mV	4.4 (-12 %)	5	5.6 (+12 %)	µA
$V_{TS(0 \,°C)}$	TS threshold voltage at 0 °C	NTC_BETA_SEL [2:0] = 000	1.171	1.372	1.45	V
$V_{TS(0 \,°C)\_HYS}$	$V_{TS(0 \,°C)}$ Hysteresis Threshold			110		mV
$V_{TS(10 \,°C)}$	TS threshold voltage at 10 °C	NTC_BETA_SEL [2:0] = 000	0.813	0.900	0.999	V
$V_{TS(10 \,°C)\_HYS}$	$V_{TS(10 \,°C)}$ Hysteresis Threshold			70		mV
$V_{TS(45 \,°C)}$	TS threshold voltage at 45 °C	NTC_BETA_SEL [2:0] = 000	0.205	0.246	0.303	V
$V_{TS(45 \,°C)\_HYS}$	$V_{TS(45 \,°C)}$ Hysteresis Threshold			24		mV

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Table 81. EC table for Linear Charger*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TS(60\ °C)}$	TS threshold voltage at 60 °C	NTC_BETA_SEL [2:0] = 000	0.128	0.151	0.187	V
$V_{TS(60\ °C)\_HYS}$	$V_{TS(60\ °C)}$ Hysteresis Threshold			20		mV
$T_{DGL\ (TS)}$	Deglitch time for TS pin			50		ms
C_{TS}	Maximum Decoupling Capacitor			10		nF
THERMAL REGULATION [1]						
$T_{THEM\_REGULATION}$	Thermal regulation (fold-back) range	I^2C Programmable, 5 °C/step	80		115	°C
$T_{THEM\_REGULATION\_HYS}$	Thermal regulation (fold-back) Hysteresis			20		°C

[1]   Guaranteed by design and characterization; not tested in production.

13.3 BUCK1 (SW1)

Table 82. EC table for BUCK1 (SW1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN(SW1)}$	Input voltage range for CORE BUCK	Input is PSYS1, guaranteed by design	2.5		5.5	V
$I_{OUT(SW1)\ MAX}$	Max Output Current	Over V_{PSYS1}, guaranteed by design	250			mA
V_{SW1} Range	Output range for CORE BUCK	I^2C programmable from 0.5 V to 1.5 V in 25 mV/step, a fixed 1.8 V	0.5		1.5	V
V_{SW1_OUT} Accuracy	CORE BUCK DC Output Accuracy	Over full V_{PSYS1}, $I_{OUT(SW1)}$, -40 °C ≤ T_{amb} ≤ +85 °C, for all V_{SW1_OUT} except for 500 mV and 1.8 V	-3		+3	%
		Over full V_{PSYS1}, $I_{OUT(SW1)}$, -40 °C ≤ T_{amb} ≤ +85 °C, for only V_{SW1_OUT} =1.8 V	-3.5		+3.5	
		Over full V_{PSYS1}, $I_{OUT(SW1)}$, -40 °C ≤ T_{amb} ≤ +85 °C, for only V_{SW1_OUT} =0.5 V	-4		+4	
$\Delta V_{SW1} / \Delta V_{PSYS1}$	DC Line regulation	$V_{SW1(NOM)}$+0.5 V < V_{PSYS1} < 5.5 V, $I_{OUT(SW1)}$ = 250 mA		0.15		%/V
$\Delta V_{SW1} / \Delta I_{OUT(SW1)}$	DC Load regulation	0 mA < $I_{OUT(SW1)}$ < 250 mA		0.008		%/mA
$T_{ON\ (SW1)}$		-40 °C ≤ T_{amb} ≤ +85 °C [1]	110	240	350	ns
$I_{IN(SW1)}$[1]	Quiescent current	SW1 enabled, $I_{OUT(SW1)}$ = 0, no switching		700		nA
Inductor value	L			2.2		µH
$R_{DSON(SW1)}$[1]	High Side P-FET R_{DSON}	V_{PSYS1}=5 V		500	900	mΩ
	Low Side N-FET R_{DSON}	V_{PSYS1}=5 V		250	450	
$R_{STDN(SW1)}$	SW1 Output Active Discharge Resistance			50		Ω
$I_{LIM(SW1)}$	Internal Peak Current Limit	Cycle by cycle peak current limit	700	950	1200	mA
$t_{ONMIN(SW1)}$	Minimum On-Time			50		ns
$t_{OFFMIN(SW1)}$	Minimum-Off Time			10		ns
$t_{SSTART(SW1)}$	Soft-start time	V_{SW1OUT}=1.2 V		1.2		ms
Efficiency[1]	V_{PSYS1}=5 V, V_{SW1OUT}=1.5 V	@I_{OUT}=10 µA		> 76		%
		@I_{OUT}=100 µA		> 84		%
		@I_{OUT}=65 mA		> 86		%

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Table 82. EC table for BUCK1 (SW1)...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		@I_{OUT}=125 mA		> 86		%
		@I_{OUT}=250 mA		> 84		%

[1] Guaranteed by design and characterization; not tested in production.

13.4 BUCK2 (SW2)

Table 83. EC table for BUCK2 (SW2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN(SW2)}$	Input voltage range for SW2	Input is V_{PSYS2}	2.5		5.5	V
$I_{OUT(SW2)MAX}$	Maximum Output Current	Over V_{PSYS2}	500			mA
V_{SW2_RANGE}	Output range for SW2	I^2C programmable, 25 mV/step	1.5		2.1	V
			2.7		3.3	
$V_{SW2\_Accuracy}$	SW2 DC Output Accuracy	Over full V_{PSYS2}, $I_{OUT(SW2)}$, T_{amb}=room temp	-2		2	%
		Over full V_{PSYS2}, $I_{OUT(SW2)}$, temperature range	-3		3	%
ΔV_{SW2} / ΔV_{PSYS2}	DC Line regulation	$V_{SW2OUT(NOM)}$+0.5 V < V_{PSYS2} < 5.5 V, $I_{OUT(SW1)}$ = 500 mA		0.15		%/V
ΔV_{SW2} / $\Delta I_{OUT(SW2)}$	DC Load regulation	0 mA < $I_{OUT(SW1)}$ < 500 mA		0.008		%/mA
$T_{ON (SW2)}$			250	360	490	ns
IIN(SW2)[1]	Quiescent current	SW2 enabled, $I_{OUT(SW2)}$ = 0, no switching		700		nA
Inductor value	L			2.2		µH
$R_{DSON(SW2)}$[1]	High Side P-FET RDSON	V_{PSYS2} = 5 V		250	450	mΩ
	Low Side N-FET RDSON	V_{PSYS2} = 5 V		125	250	
$R_{STDN(SW2)}$	SW2 Output Active Discharge Resistance			50		Ω
$I_{LIM(SW2)}$	Peak Current Limit	Cycle by cycle peak current limit	900	1300	1800	mA
$t_{ONMIN(SW2)}$	Min. On Time			50		ns
$t_{OFFMIN(SW2)}$	Max On Time			10		ns
$t_{SSTART(SW2)}$	Softstart time	V_{SW2OUT}=1.8 V		1.8		ms
Efficiency[1]	V_{PSYS2}5 V V_{SW2OUT} = 1.8 V	@I_{OUT}=10 µA		> 78		%
		@I_{OUT}=100 µA		> 87		
		@I_{OUT}=125 mA		> 88		
		@I_{OUT}=250 mA		> 88		
		@I_{OUT}=500 mA		> 86		

[1] Guaranteed by design and characterization; not tested in production.

13.5 LDO1 (Always-on LDO)

Table 84. EC table for LDO1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN_LDO1}	Input voltage range for Always- On LDO	Whichever is higher between VBAT_BKUP and ASYS	2.0		5.5	V
$I_{OUT\_LDO1\_MAX}$	Maximum Output DC Current		1			mA
$I_{OUT\_LDO1\_LIMIT}$	Internal Current Limit	LDO1_OUT = GND	1.4	3.3	7.0	mA
V_{LDO1_OUT} Range	LDO1 nominal output voltage	I^2C Programmable, 25 mV/step	1.700		1.900	V
V_{LDO1_OUT} Accuracy	LDO1 Output Voltage Accuracy	Over V_{IN_LDO1}, I_{OUT}= 0 to 1 mA	-3		+3	%
$\Delta V_{LDO1\_OUT} / (V_{LDO1\_OUT(NOM)} \times \Delta V_{IN\_LDO1})$	DC Line regulation	$V_{LDO1\_OUT(NOM)}$+0.5 V < V_{IN_LDO1} < 5 V, I_{OUT}= 1 mA		1		%/V
$\Delta V_{LDO1\_OUT} / (V_{LDO1\_OUT(NOM)} \times \Delta V \times \Delta I_{OUT})$	DC Load regulation	0 mA < I_{OUT} < 1 mA		1		%/mA
Power Supply Rejection Ratio (PSRR) [1]				40		dB
$I_{IN(LDO1)}$	Quiescent current	I_{OUT} =0 mA		94		nA
$V_{DROPOUT(LDO1)}$ [1] [2]	Dropout Voltage	I_{OUT}=1 mA			200	mV
$R_{STDN(LDO1)}$	LDO1 Output Active Discharge Resistance			50		Ω

[1] Guaranteed by design and characterization; not tested in production.
[2] Dropout voltage is defined as the input-to-output difference in the predefined load when the output is below 100 mV to the nominal regulation voltage.

13.6 LDO2 (System LDO)

Table 85. EC table for LDO2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN_LDO2}	Input voltage range	ASYS	2.5		5.5	V
$I_{OUT\_LDO2\_MAX}$	Maximum Output Current		250			mA
$I_{OUT\_LDO2\_LIMIT}$[1]	Internal Current Limit	LDO2_OUT = GND	300	450	600	mA
V_{LDO2_OUT} Range	LDO2 output voltage range	programmable 25mV steps	1.5		2.1	V
			2.7		3.3	
V_{LDO2_OUT} Accuracy	LDO2 Output Accuracy	Over V_{IN_LDO2}, I_{OUT}, temperature	-3.5		3.5	%
ΔV_{LDO2_OUT} / ($V_{LDO2\_OUT(NOM)}$ x ΔV_{IN_LDO2})	DC Line regulation	$V_{LDO2\_OUT(NOM)}$+0.5 V < V_{IN_LDO2} < 5.5 V, I_{OUT} = 250 mA		0.35		%/V
ΔV_{LDO2_OUT} / ($V_{LDO2\_OUT(NOM)}$ x ΔI_{OUT})	DC Load regulation	0 mA < I_{OUT} < 250 mA		0.0065		%/mA
PSRR[1]	Power Supply Rejection Ratio			40		dB
$I_{IN(LDO2)}$	Quiescent current	I_{OUT} = 0 mA		450		nA
$V_{DROPOUT(LDO2)}$[2]	Dropout Voltage	I_{OUT} = 100 mA			150	mV
$R_{STDN(LDO2)}$	LDO2 Output Active Discharge Resistance			150		Ω

[1] Guaranteed by design and characterization; not tested in production.
[2] Dropout voltage is defined as the input-to-output difference in the predefined load when the output is below 100mV to the nominal regulation voltage.

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13.7 I²C Interface and Logic I/O

Table 86. EC table for I²C and Logic

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SERIAL INTERFACE (SCL & SDA)						
V_{PULLUP} Range[1]	Pullup Voltage Range		1.5		3.6	V
F_{I2C}	I²C Clock frequency	On SCL	0		1000	kHz
V_{IH}	High-level Input voltage		1.5			V
V_{IL}	Low-level Input voltage				0.5	V
V_{hys}	Hysteresis of Schmitt trigger inputs		0.01			V
V_{OL}	Low-level output voltage at 3 mA sink current		0		0.4	V
I_{OL}	Low-level output current	V_{OL} = 0.4 V; Standard and Fast modes	3			mA
		V_{OL} = 0.6 V; Fast mode	6			mA
I_{IL}	Low-level input current	Pin voltage: 0.1xVpullup to 0.9x Vpullup max	-10		10	µA
C_I	Capacitance of IO pin				10	pF
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26			µs
t_{LOW}	LOW period of I²C clock	Fast mode plus	0.5			µs
t_{HIGH}	HIGH period of I²C clock	Fast mode plus	0.26			µs
$t_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26			µs
$t_{HD,DAT}$	Data Hold time	Fast mode plus	0			µs
$t_{SU,DAT}$	Data Setup time	Fast mode plus	50			ns
t_r	Rise time of I2C_SCL and I2C_SDA signals	Fast mode plus			120	ns
t_f	Fall time of I2C_SCL and I2C_SDA signals	Fast mode plus			120	ns
$t_{SU,STO}$	Setup time for STOP condition	Fast mode plus	0.26			µs
t_{BUF}	Bus free time between STOP and START condition	Fast mode plus	0.5			µs
$t_{VD,DAT}$	Data valid time	Fast mode plus			0.45	µs
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode plus			0.45	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter		0		50	ns

Table 86. EC table for I^{2}C and Logic...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MODESEL0/MODESEL1						
V_{IH1}	Logic Input High Threshold		1.5			V
V_{IL1}	Logic Input Low Threshold				0.4	V
I_{LK1}	Logic Pin Leakage Current	Pulled up to 5.0 V		0.1	1	µA
$t_{debounce\_1}$	Debounce time for MODESEL0, MODESEL1			1		µs
ON						
V_{IH2}	Logic Input High Threshold	Note: ON pin internally pulled up, no external pull-up voltage needed.	70 % * VBAT			V
V_{IL2}	Logic Input Low Threshold				0.4	V
$t_{debounce}$	Debounce time for ON	To initiate the default power-up sequence		200		µs
SYSRSTn, INTB						
V_{OL1}	Low-level output voltage at 1 mA sink current				0.5	V
I_{LK2}	Logic Pin Leakage Current	Pulled up to 5.0 V		0.01	0.1	µA
$V_{PULLUP1}$	Minimum Supply Voltage for valid Open-drain signal		1.5			V

[1]   Guaranteed by design and characterization; not tested in production.

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14 Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;
24 terminals; body 3 x 3 x 0.85 mm   **SOT905-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A[1] max	A_1	b	b_1	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	L_1	LC	v	w	y	y_1
mm	1	0.05 0.00	0.25 0.15	0.45 0.35	0.2	3.1 2.9	2.05 1.75	3.1 2.9	2.05 1.75	0.4	1.8	1.8	0.35 0.15	0.1 0.0	0.3 0.2	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT905-1	- - -	- - -	- - -			~~06-03-13~~ 06-03-31

Figure 12. Package outline SOT905-1 (HVQFN24)

DATE: 03 AUG 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01151D	REVISION: A
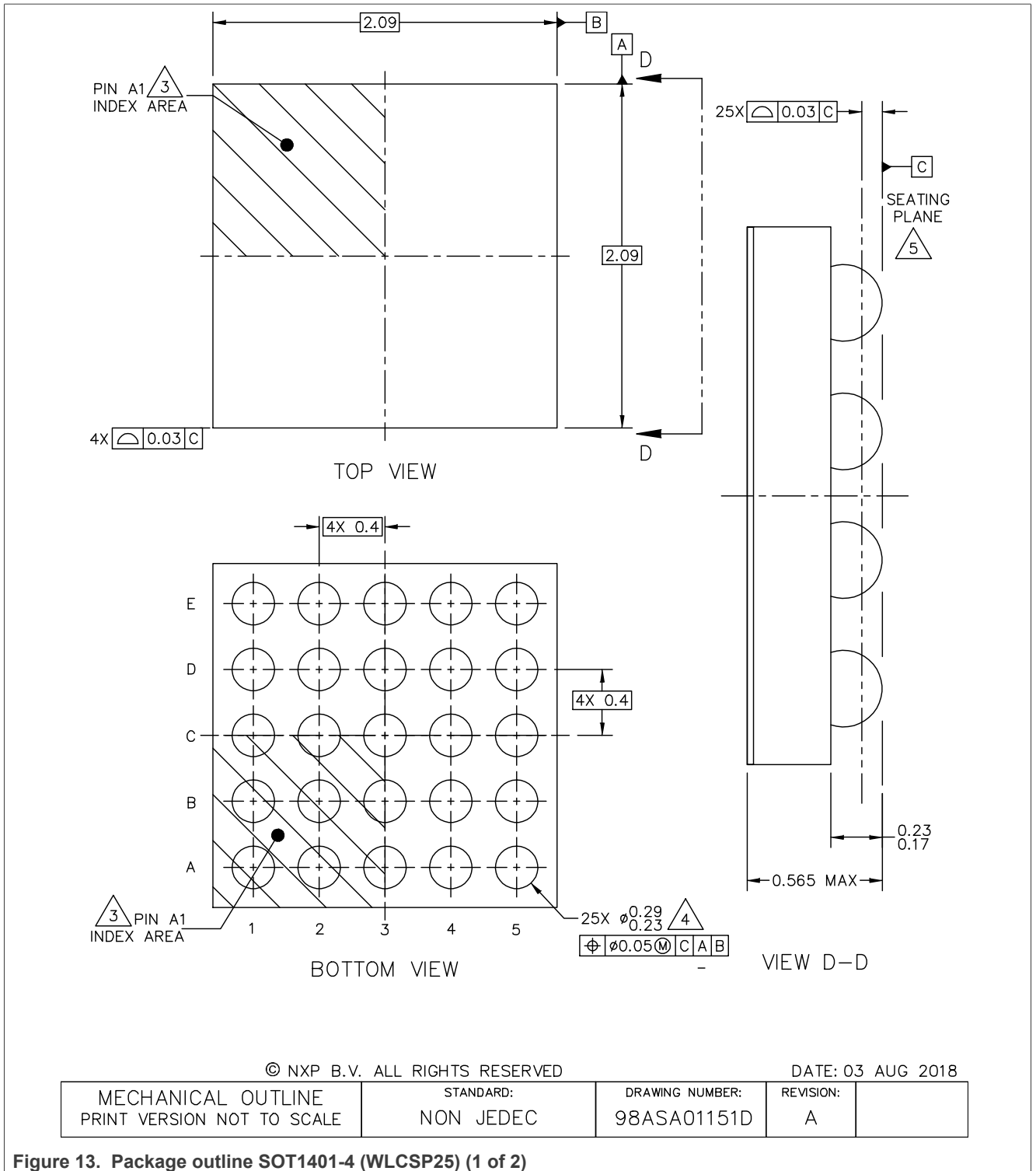
Figure 13. Package outline SOT1401-4 (WLCSP25) (1 of 2)

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 03 AUG 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01151D	REVISION: A

Figure 14. Package outline SOT1401-4 (WLCSP25) (2 of 2)

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15 Packing information

15.1 SOT905-1 HVQFN24; reel dry pack, SMD, 7" Q2 standard product orientation ordering code (12NC) ending 547

15.1.1 Dimensions and quantities

Table 87. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box
178 × 12	1400	1

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

15.1.2 Product orientation

Pin 1 is in quadrant 2.

Figure 15. Product orientation in carrier tape

15.1.3 Carrier tape dimensions

Not drawn to scale.
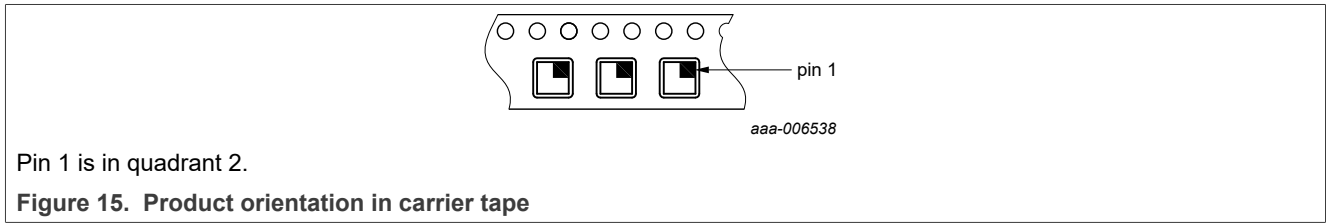
Figure 16. Carrier tape dimensions
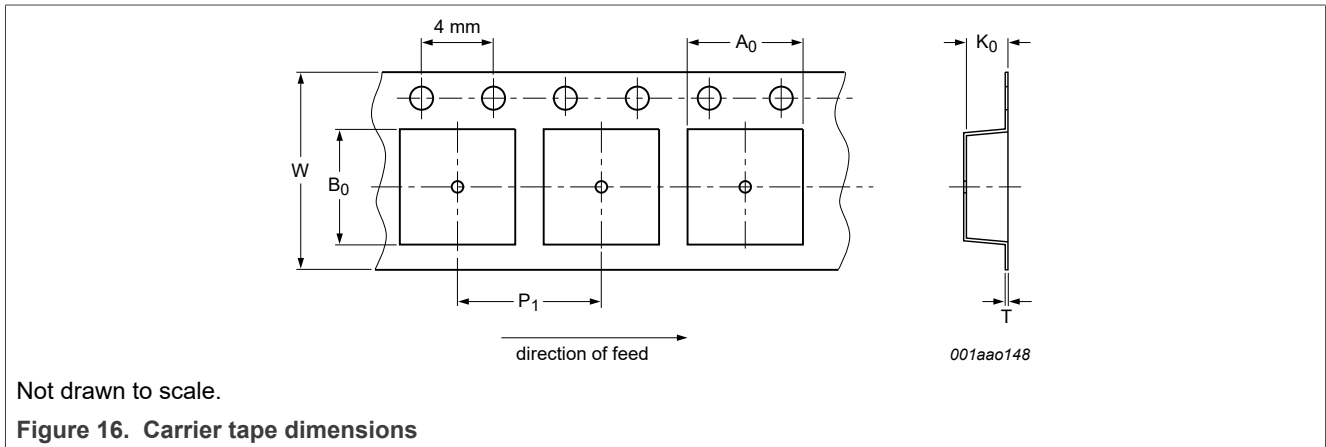
Table 88. Carrier tape dimensions
In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
3.30 ± 0.1	3.30 ± 0.1	1.10 ± 0.1	0.30 ± 0.5	8.0 ± 0.1	12 +.3/-.0

15.2 SOT1401-4 WLCSP25; reel dry pack, SMD, 7" Q1 standard product orientation ordering code (12NC) ending 012

15.2.1 Dimensions and quantities

Table 89. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box
180 × 8	3000	1

[1]   d = reel diameter; w = tape width.
[2]   Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

15.2.2 Product orientation

aaa-017857

Ball 1 is in quadrant 1.

Figure 17. Product orientation in carrier tape

15.2.3 Carrier tape dimensions

Not drawn to scale.
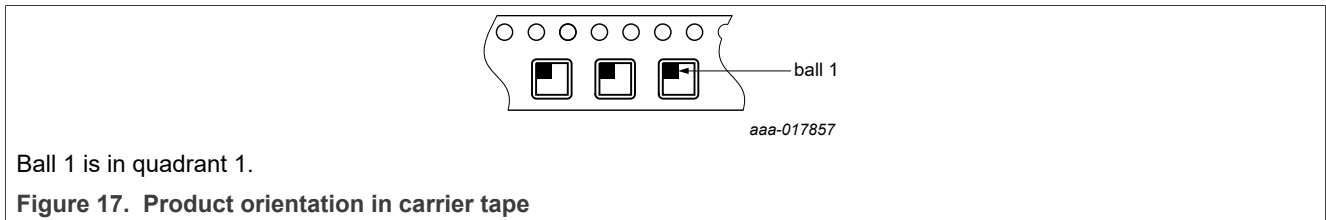
Figure 18. Carrier tape dimensions
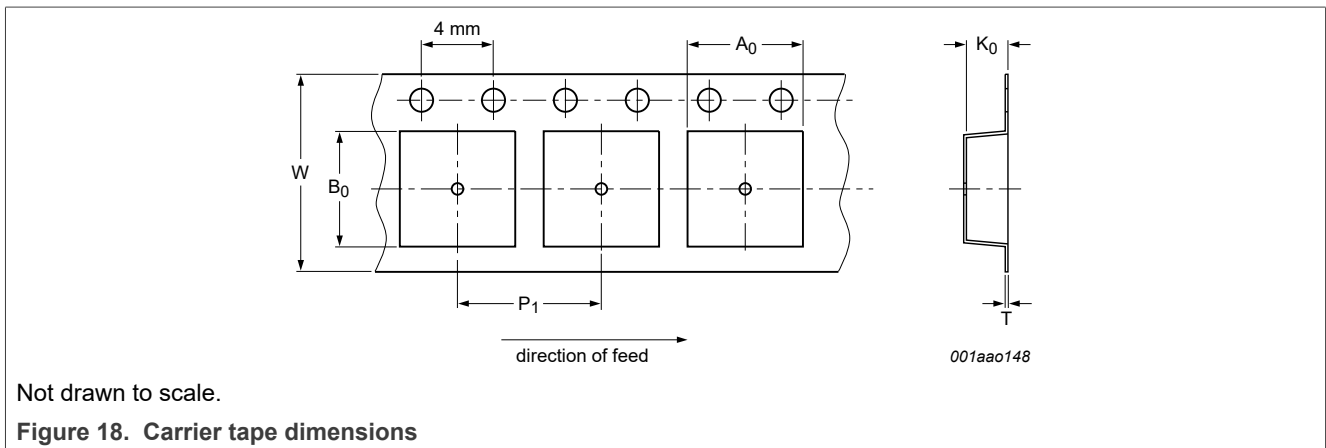
Table 90. Carrier tape dimensions
In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
2.27 ± 0.05	2.27 ± 0.05	0.67 ± 0.05	0.25 ± 0.02	4.0 ± 0.10	8 +0.30/-0.10

16 Revision history

Table 91. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9420 v.4.2	20230726	Product data sheet	CIN 202307022I	PCA9420 v.4.1
Modifications:	• Section 8: Added Section 8.2 and Section 8.2.1 • Section 8.13: Changed "Charging current limiting" to "JEITA compliant charging current limiting"; added new bullet "If VIN is not present.…" • Section 8.10: Updated description • Table 6: Updated conditions for VIN overcurrent (ILIM) and ASYS undervoltage			
PCA9420 v.4.1	20230530	Product data sheet	-	PCA9420 v.4.0
PCA9420 v.4.0	20221128	Product data sheet	CIN 202211010I	PCA9420 v.3.1
PCA9420 v.3.1	20220113	Product data sheet	-	PCA9420 v.3.0
PCA9420 v.3.0	20211208	Product data sheet	CIN 202111016I	PCA9420 v.2.0
PCA9420 v.2.0	20210126	Product data sheet	-	PCA9420 v.1.1
PCA9420 v.1.1	20191024	Product data sheet	-	PCA9420 v.1.0
PCA9420 v.1.0	20190601	Product data sheet	-	-

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17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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