NXP Semiconductors
Application Note

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QorIQ LS1046A Design Checklist

1 About this document

This document provides recommendations for new designs based on the LS1046A/LS1026A processor, which is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the NXP Value Performance line of QorIQ communications processors.

This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

NOTE

This document applies to the LS1046A and LS1026A devices. For a list of functionality differences, see the appendices in *QorIQ LS1046A Reference Manual* (document LS1046ARM).

2 Before you begin

Ensure you are familiar with the following NXP collateral before proceeding:

- *QorIQ LS1046A, LS1026A Data Sheet* (document LS1046A)
- *QorIQ LS1046A Reference Manual* (document LS1046ARM)

Contents

3 Simplifying the first phase of design

Before designing a system with the chip, it is recommended that you familiarize yourself with the available documentation, software, models, and tools.

This figure shows the major functional units within the LS1046A chip.

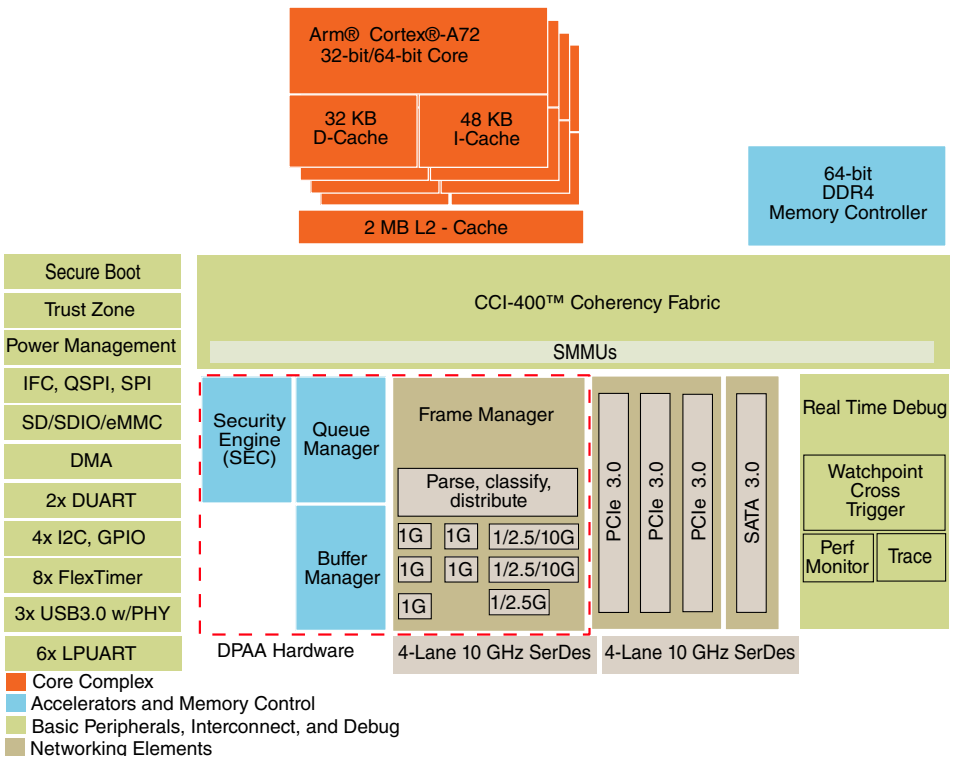

Figure 1. LS1046A block diagram

This figure shows the major functional units within the LS1026A chip.

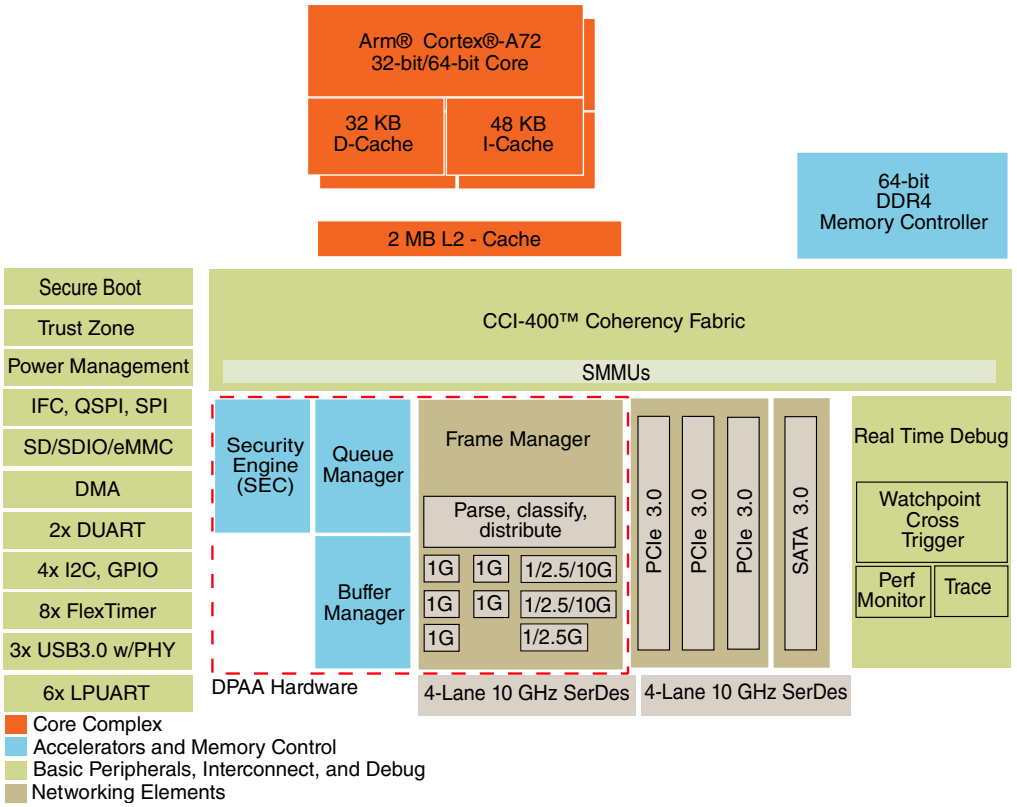

Figure 2. LS1026A block diagram

3.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
	Related collateral	
LS1046ACE	*LS1046A Chip Errata* **NOTE:** This document describes the latest fixes and workarounds for the chip. It is strongly recommended that this document be thoroughly researched prior to starting a design with the chip.	Contact your NXP representative
LS1046A	*QorIQ LS1046A, LS1026A Data Sheet*	www.nxp.com
LS1046AFS	*QorIQ LS1046A and LS1026A Communication Processors - Fact Sheet*	www.nxp.com
LS1046ARM	*QorIQ LS1046A Reference Manual*	www.nxp.com
LS1046APB	*QorIQ LS1046A Product Brief*	www.nxp.com
AN5125	*Introduction to Device Trees - Application note*	
cortex_a72_mpcore_trm_100095_0002_03_en	*ARM® Cortex®-A72 MPCore Processor - Technical Reference Manual*	Attached with LS1046ARM

Table continues on the next page...

Table 1. Helpful tools and references (continued)

ID	Name	Location
AN4871	*Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array Packages*	www.nxp.com
AN5097	*Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces - Application Note*	www.nxp.com
AN4311	*SerDes Reference Clock Interfacing and HSSI Measurements Recommendations*	www.nxp.com
AN5348	*Using QorIQ LS1046ARDB in PCIe Endpoint Mode*	www.nxp.com
Software tools		
	CodeWarrior Development Software for ARM® v8 64-bit based QorIQ LS-Series Processors	www.nxp.com
	Software Development Kit for LS1046A	www.nxp.com
Hardware tools		
	CodeWarrior TAP	www.nxp.com
	QorIQ LS Processor Probe Tips for CodeWarrior TAP	www.nxp.com
	QorIQ LS1046A reference design board	www.nxp.com
Models		
IBIS	To ensure first path success, NXP strongly recommends using the IBIS models for board-level simulations, especially for SerDes and DDR characteristics.	Contact your NXP representative
BSDL	Use the BSDL files in board verification.	Contact your NXP representative
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	Contact your NXP representative
Available training		
-	Our third-party partners are part of an extensive alliance network. More information can be found at www.NXP.com/alliances.	www.nxp.com/alliances
-	Training materials from past Smart Network Developer's Forums and NXP Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the chip.	www.nxp.com/alliances

NOTE

Design requirements in the device datasheet supersede requirements mentioned in design checklist and design requirements mentioned in design checklist supersede the design/ implementation of the NXP reference design (RDB) system.

3.2 Product revisions

This table lists the system version register (SVR) and ARM core main ID register (TRCIDR1) values for the various chip silicon derivatives.

Table 2. Chip product revisions

Part	Device revision	ARM® Cortex®-A72 MPCore processor revision	ARM core main ID register	System version register value	Note
LS1046A	1.0	r0p2	0x410F_D081h	0x8707_0110h	Without security
LS1046AE	1.0	r0p2	0x410F_D081h	0x8707_0010h	With security
LS1026A	1.0	r0p2	0x410F_D081h	0x8707_0910h	Without security
LS1026AE	1.0	r0p2	0x410F_D081h	0x8707_0810h	With security

4 Power design recommendations

4.1 Power pin recommendations

Table 3. Power and ground pin termination checklist

Signal name	Used		Not used	Completed
Power				
OV_{DD}	General I/O supply IFC, SPI, GIC (IRQ 0/1/2), Temper_Detect, System control and power management, SYSCLK, DDR_CLK, DIFF_SYSCLK, GPIO2, GPIO1, eSDHC[4-7]/VS/ DAT123_DIR/DAT0_DIR/ CMD_DIR/SYNC), Debug, JTAG, RTC, FTM5/6/7, POR signals	1.8 V	Must remain powered	
DV_{DD}	DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, eSDHC_CD/WP	1.8 /3.3 V	Must remain powered	
EV_{DD}	eSDHC supply - switchable eSDHC_DAT[0:3], eSDHC_CMD, eSDHC_CLK, FTM4_CH[6:7], LPUART3, LPUART5, LPUART6	1.8/3.3 V dynamically switchable	Must remain powered	
LV_{DD}	Ethernet Interface 1/2, Ethernet management interface 1	1.8/2.5 V	Must remain powered	

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Table 3. Power and ground pin termination checklist (continued)

Signal name	Used		Not used	Completed
	(EMI1), TSEC_1588, GPIO1, GPIO3, FTM1/2, GIC (IRQ11)			
TV_{DD}	Ethernet management interface 2 (EMI2)	1.2/1.8/2.5 V	Must remain powered	
$G1V_{DD}$	DDR4 supply	1.2 V	Must remain powered	
SV_{DD}	SerDes core logic and receiver supply	0.9/1.0 V	Must remain powered	
XV_{DD}	SerDes transmitter supply	1.35 V	Must remain powered	
PROG_MTR	This pin must be connected or pulled down via a resistor to ground (GND).			
TA_PROG_SFP	SFP fuse programming override supply	Should only be supplied 1.8 V during secure boot programming. For normal operation, this pin needs to be pulled down through a resistor.		
TH_V_{DD}	Thermal Monitor Unit supply	1.8 V	Must remain powered	
V_{DD}	Supply for cores and platform	0.9/1.0 V	Must remain powered	
$TA\_BB\_V_{DD}$	Low power security monitor supply	0.9/1.0 V	Must remain powered	
AV_{DD}_CGA1	CPU cluster group A PLL1 supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_CGA2	CPU cluster group A PLL2 supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_PLAT	Platform PLL supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_D1	DDR PLL supply	1.8 V (independent supplies derived from board 1.8 V)	Must remain powered	
AV_{DD}_SD1_PLL1	SerDes1 PLL 1 supply	1.35 V (filtered off of XV_{DD} supply)	Must remain powered (no need to filter from XV_{DD})	
AV_{DD}_SD1_PLL2	SerDes1 PLL 2 supply	1.35 V (filtered off of XV_{DD} supply)	Must remain powered (no need to filter from XV_{DD})	
AV_{DD}_SD2_PLL1	SerDes2 PLL 1 supply	1.35 V (filtered off of XV_{DD} supply)	Must remain powered (no need to filter from XV_{DD})	
AV_{DD}_SD2_PLL2	SerDes2 PLL 2 supply	1.35 V (filtered off of XV_{DD} supply)	Must remain powered (no need to filter from XV_{DD})	
$SENSEV_{DD}$	V_{DD} sense pin	Sense pin, Must be connected to regulator feedback		
USB_HV_{DD}	USB PHY Transceiver supply	3.3 V	Tie to GND	
USB_SDV_{DD}	Analog and Digital HS supply for USBPHY	0.9/1.0 V	Tie to GND	
USB_SV_{DD}	Analog and Digital SS supply for USBPHY	0.9/1.0 V	Tie to GND	

Table continues on the next page...

Table 3. Power and ground pin termination checklist (continued)

Signal name	Used		Not used	Completed
GND	Core, platform and PLL ground	GND	Tie to GND	
SD_GND	SerDes core logic, transceiver and PLL ground	GND	Tie to GND	
SENSEGND	Ground sense pin	Connect to regulator feedback		

NOTE

For supported voltage/frequency/temperature range options, see the orderable part list of *QorIQ LS1046A and LS1026A Multicore Communications Processors* at www.nxp.com.

If all USB power supplies are connected to GND when USB is not used, the JTAG IEEE Std 1149.1-2001 Boundary Scan Register (BSR) will not shift contents between TDI and TDO. USB_SVDD must be powered in order for the USB BSR cells to shift. In this case, the USB boundary cells cannot observe or control USB pins. This affects the USB BSR cells during EXTEST, EXTEST_PULSE, EXTEST_TRAIN, CLAMP and SAMPLE. The only fails are related to USB IO's when USB_SVDD is powered on, and USB_SDVDD and USB_HVDD are powered off. If all USB power supplies are connected to GND, the other 1149.1 JTAG or DAP debug instructions will still operate.

4.2 Power system-level recommendations

Table 4. Power design system-level checklist

Item	Completed
General	
Ensure to meet all of the requirements in the data sheet, including power sequencing, power down requirements, THERMAL and MAXIMUM power dissipation, I/O power dissipation, and power on ramp rate. Approximately 100mW is consumed per 100MHz of FMAN frequency.	
Ensure the PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_D1. See the "PLL power supply filtering" section of this table.	
If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AV_{DD}_SD*m*_PLL*n* pins. Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AV_{DD} pins. However, instead of using a filter, it needs to be connected to the XV_{DD} rail through a 0 Ω resistor. See the "PLL power supply filtering" section of this table.	
Ensure the PLL filter circuits are placed as close to the respective AV_{DD}_SD*m*_PLL*n* pin as possible. If possible, a small cap for the filter should be placed directly at the pin. If no small cap for the filter is available, consider at least a standard decoupling cap, such as 0.1 µF.	
General Power supply decoupling	
Because of large address and data buses and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the device itself, so this requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TA_BB_V_{DD}, OV_{DD}, TV_{DD}, EV_{DD}, DV_{DD}, LV_{DD}, $G1V_{DD}$, SV_{DD}, and XV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, TA_BB_V_{DD}, OV_{DD}, TV_{DD}, EV_{DD}, DV_{DD}, LV_{DD}, $G1V_{DD}$, SV_{DD}, XV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.	

Table continues on the next page...

Table 4. Power design system-level checklist (continued)

Item	Completed
These capacitors typically should have a value of approximately 0.1 µF. However, larger values available in the given package, such as 10 µF for 0402 (supports 1.0 mm pitched parts) or 4.7 µF for 0201 (supports 0.8 mm pitched parts), may be used to provide both decoupling and intermediate capacitance for the power supply design. For example, a system may have 0.1 µF at the pin, but also needs 22 µF intermediate capacitance outside the package. Given routing escape density, it may be more beneficial to remove the 22 µF caps and replace the 0.1 µF with 4.7 µF to 10 µF 0201/0402. Thus, it allows more room for routing to escape as an option. It is best to have one decoupling capacitor at each pin location. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes for 1 mm pitched parts and 0201 for 0.8 mm pitched parts. As presented in the "Core and platform supply voltage filtering" section of this table, it is recommended that there be several medium and large sized bulk storage capacitors distributed around the PCB, feeding the V_{DD} and other planes (for example, TV_{DD}, EV_{DD}, DV_{DD}, LV_{DD}, $G1V_{DD}$, and so on), to enable quick recharging of the smaller chip capacitors.	
Provide sufficiently-sized power planes for the respective power rail. Use separate planes if possible; split (shared) planes if necessary. If split planes are used, ensure that signals on adjacent layers do not cross splits. Avoid splitting ground planes at all costs.	
Ensure the bulk capacitors have a low ESR rating to ensure the quick response time necessary.	
Ensure the bulk capacitors are connected to the power and ground planes through two vias, as necessary, to minimize inductance.	
Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply to be able to handle the chip's power requirements. Most regulators perform best with a mix of ceramic and other low ESR types, such as OSCON, POS, and other types of capacitor technologies.	
Core and platform supply voltage filtering	
The V_{DD} supply is normally derived from a high current switching power supply, which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator. Bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the necessary response time. They should also be connected to the power and ground planes through two vias at each side, if necessary, to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors. Most power supply designs work well with small ceramic caps at each pin, as discussed in the "General power supply decoupling" section of this table. But also nearby the SoC should be intermediate caps, such as 22 µF ceramic and larger 330 to 560 µF POS type caps, as an example. As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors should be chosen to maintain the positive transient power surges to less than V_{DD} + 50 mV (negative transient undershoot should comply with specification of VDD - 30 mV) for current steps of up to 50% to 100% rise and 100% to 50% of max current (based on maximum power in the data sheet) with a slew rate of 7 A/us. These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the MHz range. See the "General power supply decoupling" section of this table for further decoupling recommendations.	
PLL supply filtering (core, platform, DDR, filtered from 1.8 V source)	
All PLLs are provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CGA1/2, and AV_{DD}_D1 voltages must be derived directly from a 1.8 V voltage source, such as OV_{DD}, through a low frequency filter. The recommended solution for this type of PLL filtering is to provide independent filter circuits per PLL power supply, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range. Provide independent filter circuits per PLL power supply, as illustrated in the following figure. Where	

Table continues on the next page...

Table 4. Power design system-level checklist (continued)

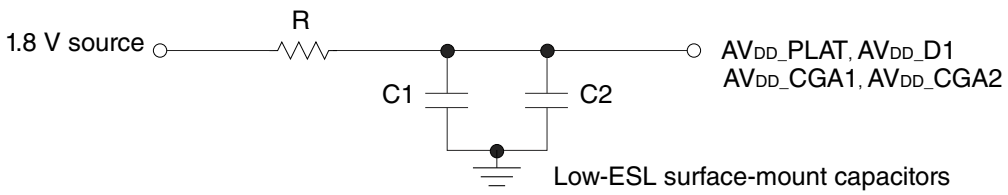
Item	Completed
• R = 5 Ω ± 5% • C1 = 10 µF ± 10%, 0603 or smaller, X5R or better (X7R or C0G are fine), with ESL ≤ 0.5 nH • C2 = 1.0 µF ± 10%, 0402 or 0201, X5R, with ESL ≤ 0.5 nH • Low-ESL surface-mount capacitors  Note the following: • Each AV_{DD} pin must have its own independent filter circuit. • Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}. • If done properly, it is possible to route directly from the capacitors to the AV_{DD} pins, without the added inductance of vias. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. • Placement should be such that the smaller capacitors are nearest to the AV_{DD} pin. If routing permits, the smallest cap would be best located at the pin of AV_{DD}. • **Caution:** These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	
PLL supply filtering (SerDes, filtered from XV_{DD})	
The AV_{DD}_SD*m*_PLL*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in the following figure. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, one for each side of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. Note the following: • Each AV_{DD} must have its own independent filter circuit. • AV_{DD}_SD*m*_PLL*n* should be a filtered version of XV_{DD}. • Voltage for AV_{DD} is defined at the pin of AV_{DD}. This is in contrast to the requirement, for example for the core PLL filter such as AV_{DD}_CGA*n*, which is measured at the input of the filter. • Placement should be such that the smaller capacitors are nearest to the AV_{DD} pin. If routing permits, the smallest cap would be best located at the pin of AV_{DD}. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • A 47 µF 0805 XR5 or XR7, 4.7 µF 0603 or smaller, and 0.0033 µF 0402 or 0.0033 µF 0201 capacitor are recommended. The size and material type are important. A 0.33 Ω ± 1% resistor is recommended. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.	

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Table 4. Power design system-level checklist (continued)

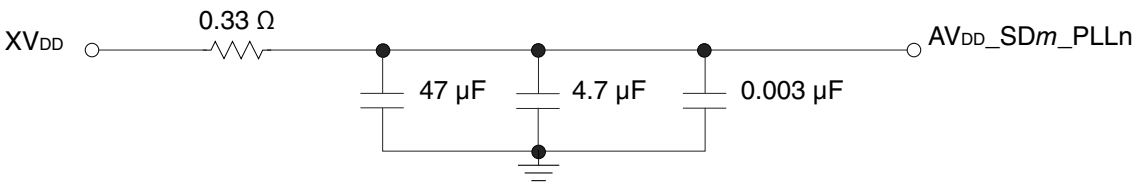
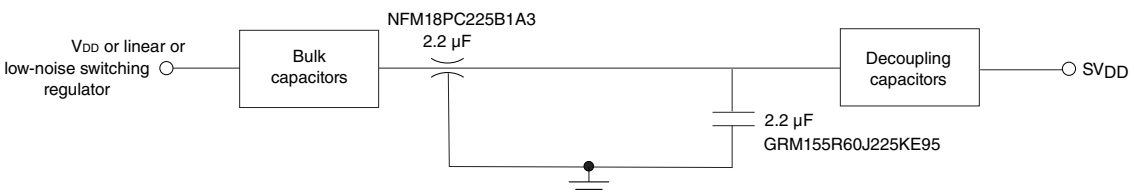
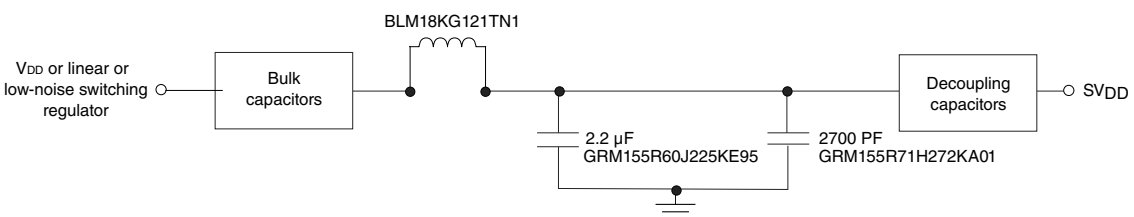
Item	Completed
	
SerDes power supply filtering	
The ferrite beads should be placed in parallel to reduce voltage droop. For the linear or low-noise switching regulator, 10 mVp-p, 50 kHz to 500 MHz is the noise goal. All traces should be kept short, wide, and direct. Use small area fill, if possible. The goal is to lower the impedance of this net, thus lowering the noise. SV_{DD} may be supplied by linear or low noise switching regulator or sourced by a filtered V_{DD}. Two example solutions for SV_{DD} filtering, where SV_{DD} is sourced from V_{DD}, linear or low noise switching regulator, are illustrated in Figure 3 and Figure 4. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 3. Primary SV_{DD} power supply filter circuit**  **Figure 4. Alternate SV_{DD} power supply filter circuit** Note the following: • See "Power-on ramp rate," in the data sheet for maximum SV_{DD} power-up ramp rate. • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
XV_{DD} may be supplied by a linear or low noise switching regulator. Two example solutions for XV_{DD} filtering, where XV_{DD} is sourced from a linear or low noise switching regulator, are illustrated in Figure 5 and Figure 6. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution	

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Table 4. Power design system-level checklist (continued)

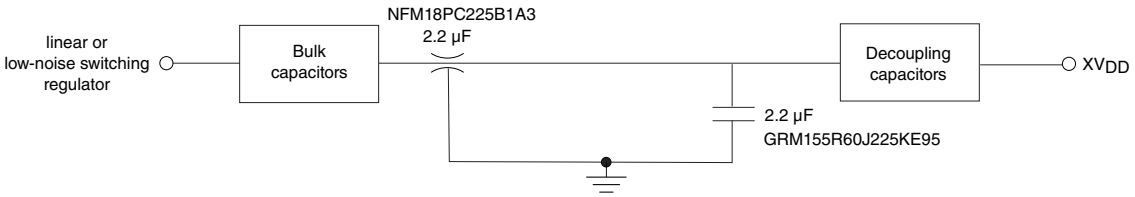
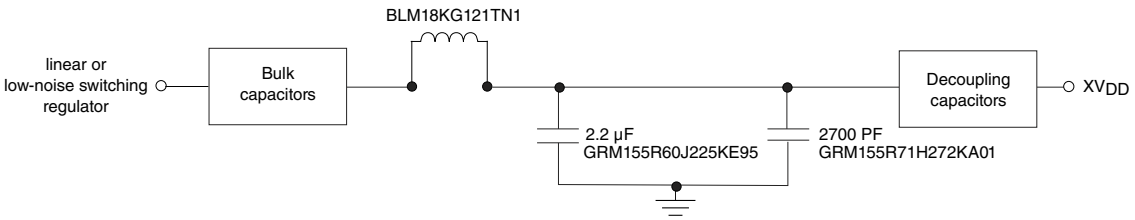
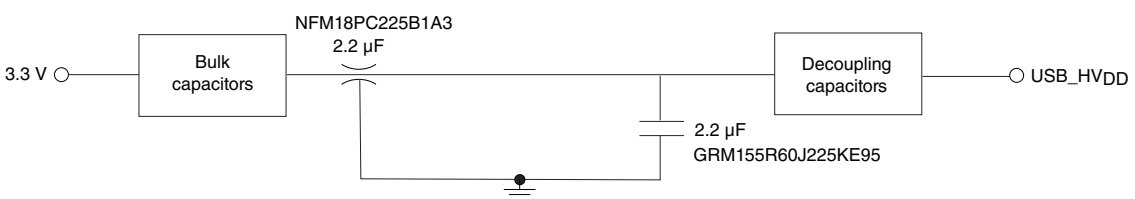
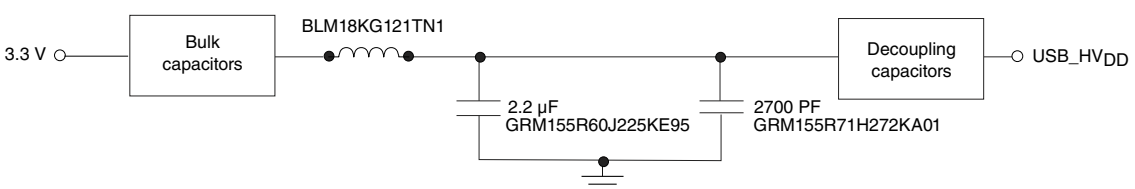
Item	Completed
 **Figure 5. Primary XV_{DD} power supply filter circuit**  **Figure 6. Alternte XV_{DD} power supply filter circuit** Note the following: • See "Power-on ramp rate," in the data sheet for maximum XV_{DD} power-up ramp rate. • It is recommended that an area fill or power plane split be provided for a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
USB_HV_{DD} may be supplied by a linear or low noise switching regulator, which may be the system-wide 3.3 V power supply. Two example solutions for USB_HV_{DD} filtering, where USB_HV_{DD} is sourced from a linear or low noise switching regulator, are illustrated in Figure 7 and Figure 8. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 7. Primary USB_HV_{DD} power supply filter circuit**  **Figure 8. Alternate USB_HV_{DD} power supply filter circuit**	

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Table 4. Power design system-level checklist (continued)

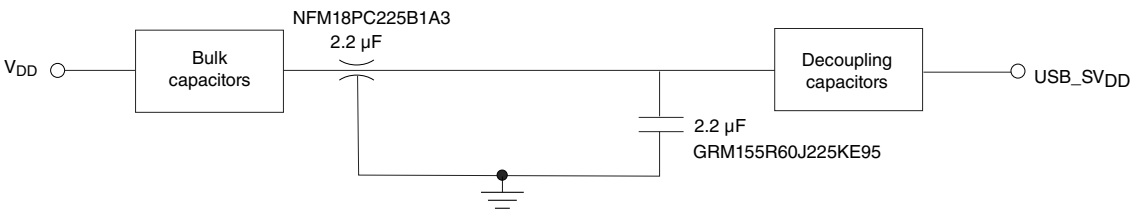
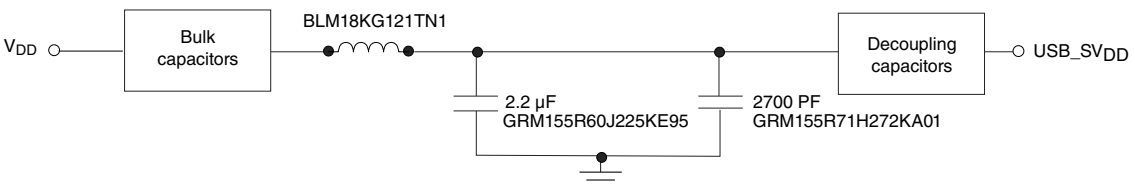
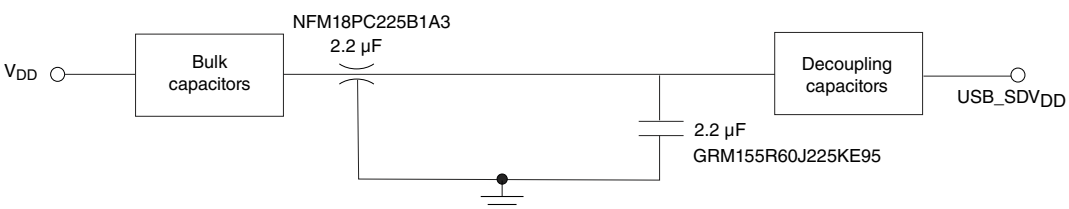
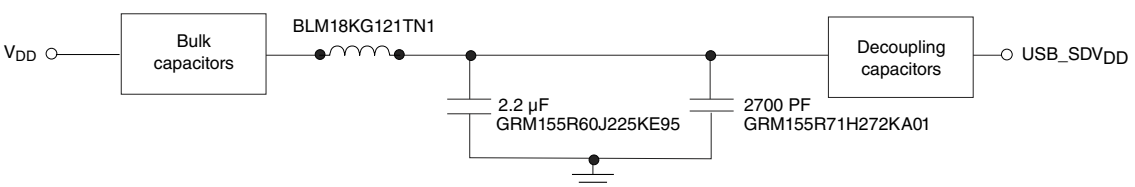
Item	Completed
Note the following: • It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	
USB_SV_{DD} and USB_SDV_{DD} are to be filtered from the V_{DD} power supply. Two example solutions for USB_SV_{DD} and USB_SDV_{DD} filtering, where USB_SV_{DD} and USB_SDV_{DD} are sourced from a filtered version of V_{DD}, are illustrated in Figure 9, Figure 10, Figure 11 and Figure 12. Users can choose either one as they see best fit their needs, but the primary NFM type filter has two advantages: lower DC droop and easier layout than the ferrite bead solution.  **Figure 9. Primary USB_SV_{DD} power supply filter circuit**  **Figure 10. Alternate USB_SV_{DD} power supply filter circuit**  **Figure 11. Primary USB_SDV_{DD} power supply filter circuit**  **Figure 12. Alternate USB_SDV_{DD} power supply filter circuit** Note the following:	

Table 4. Power design system-level checklist

Item	Completed
• It is recommended that an area fill or power plane split be provided for a low-impedence profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Place each circuit as close as possible to the specific set of pins being supplied to minimize noise coupled from nearby circuits. • Located at each pin should have a decouple capacitor, such as 0.1 µF.	

4.3 Power-on and Reset recommendations

Various chip functions are initialized by sampling certain signals during the assertion of PORESET_B. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while PORESET_B is asserted. When PORESET_B de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Table 5. Reset system-level checklist

Item	Completed
Ensure PORESET_B is asserted for a minimum of 1 ms after V_{DD} ramps up.	
Ensure HRESET_B is asserted for a minimum of 32 SYSCLK cycles.	
In cases where a configuration pin has no default, use a 4.7 kΩ pull-up or pull-down resistor for appropriate configuration of the pin.	
Optional: An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when PORESET_B is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of PORESET_B (other than cfg_eng_use0), hold their values for at least two SYSCLK cycles after the de-assertion of PORESET_B, and then release the pins to high impedance afterward for normal device operation **NOTE:** See the applicable chip data sheet for details about reset initialization timing specifications.	
Configuration settings	
Ensure the settings in Configuration signals sampled at reset are selected properly. **NOTE:** See the applicable chip reference manual for a more detailed description of each configuration option.	
Power sequencing	
The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For details, see *QorIQ LS1046A, LS1026A Data Sheet*" (document LS1046A).	

4.3.1 Configuration signals sampled at reset

The signals that serve alternate functions as configuration input signals during system reset are summarized in this table.

Reset configuration signals are sampled at the negation of PORESET_B. However, there is a setup and hold time for these signals relative to the rising edge of PORESET_B, as described in the *QorlQ LS1046A Data Sheet* (document LS1046A).

The reset configuration signals are multiplexed with other functional signals. The values on these signals during reset are interpreted to be logic one or zero, regardless of whether the functional signal name is defined as active-low. The reset configuration signals have internal pull-up resistors so that if the signals are not driven, the default value is high (a one), as shown in the table below. Some signals must be driven high or low during the reset period. For details about all the signals that require external pull-up resistors, see the applicable device data sheet.

Table 6. LS1046A reset configuration signals

Configuration Type	Functional Pins	Comments
Reset configuration word (RCW) source inputs cfg_rcw_src[0:8]	IFC_AD[8:15] IFC_CLE	They must be set to one of the valid RCW source input option. The 512-bit RCW word has all the necessary configuration information for the chip. If there is no valid RCW in the external memory, it can be programmed using the Code Warrior or other programmer. The JTAG configuration files (path: CWInstallDir \CW4NET_v2019.01\CW_ARMv8\Config \boards) can be used in the following situations: • target boards that do not have RCW already programmed • new board bring up • recovering boards with blank or damaged flash
IFC external transceiver enable polarity select (cfg_ifc_te)	IFC_TE	Default is "1"
DRAM type select (cfg_dram_type)	IFC_A[21]	The reset configuration pin selects the proper IO voltage. • 1=Reserved • 0=DDR4 (1.2 V) Ensure the selected value matches DDR4
General-purpose input (cfg_gpinput[0:7])	IFC_AD[0:7]	Default "1111 1111", values can be application defined
"Single Oscillator Source" clock select. This field selects between SYSCLK (Single ended) and DIFF_SYSCLK/ DIFF_SYSCLK_B (differential) inputs. (cfg_eng_use0)	IFC_WE0_B	0=DIFF_SYSCLK/ DIFF_SYSCLK_B(differential) 1=SYSCLK (single ended) Default selection is single ended SYSCLK; "1"
"Single Oscillator Source" clock. This field indicates whether on-chip LVDS termination for differential clock is enabled or disabled. configuration (cfg_eng_use1)	IFC_OE_B	0 = Disabled (MUST make sure that External termination pads of DIFF_SYSCLK/DIFF_SYSCLK_B have proper termination) 1 = Enabled (default) Default is "1". It is recommened to keep provision for optional pull-down resistor on board.
"Single Oscillator Source" clock configuration (cfg_eng_use2)	IFC_WP0_B	Default is "1". Reserved.

4.3.2 Hard-coded RCW

The hard-coded RCW can be used as an alternative method for the initial board bring-up when there is no valid RCW in the external memory.

If a new board is using a blank flash and flash is the source of RCW, then all 0xff value from flash for RCW will put the device in an unknown state.

There are two methods to workaround this problem:

1. Put the switches on cfg_rcw_src signals to select hard-coded RCW (0x9F, 0x9E).
2. Use the CodeWarrior tool from NXP to override RCW.

NOTE

- It is recommended to disconnect RESET_REQ_B from PORESET_B when using hard-coded RCW as any different board configuration may push the chip to an endless reset loop. For more information, see the hard-coded RCW options listed in *QorIQ LS1046A Reference Manual* (document LS1046ARM).
- Use 0x9F for hard coded RCW when using DIFF_SYSCLK/DIFF_SYSCLK_B as the primary clock input to LS1046A.
- For bringing-up a new board when no valid RCW or bootloader is available and onboard flash is not supported in CodeWarrior then refer to AN12081.

5 Interface recommendations

This section details the pin termination guidelines for different interfaces. In general, any unused input pin should be terminated by a pull down unless recommended otherwise.

5.1 DDR controller recommendations

The memory interface controls main memory accesses. The LS1046A/LS1026A device supports 32-bit/64-bit (1.2 V) DDR4 SDRAM with ECC.

5.1.1 DDR SDRAM memory interface pin termination recommendations

Table 7. DDR SDRAM memory interface pin termination checklist

Signal name	IO type	Used	Not used	Completed
D1_MALERT_B	I	Recommend that a weak pull-up resistor (2-10 kΩ) for SDRAM DDR4 or strong pull-up resistor (50-100 Ω) for discrete/RDIMM SDRAM DDR4, be placed on this pin to the respective power supply.	Pull up whether used or not used.	

Table continues on the next page...

Table 7. DDR SDRAM memory interface pin termination checklist (continued)

Signal name	IO type	Used	Not used	Completed
D1_MPAR	O	MPAR from memory controller should be connected to the PAR signal at DRAM	May be left unconnected.	
D1_MACT_B	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MA[0:13]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MBA[0:1]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MBG[0:1]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MCAS_B[2]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MCKE[0:1]	O	Must be properly terminated to VTT. This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
D1_MCK[0:1]	O	Ensure these pins are terminated correctly.	May be left unconnected. Unused MCK pins can be disabled using DDRCLKDR register.	
D1_MCK_B[0:1]	O	Ensure these pins are terminated correctly.	May be left unconnected.	
D1_MCS[0:3]_B[2]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MDIC[0:1]	IO	• These pins are used for automatic calibration of the DDR4 IOs. • MDIC[0] is grounded through a 162 Ω precision 1% resistor and MDIC[1] is connected to G1VDD through a 162 Ω precision 1% resistor. • For either full or half drive strength calibration of DDR IOs, use the same MDIC resistor value of 162 Ω. • The memory controller register setting can be used to determine if automatic calibration is done to full or half drive strength.	May be left unconnected.	
D1_MDM[0:8]	O	—	May be left unconnected.	
D1_MDQS[0:8]_B	IO	—	May be left unconnected.	
D1_MDQS[0:8]	IO	—	May be left unconnected.	
D1_MDQ[0:63]	IO	—	May be left unconnected.	
D1_MECC[0:7]	IO	—	May be left unconnected.	

Table continues on the next page...

Table 7. DDR SDRAM memory interface pin termination checklist (continued)

Signal name	IO type	Used	Not used	Completed
D1_MODT[0:1]	O	Ensure the MODT signals are connected correctly. In general, for dual-ranked DIMMS, the following should all go to the same physical memory bank: • MODT(0), MCS(0), MCKE(0) • MODT(1), MCS(1), MCKE(1) For quad-ranked DIMMS, it is recommended to obtain a data sheet from the memory supplier to confirm required signals. But in general, each controller needs MCS(0:3), MODT(0:1), and MCKE(0:1) connected to the one quad-ranked DIMM.	May be left unconnected.	
D1_MRAS_B[2]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MWE_B[2]	O	Must be properly terminated to VTT.	May be left unconnected.	

NOTE

1. For DDR4 bit and byte swapping rules and layout guidelines, see the application note *Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces* (document AN5097).
2. When using RDIMM, the CS, RAS, CAS, WE signals may need series termination to prevent an excessive overshoot
3. When DDR4 Discrete or RDIMM DRAM is soldered on the board and two chip selects are used, and the second chip select is bit swizzling (meaning bits mapping from CS0 is additionally swapped in CS1 by swapping DQ0 with DQ1, DQ2 with DQ3, DQ4 with DQ5, and DQ6 with DQ7), then bit map orders of 0x10 (2 1 3 0) and 0x30 (6 5 7 4) are not allowed.

5.1.2 DDR system-level recommendations

Table 8. DDR system-level checklist

Item	Completed
General	
Data Bus inversion (DBI) signals are muxed on Data Mask (D1_MDM) signals and are optional function for DDR4. Only one function can be used at a time.	
HRESET can be used to reset unbuffered DIMM (UDIMM, SoDIMM) or discrete DRAM. For Registered DIMM, refer AN5097	
CKE termination requirment during self refresh -- In order to keep DRAM memory in a self-refresh mode, the CKE signal must be driven low. For applications requiring LS1046A to be powered off and SDRAM memory in self refresh, the CKE signal must be driven/pulled low during power ramp up, external to the SoC by hardware on the board. Refer AN4531	

NOTE

Stacked memory for DDR4 are not supported.

5.2 IFC recommendations

The integrated Flash controller shares signals with QSPI flash and Flex Timer Module. The functionality of these signals is determined by the IFC_GRP_[a]_BASE fields in the reset configuration word The LS1046A Integrated Flash Controller (IFC), supports upto 28-bit addressing and 8- or 16-bit data widths, for a variety of devices

5.2.1 IFC pin termination recommendations

Table 9. IFC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
IFC_A[16:20]	O	These pins must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If these pins are connected to a device that pulls down during reset, an external pull-up is required to drive these pins to a safe state during reset.		
IFC_A[21]	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_A[22:27]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_AD[0:15]	I/O	These pins are reset configuration pins. They have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. These pull-ups are designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_PAR[0:1]	I/O	Connect as needed.	These pins can be left unconnected.	
IFC_CS[0]_B	O	Recommend weak pull-up resistors (2–10 kΩ) be placed on these pins to OV_{DD}.	This pin can be left unconnected.	
IFC_CS[1:3]_B	O	Recommend weak pull-up resistors (2–10 kΩ) be placed on these pins to OV_{DD}.	These pins can be left unconnected.	
IFC_WE[0]_B	O	These pins are reset configuration pins, they have a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. The internal pull-ups are designed such that it can be overpowered by an external 4.7 kΩ resistor. However, It is recommended to keep a provision for optional pull-up and pull-down resistor on board.		
IFC_OE_B	O			
IFC_WP[0]_B	O			

Table continues on the next page...

Table 9. IFC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
IFC_PERR_B	I	Connect as needed.	This pin should be pulled high through a 2-10 kΩ resistor to OVDD or can be left floating if configured as output via the GPIO_GPDIR register.	
IFC_BCTL	O	Connect as needed.	This pin can be left unconnected.	
IFC_TE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_NDDQS	I/O	Connect as needed.	This pin can be left unconnected.	
IFC_AVD	O	This pin must not be pulled down during power-on reset. It may be pulled up, driven high, or if there are no externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		
IFC_CLE	O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_RB[0:1]_B	I	These pins should be pulled high through a 1 kΩ resistor to OV_{DD}.	These pins should be pulled high through a 1 kΩ resistor.	
IFC_CLK[0:1]	O	Connect as needed.	This pin can be left unconnected.	
IFC_NDDDR_CLK	O	Connect as needed	This pin can be left unconnected.	

NOTE

The IFC interface is on OVDD power domain which is 1.8 V only.

For functional connection diagram, see the chip reference manual.

5.3 DUART pin termination recommendations

Table 10. DUART pin termination checklist

Signal name	I/O type	Used	Not used	Completed
UART1_SOUT	O	The functionality of these pins is determined by the UART_BASE and UART_EXT fields in the reset	These pins can be left unconnected.	
UART1_RTS_B	O			

Table continues on the next page...

Table 10. DUART pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
UART1_SIN	I	configuration word (RCW[UART_BASE], RCW[UART_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART1_CTS_B	I			
UART2_SOUT	O		These pins can be left unconnected.	
UART2_RTS_B	O			
UART2_SIN	I		These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART2_CTS_B	I			
UART3_SOUT	O		This pin can be left unconnected.	
UART3_SIN	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	
UART4_SOUT	O		This pin can be left unconnected.	
UART4_SIN	I		This pin should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIO and output.	

5.4 LPUART pin termination recommendations

Table 11. LPUART pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
LPUART1_CTS_B	I	The functionality of LPUART1_CTS_B is determined by the UART_EXT field in the reset configuration word.	These pins should be pulled high through a 2-10 kΩ resistor to DVDD or else programmed as GPIO and output.	
LPUART[2:3]_CTS_B	I	The functionality of LPUART[2:3]_CTS_B is determined by the SDHC_EXT field in the reset configuration word.	These pins should be pulled high through a 2-10 kΩ resistor to EVDD or else programmed as GPIOs and outputs.	
LPUART1_RTS_B	O	The functionality of LPUART1_RTS_B is determined by the UART_EXT field in the reset configuration word RCW[UART_EXT].	Can be left floating or else program as GPIO and output.	
LPUART[2:3]_RTS_B	O	The functionality of LPUART[1:3]_RTS_B is determined by the SDHC_EXT field in the reset configuration word (RCW[SDHC_EXT]).	Can be left floating or else programmed as GPIOs and outputs.	
LPUART[1:2]_SIN, LPUART4_SIN	I	The functionality of LPUART[1:2]_SIN and LPUART[4]_SIN is determined by	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD} or else programmed as GPIOs and outputs.	

Table continues on the next page...

Table 11. LPUART pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
		the UART_EXT field in the reset configuration word (RCW[UART_EXT]).		
LPUART[3]_SIN, LPUART[5:6]_SIN	I	The functionality of LPUART[5:6]_SIN and LPUART[3]_SIN is determined by the SDHC_EXT field in the reset configuration word (RCW[SDHC_EXT]).	These pins should be pulled high through a 2-10 kΩ resistor to EV_{DD} or else programmed as GPIOs and outputs.	
LPUART[1:2]_SOUT, LPUART[4]_SOUT	O	The functionality of LPUART[1:2]_SOUT and LPUART[4]_SOUT is determined by the UART_EXT field in the reset configuration word (RCW[UART_EXT]).	Can be left floating or else programmed as GPIOs and outputs.	
LPUART3_SOUT, LPUART[5:6]_SOUT	O	The functionality of LPUART[5:6]_SOUT and LPUART[3]_SOUT is determined by the SDHC_EXT field in the reset configuration word (RCW[SDHC_EXT]).	Can be left floating or else programmed as GPIOs and outputs.	

5.5 I2C pin termination recommendations

Table 12. I2C pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
IIC1_SDA	I/O	Tie these open-drain signals high through a nominal 1 kΩ resistor to DV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	These pins should be pulled high through a 2-10 kΩ resistor to DV_{DD}.	
IIC1_SCL	I/O			
IIC2_SDA	I/O	The functionality of this signal is determined by the IIC2_EXT field in the reset configuration word (RCW[IIC2_EXT]). Recommend that a weak pull-up resistor (1 kΩ)be placed on this pin to the respective power supply.This pin is an open-drain signal.	When programmed as IIC2, pull high through a 2-10 kΩ resistor. Alternately, these pins can be programmed as GPIO and output	
IIC2_SCL	I/O			
IIC3_SDA	I/O	The functionality is determined by the SCFG_RCWPMUXCR0 register. Recommend that a weak pull-up resistor (1 kΩ)be placed on the pin to the respective power supply.These pins are open-drain.	When programmed as IIC, pull high through a 2-10 kΩ resistor. Alternately, these pins can be programmed as GPIO and output.	
IIC3_SCL	I/O			
IIC4_SDA	I/O			
IIC4_SCL	I/O			

5.6 eSDHC recommendations

The LS1046A/LS1026A eSDHC interface supports a large variety of devices, as the following list shows:

- SDXC cards upto 2 TB space with UHS-I speed grade are supported
- UHS-I (Ultra high speed grade) SDR12, SDR25, SDR50, SDR104, and DDR50 are supported
- UHS-I cards work on 1.8 V power signaling
- On board dual voltage regulators are needed to support UHS-I cards because card initialization happens at 3.3 V and regular operations happen at 1.8 V. The SD controller provides a signal to control the voltage regulator, controlled via SDHC_VS bit
- eMMC 4.5 is supported (HS200, DDR)

Table 13. Supported SD card Modes

Mode	1-bit support		4-bit support		8-bit support
	LS1046A/ LS1026A	SD (3.0)	LS1046A/ LS1026A	SD (3.0)	
DS (Default Speed)	Yes	Yes	Yes	Yes	Neither supported by the SD standards nor by the LS1046A/ LS1026A device.
HS (High Speed)	Yes	Yes	Yes	Yes	
SDR12	No	No	Yes	Yes	
SDR25	No	No	Yes	Yes	
SDR50	No	No	Yes	Yes	
SDR104	No	No	Yes	Yes	
DDR50	No	No	Yes	Yes	

Table 14. Supported MMC/eMMC Modes

Mode	1-bit support		4-bit support		8-bit support	
	LS1046A/ LS1026A	eMMC (4.5)	LS1046A/ LS1026A	eMMC (4.5)	LS1046A/ LS1026A	eMMC (4.5)
DS (Default Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS(High Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS200	No	No	Yes	Yes	Yes	Yes
DDR	No	No	Yes	Yes	No	Yes

5.6.1 eSDHC pin termination recommendations

Table 15. eSDHC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SDHC_CMD	I/O	This pin should be pulled high through a 10-100 kΩ resistor to EV_{DD}.	Program as GPIO and output.	

Table continues on the next page...

Table 15. eSDHC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
		The functionality is determined by the RCW[SDHC_EXT] and SDHC_BASE field in the reset configuration word (RCW[SDHC_EXT], RCW[SDHC_BASE]).		
SDHC_CLK	O	The functionality is determined by the SDHC_EXT and SDHC_BASE field in the reset configuration word (RCW[SDHC_EXT], RCW[SDHC_BASE]).		
SDHC_DATA[0]	I/O	These pins should be pulled high through a 10-100 kΩ resistor to EV_{DD}. The functionality is determined by the SDHC_EXT and SDHC_BASE field in the reset configuration word (RCW[SDHC_EXT], RCW[SDHC_BASE]).	Program as GPIOs and output.	
SDHC_DATA[1:3]	I/O		Unused pins should be pulled high through a 10-100 kΩ resistor to EV_{DD}. Alternately they can be configured as GPIO outputs through RCW[SDHC_BASE].	
SDHC_DATA[4:7]	I/O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality is determined by the SPI_EXT and SPI_BASE field in the reset configuration word (RCW[SPI_EXT], RCW[SPI_BASE]).	Program as GPIOs and output.	
SDHC_CD_B	I	These pins should be pulled high through 10-100 kΩ resistors to DV_{DD}. The functionality is determined by the SDHC field in the reset configuration word (RCW[IIC2_EXT]).	This pin should be pulled high through a 10-100 kΩ resistor to DV_{DD} or program as GPIOs and output.	
SDHC_WP	I		This pin should be pulled low through a 10-100 kΩ resistor to GND or program as GPIOs and output.	
SDHC_CMD_DIR	O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality is determined by the SPI_EXT field in the reset configuration word (RCW[SPI_EXT]). **NOTE:** DIR signals are used as direction controls of external voltage translator	These pins can be programmed for other functions or GPIOs and output.	
SDHC_DAT0_DIR	O			
SDHC_DAT123_DIR	O			
SDHC_VS	O	These pins should be pulled high through 10-100 kΩ resistors to OV_{DD}. The functionality is determined by the SPI_BASE field and SPI_EXT field in the reset configuration word (RCW[SPI_BASE] and RCW[SPI_EXT]). **NOTE:** External voltage select, to change voltage of external regulator.	Can be left floating or programmed for other function.	

Table continues on the next page...

Table 15. eSDHC pin termination checklist (continued)

Signal name	I/O type	Used	Not used	Completed
SDHC_CLK_SYNC_IN	I	The functionality is determined by the SPI_EXT field in the reset configuration word (RCW[SPI_EXT]).	If signal is not used, pin can be programmed as output for other functions or pulled down using a weak resistor.	
SDHC_CLK_SYNC_OUT	O	The functionality is determined by the SPI_EXT field in thereset configuration word (RCW[SPI_EXT]).	Can be left floating or programmed for other function.	

NOTE

1. Separate DIR signals are implemented to support card interrupt on DAT1 in single bit mode.
2. SDHC_CLK_SYNC_OUT to SDHC_CLK_SYNC_IN connection is required in SDR50 and DDR50 mode only.
3. In SDR50 and DDR50 mode, all the input signals are sampled with respect to SDHC_CLK_SYNC_IN.
4. SDHC_CLK_SYNC_OUT and SDHC_CLK_SYNC_IN should be routed as close as possible to the card, with minimum skew with respect to SD_CLK.
5. When using 8-bit MMC/eMMC configuration, EV_{DD} and OV_{DD} should be set at same voltage.
6. As per the SD specification, a power cycle is required to reset the SD card working on UHS-I speed mode. Board design needs to provide some mechanism to power cycle the SD card during every reset.

5.6.2 eSDHC system-level recommendations

Table 16. eSDHC system-level checklist

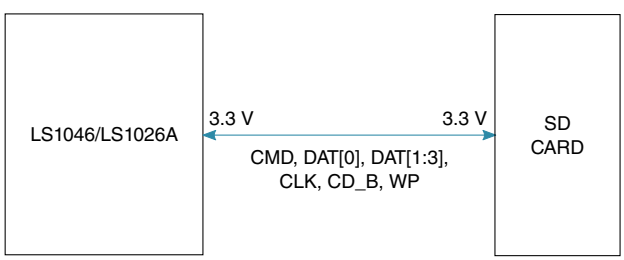
Item	Completed
SD Card interfacing (8-bit is not supported)	
SD Card Connections (DS and HS mode) EVDD configured for 3.3 V  **Figure 13. DS and HS modes**	
SD Card Connections (SDR12, 25, 50, 104, and DDR50 modes) UHS-I modes, work on 1.8 V signalling. The SYNC_OUT, SYNC_IN connections are required in SDR50 and DDR50 modes only.	

Table continues on the next page...

Table 16. eSDHC system-level checklist (continued)

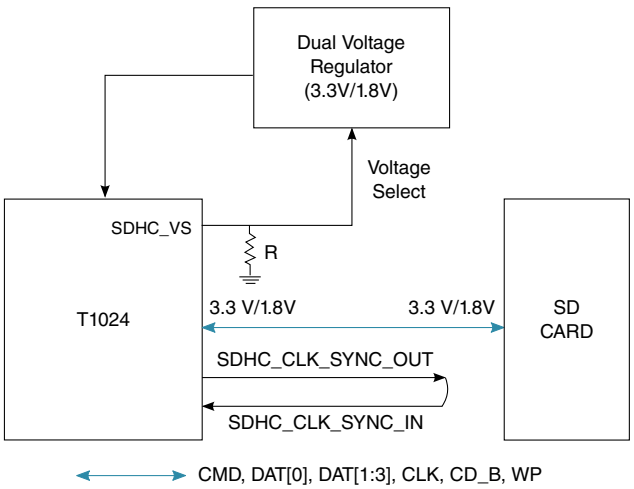
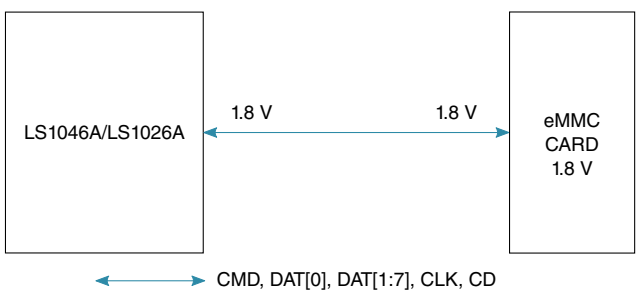
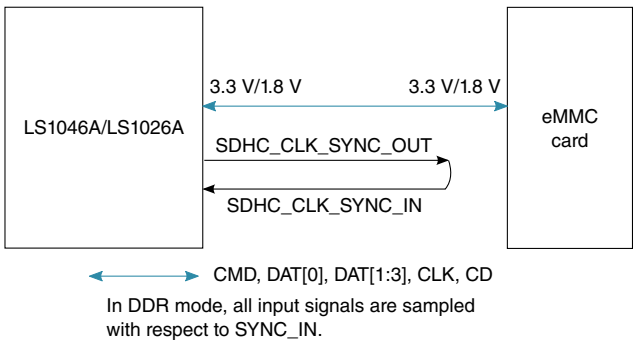
Item	Completed
NOTE: Resistor R=10 K is needed when RCW loading is required to be done from SD card.  **Figure 14. SDR12, 25, 50, 104, and DDR50 modes**	
eMMC Interfacing	
eMMC Card Connections (DS, HS, HS200 Modes) at 1.8 V card The 8-bit eMMC interface requires EVDD and OVDD configured at 1.8V  **Figure 15. DS, HS, and HS200 modes for eMMC (1.8 V)** **NOTE:** • HS200 mode is 1.8 V only mode as per eMMC 4.5 specification	
eMMC Card Connection in DDR mode The 8-bit operation cannot be supported due to RCW selection constraints. The DDR mode supports both 3.3 V and 1.8 V operation as per eMMC 4.4 specification.	

Table 16. eSDHC system-level checklist

Item	Completed
 **Figure 16. DDR mode**	

5.7 Global interrupt controller (GIC) recommendations

Note that the GIC pins in LS1046/LS1026A are distributed over several voltage domains.

5.7.1 GIC pin termination recommendations

Table 17. GIC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
IRQ[0:2]	I	Ensure these pins are driven in the non-asserted state.	These pins should be tied to nonasserted state through a 2-10 kΩ resistor. • When non-asserted state is high, tied to OV_{DD} • When non-asserted state is low, tied to GND	
IRQ[3:10]	I	Ensure these pins are driven in the non-asserted state. The functionality is determined by the IRQ_BASE and IRQ_EXT field in the reset configuration word (RCW[IRQ_BASE] and RCW[IRQ_EXT]).	These pins should be tied to nonasserted state through a 2-10 kΩ resistor. • When non-asserted state is high, tied to DV_{DD} • When non-asserted state is low, tied to GND or else programmed as GPIOs and ouputs.	
IRQ[11]	I		This pin should be tied to nonasserted state through a 2-10 kΩ resistor.	

Table 17. GIC pin termination checklist

Signal name	I/O type	Used	Not used	Completed
			• When non-asserted state is high, tied to LV_{DD} • When non-asserted state is low, tied to GND or else programmed as GPIOs and ouputs.	

NOTE

1. Interrupt polarity can be programmed through Interrupt Polarity Register (SCFG_INTPCR) register. Default polarity for the IRQ's is active high.

5.8 Trust pin termination recommendations

Table 18. Trust pin termination checklist

Signal name	IO type	Used	Not used	Completed
TA_BB_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (1.0 V) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	This pin should be pulled high through a 2-10 kΩ resistor to VDD (1.0 V).	
TA_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage (OVDD) until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	This pin should be pulled high through a 2-10 kΩ resistor to OVDD.	

5.9 Power management pin termination recommendations

Table 19. Power Management pin termination checklist

Signal name	IO type	Used	Not used	Completed
ASLEEP	O	The functionality of this signal is determined by the ASLEEP field in the reset configuration word (RCW[ASLEEP]).	Can be left floating as it is an output, alternately it may be programmed as GPO.	

5.10 Debug and reserved pin recommendations

5.10.1 Debug and reserved pin termination recommendations

Table 20. Debug and test pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SCAN_MODE_B	I	This is a test signal for factory use only and must be pulled up (100 Ω - 1 kΩ) to OV_{DD} for normal device operation.		
TEST_SEL_B	I	This pin must be pulled to OV_{DD} through a 100 Ω to 1 kΩ resistor for a four core LS1046A device and tied to the ground for a two core LS1026A device.		
EVT_B[0:4]	I/O	Debug event pins	By default EVT_B[0:4] signals are input. EVT_B0 has a weak internal pull up and can be left floating, EVT_B[1:4] need to be pulled up through a 2-10 kΩ resistor to OV_{DD}. Alternately EVT_B[0:4] can be programmed as outputs through EPU_EPEVTCR register early in boot code and left floating.	
EVT_B[5:8]	I/O	The functionality of these signals is determined by the IIC3 and IIC4 field in the SCFG_RCWPMUXCR0 register	EVT[5:8] can be programmed as GPIO outputs through SCFG_RCWPMUXCR0 bits and left floating.	
EVT_B[9]	I/O	Connect as required.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD} Alternately, EVT_B[9] can be programmed as output through EPU_EPEVTCR register early in boot code and left unconnected.	
JTAG_BSR_VSEL[1]	I	It is advised that boards are built with the ability to pull up and pull down this pin. • For normal debug operation, this pin must be pulled low to GND through 4.7 kΩ resistor. • For boundary scan operation, this pin must be pulled high to OV_{DD} through 4.7 kΩ resistor.		
TBSCAN_EN_B[2]	I	It is advised that boards are built with the ability to pull up and pull down this pin. • For normal debug operation, this pin must be pulled high to OV_{DD} through 4.7 kΩ resistor. • For boundary scan operation, this pin must be pulled low to GND through 4.7 kΩ resistor.		
FA_VL	-	Reserved. This pin must be pulled to ground (GND).		
PROG_MTR	-	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_G_V	-	Reserved. This pin must be pulled to ground (GND).		
FA_ANALOG_PIN	-	Reserved. This pin must be pulled to ground (GND).		
TH_TPA	-	Do not connect. This pin should be left floating.		
TD1_ANODE	-	Connect as required.	Tie to GND if not used.	
TD1_CATHODE	-	Connect as required.	Tie to GND if not used.	
D1_TPA	IO	Do not connect. These pins should be left floating.		

NOTE

1. JTAG_BSR_VSEL is an IEEE 1149.1 JTAG Compliance Enable pin.
   - 0: normal operation.
   - 1: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.
2. TBSCAN_EN_B is an IEEE 1149.1 JTAG Compliance Enable pin.
   - 0:To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.
   - 1: JTAG connects to DAP controller for the ARM core debug.

5.11 SerDes pin termination recommendations

Table 21. SerDes pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
SD1_IMP_CAL_RX	I	Tie to SV_{DD} through a 200 Ω 1% resistor.	If the SerDes interface is entirely unused, this pin must be left unconnected.	
SD1_IMP_CAL_TX	I	Tie to XV_{DD} through a 698 Ω 1% resistor.		
SD1_PLL1_TPA	O	Provide a test point if possible. These pins should be left floating		
SD1_PLL1_TPD	O			
SD1_PLL2_TPA	O			
SD1_PLL2_TPD	O			
SD1_REF_CLK1_P SD1_REF_CLK1_N	I	Ensure clocks are driven from an appropriate clock source, as per the protocol selected by the RCW settings.	If the PLL is unused, pull down to GND.	
SD1_REF_CLK2_N SD1_REF_CLK2_P	I			
SD1_RX[0:3]_N	I	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be pulled down to GND.	
SD1_RX[0:3]_P	I			
SD1_TX[0:3]_N	O	Ensure pins are correctly terminated for the interface type used.	If SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD1_TX[0:3]_P	O			
SD2_IMP_CAL_RX	I	Tie to SV_{DD} through a 200 Ω 1% resistor.	If the SerDes interface is entirely unused, the pin must be left unconnected.	
SD2_IMP_CAL_TX	I	Tie to XV_{DD} through a 698 Ω 1% resistor.	If the SerDes interface is entirely unused, the pin must be left unconnected.	
SD2_PLL1_TPA	O	Provide a test point if possible. These pins should be left floating		
SD2_PLL1_TPD	O			
SD2_PLL2_TPA	O			
SD2_PLL2_TPD	O			
SD2_REF_CLK1_N SD1_REF_CLK1_P	I	Ensure clocks are driven from an appropriate clock source, as per the protocol selected by the RCW settings.	If the PLL is unused, pull down to GND.	
SD2_REF_CLK2_N	I			

Table continues on the next page...

Table 21. SerDes pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
SD2_REF_CLK2_P				
SD2_RX[0:3]_N	I	Ensure pins are correctly terminated for the interface type used.	If the SerDes interface is entirely or partly unused, the unused pins must be pulled down to GND.	
SD2_RX[0:3]_P	I			
SD2_TX[0:3]_N	O	Ensure pins are correctly terminated for the interface type used.	If SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD2_TX[0:3]_P	O			

NOTE

1. In the RCW configuration field SRDS_PLL_PD_S1 and SRDS_PLL_PD_S2, the respective bits for each unused PLL must be set to power it down. The SerDes module is disabled when both of its PLLs are turned off.
2. After Power on Reset, if an entire SerDes module is unused, it must be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDSxPLLaRSTCTL).
3. Unused lanes must be powered down by clearing the RRST_B and TRST_B fields and setting the RX_PD and TX_PD fields in the corresponding lane's general control register (SRDSxLNmGCR0).
4. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interface, such as SGMII or SATA, is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.
5. PCIe Gen 3 cannot be used if SATA is also being used on the same SerDes.
6. PCIe Gen 3 speed support requires switching to second PLL so when Gen 3 is used both SerDes PLL will be used by PCIe protocol.
7. When LS1046A is used as an EP on motherboards, it is recommended to use the PCIe express clock from the PCIe slot as SerDes reference clock for LS1046A. This ensures that +/- 300ppm reference clock tolerance is met at both ends. This clocking architecture also supports spread spectrum clocking as per PCIe base specification.
8. As per PCIe base specification 3.0, both ends of link should enter LTSSM Detect state within 20 ms of the end of Fundamental Reset.
9. If SerDes lanes are routed to a backplane slot or a PCIe connector, SerDes pins can be left unterminated even if the link partner card is not present. If some SerDes lanes are a no-connect, pull down their receiver pins to GND. Then, if the SerDes block is powered, refer to the RM’s Unused Lanes section for directions on how to power them down. To power down a SerDes lane, configure the General Control 0 register during the PBI phase. If the whole SerDes block is already powered down, there is no need to individually power down a lane.

5.11.1 Optimal setting for the SerDes channel Rx Equalization Boost bit

Select the optimal setting for the SerDes channel Rx Equalization Boost bit suitable for a particular end product system board.

For certain high speed SerDes protocols, the Rx Equalization Boost bits for all the SerDes lanes in use are initialized with a default value of 1b by the RCW. In reality, although the default 1b setting does overlap with the 0b setting in terms of Rx Equalization boost effect, the 0b setting works better for short and normal SerDes channels, while the 1b setting works better for high loss channels.

For end product system with non-high loss SerDes channels (lanes), using the default 1b setting of the Rx Equalization Boost bit may adversely enhance the return loss due to some discontinuities possibly presented in the channel. This may further causes more reflection. Therefore, unless the channel is high loss, to ensure the channel's health and better performance, the 0b setting of Rx Equalization Boost bit should be used for all the lanes, instead of the default 1b setting.

The following high speed SerDes protocols are related to this issue. If a protocol supports more than one speed, only the speed(s) listed below is affected.

- PCI Express Gen3 (8.0 GT/s)
- SATA 6 Gbaud
- 10GBase-KR
- XFI 10.3125 Gbaud

Since the channel characteristics is board and layout dependent, NXP cannot quantify the actual channel loss introduced during board design, layout and fabrication of all end product systems for our customers. Customers should always perform board level simulation and also use other appropriate tool (for example, NXP's SerDes Validation Tool) and/or instrument to determine whether the SerDes channels (lanes) are in high loss condition and then adopt the best setting suitable for their end product and application. Instead of quantifying a SerDes channel as high or non-high loss, a more practical way is to try both the 1b and 0b settings and find out which setting yields better signal integrity for the customer's particular end product system or board.

Once determined that the channels are in non-high loss condition, the Rx Equalization Boost bit for all the lanes in use should be set to 0b during the Pre-boot Initialization (PBI) stage.

Since the Rx Equalization Boost bit is defined in different SerDes registers depending on the SerDes protocols in use, it is important to select the appropriate SerDes register with the correct offset and value as described below when implementing the register write in PBI. The SerDes registers involved are defined on a per lane basis. Therefore, PBI register write must be implemented for all the lanes utilized for the affected SerDes protocols and speeds.

- For PCI Express Gen3 (8.0 GT/s):

  Perform a PBI write to each lane's LNaSSCR1 register with a value of 0x9849_db00, which sets this lane's Rx Equalization Boost bit, LNaSSCR1 [RXEQ_BST_1] to 0b.

  Note that the RATIO_PST1Q_1 and AMP_RED_1 bit fields of the LNaSSCR1 register are read-only and directly driven by the PCI Express controller core hardware based on the Gen3 link training equalization negotiation result. Therefore, it is normal to observe values of the above bit fields different from lane to lane.

- For SATA 6 Gbaud:

  Perform a PBI write to each lane's LNaSSCR1 register with a value of 0x0050_2880, which sets this lane's Rx Equalization Boost bit, LNaSSCR1 [RXEQ_BST_1] to 0b.

- For 10GBase-KR:

  Perform a PBI write to each lane's LNaRECR0 register with a value of 0x0000_045F, which sets this lane's Rx Equalization Boost bit, LNaRECR0 [RXEQ_BST] to 0b.

- For XFI 10.3125 Gbaud:

  Perform a PBI write to each lane's LNaRECR0 register with a value of 0x0000_045F, which sets this lane's Rx Equalization Boost bit, LNaRECR0 [RXEQ_BST] to 0b.

5.12 USB PHY pin termination recommendations

Table 22. USB 1/2/3 PHY pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
USB[1/2/3]_D_P	IO	USB PHY Data Plus	Do not connect. These pins should be left floating.	
USB[1/2/3]_D_M	IO	USB PHY Data Minus	Do not connect.These pins should be left floating.	
USB[1/2/3]_VBUS	I	USB1 power supply pin. A charge pump external to the USB 3.0 PHY must provide power to this pin. The nominal voltage for this pin is 5 V.	Do not connect.These pins should be left floating.	
USB[1/2/3]_ID	I	USB PHY ID Detect	Pull low through a 1kΩ resistor to GND.	
USB[1/2/3]_TX_P	O	USB PHY 3.0 Transmit Data (positive)	Do not connect.These pins should be left floating.	
USB[1/2/3]_TX_M	O	USB PHY 3.0 Transmit Data (negative)	Do not connect.These pins should be left floating.	
USB[1/2/3]_RX_P	I	USB PHY 3.0 Receive Data (positive)	Connect to ground (GND)	
USB[1/2/3]_RX_M	I	USB PHY 3.0 Receive Data (negative)	Connect to ground (GND)	
USB[1/2/3]_RESREF	IO	Attach a 200-Ω 1% 100-ppm/ ^{0}C precision resistor-to-ground on the board.	Do not connect.These pins should be left floating.	
USB_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB_DRVVBUS signal is determined by the RCW[USB_DRVVBUS] field in the reset configuration word. The register SCFG_USBDRVVBUS_SELCR selects which of the three controllers drives USB_DRVVBUS.	Do not connect.These pins can be left floating.	
USB_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by the RCW[PWRFAULT] field in the reset configuration word. USB_PWRFAULT can be shared by all the three controllers, selection through SCFG_USBPWRFAULT_SELCR register bits.	Pull low through a 1kΩ resistor to GND. Alternately can be configured as a GPIO output through RCW[USB_PWRFAULT].	
USB2_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB2_DRVVBUS signal is determined by Extended RCW PinMux Control Register (SCFG_RCWPMUXCR0) in bitfield IIC3_SCL.	Do not connect.These pins can be left floating.	

Table continues on the next page...

Table 22. USB 1/2/3 PHY pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
USB2_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by Extended RCW PinMux Control Register (SCFG_RCWPMUXCR0) in bitfield IIC3_SDA. The register SCFG_USBPWRFAULT_SELCR[USB2_SEL] can be used to select dedicated USB2_PWRFAULT signal for controller 2 or select shared USB_PWRFAULT signal.	Pull low through a 1kΩ resistor to GND.	
USB3_DRVVBUS	O	VBUS power enable. For example, if an external hub is used, it can handle this signal. The functionality of the USB_DRVVBUS signal is determined by Extended RCW PinMux Control Register**(SCFG_RCWPMUXCR0)** in bitfield IIC4_SCL.	Do not connect.These pins can be left floating.	
USB3_PWRFAULT	I	Indicates that a VBUS fault has occurred. For example, if an external hub is used, it can handle this signal. The functionality of the USB_PWRFAULT signal is determined by Extended RCW PinMux Control Register (SCFG_RCWPMUXCR0) in bitfield IIC4_SDA. The register SCFG_USBPWRFAULT_SELCR[USB3_SEL] can be used to select dedicated USB3_PWRFAULT signal for controller 3 or select shared USB_PWRFAULT signal.	Pull low through a 1kΩ resistor to GND.	

NOTE

USB 3.0 PLLs can receive clock either from SYSCLK or DIFF_SYSCLK/ DIFF_SYSCLK_B. Ensure that the selected clock has 100 MHz frequency.

USB[1/2/3]_VBUS: The permissible voltage range is 0 - 5.25V.

USB[1/2/3]_ID: The permissible voltage range for input signal is 0 - 1.8V.

5.12.1 USB1 PHY connections

This section describes the hardware connections required for the USB PHY.

This figure shows the VBUS interface for the chip.

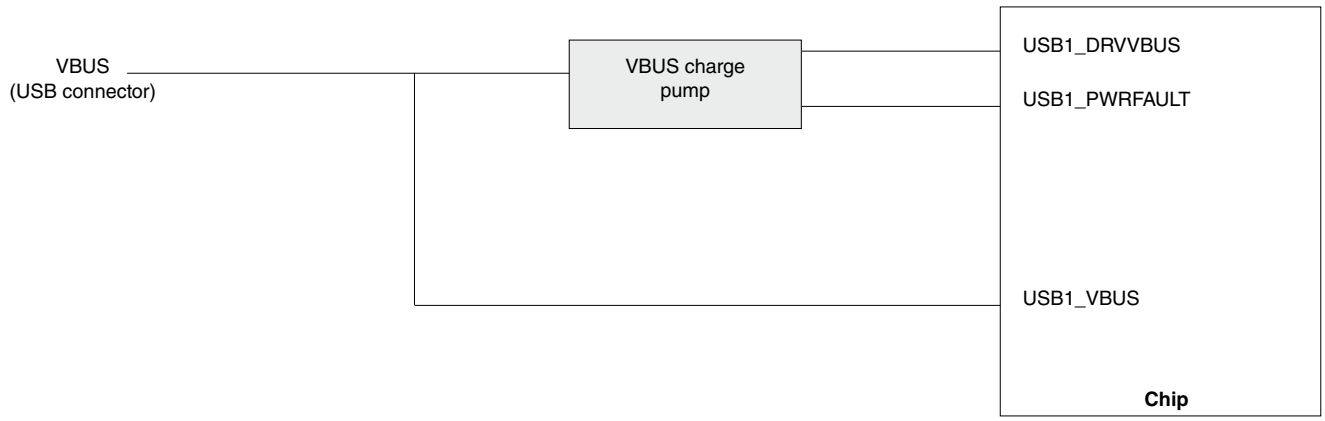


Figure 17. USB1 PHY VBUS interface

5.13 Ethernet Management Interface 1/2 pin termination recommendations

Table 23. Ethernet Management Interface (EMI1/2) pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EMI1_MDC	O	The functionality of these signals is determined by the EM1 field in the reset configuration word (RCW[EM1]). To configure as open drain signal, write EMI1_CMODE in reset configuration word. If configured as open-drain, pull this pin to LVDD with a suitable resistor. The value of pull-up resistor depends on input impedance of all the peripherals connected on EMI1 bus. More the peripherals or more the impedance stronger the pull-up. Typically 200ohm pull-up should suffice for 3-4 peripherals. Unless there is a requirement of EMI1_MDC being an open-drain, it is advised to configure EMI1_MDC in "normal functional" mode. In "normal functional" mode, the EMI1_MDC will be actively driven and pull up resistors are not required.	These pins should be tied low through a 2-10 kΩ resistor to ground (GND), or may be configured as a GPIOs and outputs.	

Table continues on the next page...

Table 23. Ethernet Management Interface (EMI1/2) pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
EMI1_MDIO	IO	The functionality of these signals is determined by the EM1 field in the reset configuration word (RCW[EM1]). To configure as open drain signal, write EMI1_DMODE in reset configuration word. If configured as open-drain, pull this pin to LVDD with a suitable resistor. The value of pull-up resistor depends on input impedance of all the peripherals connected on EMI1 bus. More the peripherals or more the impedance stronger the pull-up. Typically 330ohm pull-up should suffice for 3-4 peripherals. Unless there is a requirement of EMI1_MDIO being an open-drain, it is advised to configure EMI1_MDIO in "normal functional" mode. In "normal functional" mode, the EMI1_MDIO will be actively driven. A pull up resistors might still be required as the peripherals on EMI bus might have their EMI1_MDIO pins configured as open-drain. The value of pull-up resistor depends on total input impedance of all the peripherals connected.		
EMI2_MDC	O	The functionality of these signals is determined by the EM2 field in the reset configuration word (RCW[EM2]). To configure as open drain signal, write EMI2_CMODE in reset configuration word. If configured as open-drain, pull this pin to TVDD with a suitable resistor. The value of pull-up resistor depends on input impedance of all the peripherals connected on EMI2 bus. More the peripherals or more the impedance stronger the pull-up. Typically 200ohm pull-up should suffice for 3-4 peripherals. Unless there is a requirement of EMI2_MDC being an open-drain, it is advised to configure EMI2_MDC in "normal functional" mode. In "normal functional" mode, the	These pins should be tied low through a 2-10 kΩ resistor to ground (GND), or may be configured as a GPIOs and outputs.	

Table continues on the next page...

Table 23. Ethernet Management Interface (EMI1/2) pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
		EMI2_MDC will be actively driven and pull up resistors are not required.		
EMI2_MDIO	IO	The functionality of these signals is determined by the EM2 field in the reset configuration word (RCW[EM2]). To configure as open drain signal, write EMI2_DMODE in reset configuration word. If configured as open-drain, pull this pin to TVDD with a suitable resistor. The value of pull-up resistor depends on input impedance of all the peripherals connected on EMI2 bus. More the peripherals or more the impedance stronger the pull-up. Typically 330ohm pull-up should suffice for 3-4 peripherals. Unless there is a requirement of EMI2_MDIO being an open-drain, it is advised to configure EMI2_MDIO in "normal functional" mode. In "normal functional" mode, the EMI2_MDIO will be actively driven. A pull up resistors might still be required as the peripherals on EMI bus might have their EMI2_MDIO pins configured as open-drain. The value of pull-up resistor depends on total input impedance of all the peripherals connected.		

NOTE

- Refer Ethernet A-010717: EMI - MDIO to MDC input hold time (tMDDXKH) specification violation from LS1046A Chip errata.
- For MDC frequency greater than 2.5 MHz and less than (or equal to) 10 MHz, the load on the MDC/MDIO pads must not exceed 75pf

5.14 Ethernet controller pin termination recommendations

The LS1046A/LS1026A supports two Ethernet Controllers (EC) which can connect to Ethernet PHYs using RGMII protocols. Both, EC1 and EC2 operated using LVDD supply which supports 1.8 V/2.5 V operation.

Table 24. Ethernet controller pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
EC1 in RGMII mode				

Table continues on the next page...

Table 24. Ethernet controller pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
EC1_TXD[0:3], EC1_TX_EN[1]	O	The functionality of these signals is determined by the EC1 field in the reset configuration word (RCW[EC1]). FMAN-MAC3 is connected to EC1 interface when RGMII is selected through RCW[EC1] field	Entire EC1 interface can be configured as GPIOs and outputs through RCW[EC1].	
EC1_GTX_CLK	O			
EC1_RXD[0:3]	I			
EC1_RX_DV	I			
EC1_RX_CLK	I			
EC1_GTX_CLK125[2]	I			
EC2 in RGMII mode				
EC2_TXD[0:3], EC2_TX_EN[1]	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]). FMAN-MAC4 is connected to EC2 interface when RGMII is selected through RCW[EC2] field	Entire EC2 interface can be configured as GPIOs and outputs through RCW[EC2].	
EC2_GTX_CLK	O			
EC2_RXD[0:3]	I			
EC2_RX_DV	I			
EC2_RX_CLK	I			
EC2_GTX_CLK125[2]	I			

NOTE

1. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
2. Either of the EC1_GTX_CLK125 or EC2_GTX_CLK125 can be used to clock both the EC interfaces in RGMII mode. The selection is through SCFG_ECGTXCMCR[CLKSEL]. The unused clock pin should be pulled to GND.

5.15 QSPI controller recommendations

LS1046A supports one Quad Serial Peripheral Interface (QSPI) controller. It supports 1 bit, 2 bit and 4 bit modes.

5.15.1 QSPI pin termination recommendations

Table 25. QSPI pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
QSPI_A_SCK	O	The functionality of these signals is determined by the RCW[IFC_GRP_F_EXT] bits of reset configuration word.	Pin can be left unconnected.	
QSPI_B_SCK	O			
QSPI_A_CS[0:1]	O			
QSPI_B_CS[0:1]	O			
QSPI_A_DATA[0:2]	IO		If these pins are not used, they should be pulled to GND through 1 kΩ resistance.	

Table continues on the next page...

Table 25. QSPI pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
QSPI_A_DATA[3]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_A_EXT] bits of reset configuration word.	If this pin is not used, it should be programmed as GPIO and output.	
QSPI_B_DATA[0:2]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_D_EXT] bits of reset configuration word.	If this pin is not used, it should be programmed as GPIO and output.	
QSPI_B_DATA[3]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_E1_EXT] bits of reset configuration word.	If this pin is not used, it should be programmed as GPIO and output.	

NOTE

1. QSPI signals are multiplexed with IFC signals and only select lines are available on IFC when QSPI is used.
2. Refer erratum GEN A-010539, which states that SDHC_CLK_SYNC_OUT, SDHC_CLK_SYNC_IN, SDHC_VS, SDHC_DAT[4:7], SDHC_DAT0_DIR, SDHC_DAT123_DIR, SDHC_CMD_DIR, GPIO2_[0:3] are not available when booting from QSPI. Once the workaround is applied HRESET_B can no longer be used. The following are the modes which can be used without applying the workaround:
   - SDHC interface is not used at all.
   - SDHC full speed and high speed modes (ensure that SDHC_CLK_SYNC_IN and SDHC_CLK_SYNC_OUT are not used).
   - eMMC full speed and high speed in 4 bit mode at 1.8V or 3.3V.
   - eMMC HS200 in 4 bit mode and 1.8V.
3. If RCW[IFC_GRP_A_EXT]=001, IFC_A26 and IFC_A27 should be pulled to GND through 4.7 kΩ resistor. Otherwise these pins should be configured as output GPIOs and left as unconnected.

5.16 SPI recommendations

The LS1046A/LS1026A serial peripheral interface (SPI) supports master mode and is powered from OVDD (1.8V) supply.

5.16.1 SPI pin termination recommendations

Table 26. SPI pin termination checklist

Signal name	I/O type	Used	Not used	Completed
SPI_SIN	I	The functionality of these signals is determined by the RCW[SPI_BASE] and RCW[SPI_EXT] fields.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD}.	
SPI_SOUT	I/O			
SPI_SCK	O		This pin may be left unconnected.	
SPI_PCS[0:3]	O			

NOTE

- SPI_CLK is available when RCW[SPI_EXT]=000 and RCW[SPI_BASE]=00. Master mode requires that SPI_CLK is generated by Master, therefore only RCW[SPI_EXT]=000 and RCW[SPI_BASE]=00 can be used for SPI controller on this device although some SPI signals are also available when RCW[SPI_EXT]=001

5.17 General Purpose Input/Output pin termination recommendations

Table 27. General Purpose Input/Output pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
GPIO1_13	O	The functionality of this signal is determined by the RCW[ASLEEP] field in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO1_14	IO	The functionality of this signal is determined by the RCW[RTC] field in the reset configuration word.		
GPIO1_[15:22]	IO	The functionality of these signals is determined by the RCW[UART_BASE] & RCW[UART_EXT] field in the reset configuration word.		
GPIO1_[23:31]	IO	The functionality of these signals is determined by the RCW[IRQ_EXT] and RCW[IRQ_BASE] fields in the reset configuration word.		
GPIO2_[0:3]	IO	The functionality of these signals is determined by the RCW[SPI_EXT] and RCW[SPI_BASE] fields in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO2_[4:9]	IO	The functionality of these signals is determined by the RCW[SDHC_EXT] and RCW[SDHC_BASE] fields in the reset configuration word.		
GPIO2_[10:12]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_E1_BASE] field in the reset configuration word.		
GPIO2_[13:15]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_D_BASE] fields in the reset configuration word.		

Table continues on the next page...

Table 27. General Purpose Input/Output pin termination checklist (continued)

Signal Name	IO type	Used	Not Used	Completed
GPIO2_[25:27]	IO	The functionality of these signals is determined by the RCW[IFC_GRP_A_BASE] field in the reset configuration word.		
GPIO3_[0:1]	IO	The functionality of these signals is determined by the RCW[EM1] field in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO3_[2:14]	IO	The functionality of these signals is determined by the RCW[EC1] field in the reset configuration word.		
GPIO3_[15:27]	IO	The functionality of these signals is determined by the RCW[EC2] field in the reset configuration word.		
GPIO4_[0:1]	IO	The functionality of these signals is determined by the RCW[EM2] field in the reset configuration word.	For all GPIOx pins: When programmed as outputs, no termination is required.	
GPIO4_[2:3]	IO	The functionality of these signals is determined by the RCW[IIC2_EXT] field in the reset configuration word.		
GPIO4_[10:11]	IO	The functionality of these signals is determined by the IIC3_SCL and IIC3_SDA fields in **SCFG_RCWPMUXCR0** respectively.		
GPIO4_[12:13]	IO	The functionality of these signals is determined by the IIC4_SCL and IIC4_SDA fields in **SCFG_RCWPMUXCR0** respectively.		
GPIO4_[29]	IO	The functionality of these signals is determined by the RCW[USB_DRVVBUS] field in the reset configuration word.		
GPIO4_[30]	IO	The functionality of these signals is determined by the RCW[USB_PWRFAULT] fields in the reset configuration word.		

5.18 FTM1 pin termination recommendations

Table 28. FTM1 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM1_CH[0:7]	IO	The functionality of this signal is determined by the EC1 field in the reset configuration (RCW[EC1]).	Program as GPIOs and as outputs.	
FTM1_EXTCLK	I			
FTM1_FAULT	I			
FTM1_QD_PHA	I			
FTM1_QD_PHB	I			

5.19 FTM2 pin termination recommendations

Table 29. FTM2 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM2_CH[0:7]	IO	The functionality of this signal is determined by the EC2 field in the reset configuration (RCW[EC2]).	Program as a GPIO and as an output.	
FTM2_EXTCLK	I			
FTM2_FAULT	I			
FTM2_QD_PHA	I			
FTM2_QD_PHB	I			

5.20 FTM3 pin termination recommendations

Table 30. FTM3 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM3_CH[0:7]	IO	The functionality of these signals is determined by the IRQ_BASE and IRQ_EXT fields in the reset configuration word (RCW[IRQ_BASE] and RCW[IRQ_EXT]).	Program as a GPIO and as an output.	
FTM3_EXTCLK	I	The functionality of these signals is determined by the IIC4_SDA bitfield in register **SCFG_RCWPMUXCR0**		
FTM3_FAULT	I			
FTM3_QD_PHA	I	The functionality of these signals is determined by the IIC2_EXT fields in the reset configuration word (RCW[IIC2_EXT]).		
FTM3_QD_PHB	I			

5.21 FTM4 pin termination recommendations

Table 31. FTM4 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM4_CH[0:7]	IO	The functionality of FTM4_CH[0-5] signals is determined by the UART_EXT fields in the reset configuration word (RCW[UART_EXT]). The functionality of FTM4_CH6 and FTM4_CH7 signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).	Program as a GPIO and as an output.	
FTM4_EXTCLK	I	The functionality of these signals is determined by the SDHC_EXT fields in the reset configuration word (RCW[SDHC_EXT]).		
FTM4_FAULT	I			
FTM4_QD_PHA	I			
FTM4_QD_PHB	I			

5.22 FTM5 pin termination recommendations

Table 32. FTM5 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM5_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_A_EXT fields in the reset configuration word (RCW[IFC_GRP_A_EXT]).	Program as a GPIO and as an output.	
FTM5_EXTCLK	I			

5.23 FTM6 pin termination recommendations

Table 33. FTM6 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM6_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_D_EXT fields in the reset configuration word (RCW[IFC_GRP_D_EXT]).	Program as a GPIO and as an output.	
FTM6_EXTCLK	I			

5.24 FTM7 pin termination recommendations

Table 34. FTM7 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM7_CH[0:1]	IO	The functionality of these signals is determined by the IFC_GRP_E1_EXT fields in the reset configuration word (RCW[IFC_GRP_E1_EXT]).	Program as a GPIO and as an output.	
FTM7_EXTCLK	I			

5.25 FTM8 pin termination recommendations

Table 35. FTM8 pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
FTM8_CH[0:1]	IO	The functionality of these signals is determined by the IIC3_SCL and IIC3_SDA bitfields respectively in register **SCFG_RCWPMUXCR0**	Program as a GPIO and as an output.	

5.26 IEEE 1588 recommendations

5.26.1 IEEE 1588 pin termination recommendations

Table 36. IEEE 1588 pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
TSEC_1588_CLK_IN	I	Connect to external high-precisiontimer reference input. The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).	Program as GPIO's and output.	
TSEC_1588_ALARM_OUT1	O	The functionality of these signals is determined by the EC2 field in the reset configuration word (RCW[EC2]).		
TSEC_1588_ALARM_OUT2	O			
TSEC_1588_CLK_OUT	O			
TSEC_1588_PULSE_OUT1	O			

Table continues on the next page...

Table 36. IEEE 1588 pin termination checklist (continued)

Signal Name	I/O type	Used	Not used	Completed
TSEC_1588_PULSE_OUT2	O			
TSEC_1588_TRIG_IN1	I			
TSEC_1588_TRIG_IN2	I			

NOTE

When configured for IEEE 1588, the EC2 pins those are not available for IEEE 1588, are configured for GPIO. All IEEE 1588 pins are referenced to LV_{DD}.

5.27 System control pin termination recommendations

Table 37. System Control pin termination checklist

Signal Name	I/O type	Used	Not used	Completed
PORESET_B	I	This pin is required to be asserted as per the applicable chip data sheet, in relation to minimum assertion time and during power-up/power-down. It is an input-only pin and must be asserted to sample power on configuration pins.		
HRESET_B	I/O	This pin is an open drain signal and should be pulled high through a 2-10 kΩ resistor to OV_{DD}.		
RESET_REQ_B	O	Must not be pulled down during power-on reset.	This pin should be pulled high through a 2-10 kΩ resistor to OV_{DD} and must not be pulled down during power-on reset.	

NOTE

1. If on-board programming of NOR boot flash, QSPI boot flash, or SD card is needed, then maintain an option (may be via a jumper) that keeps PORESET_B and RESET_REQ_B disconnected from each other. Booting from a SPI flash causes boot error, which in turn causes assertion of RESET_REQ_B. When RESET_REQ_B is connected with PORESET_B, the device goes in a recurring reset loop and does not provide enough time for JTAG to take control of the device and perform any operation.
2. For RCW override, RESET_REQ_B should be disconnected from PORESET_B or HRESET_B. An option on board is required.

5.28 JTAG pin termination recommendations

Table 38. JTAG pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
TCK	I	Connect to pin 4 of the ARM Cortex 10-pin header. This pin requires a 2-10 kΩ resistor to OV_{DD}.		

Table continues on the next page...

Table 38. JTAG pin termination checklist (continued)

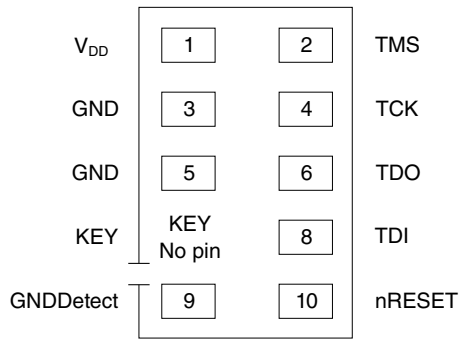
Signal Name	IO type	Used	Not Used	Completed
TDI	I	Connect to pin 8 of the ARM Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TDO	O	Connect to pin 6 of the ARM Cortex 10-pin header. This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
TMS	I	Connect to pin 2 of the ARM Cortex 10-pin header. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TRST_B	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled. Connect as shown in Figure 18.	Tie TRST_B to PORESET_B through a 0 kΩ resistor.	

5.28.1 JTAG system-level recommendations

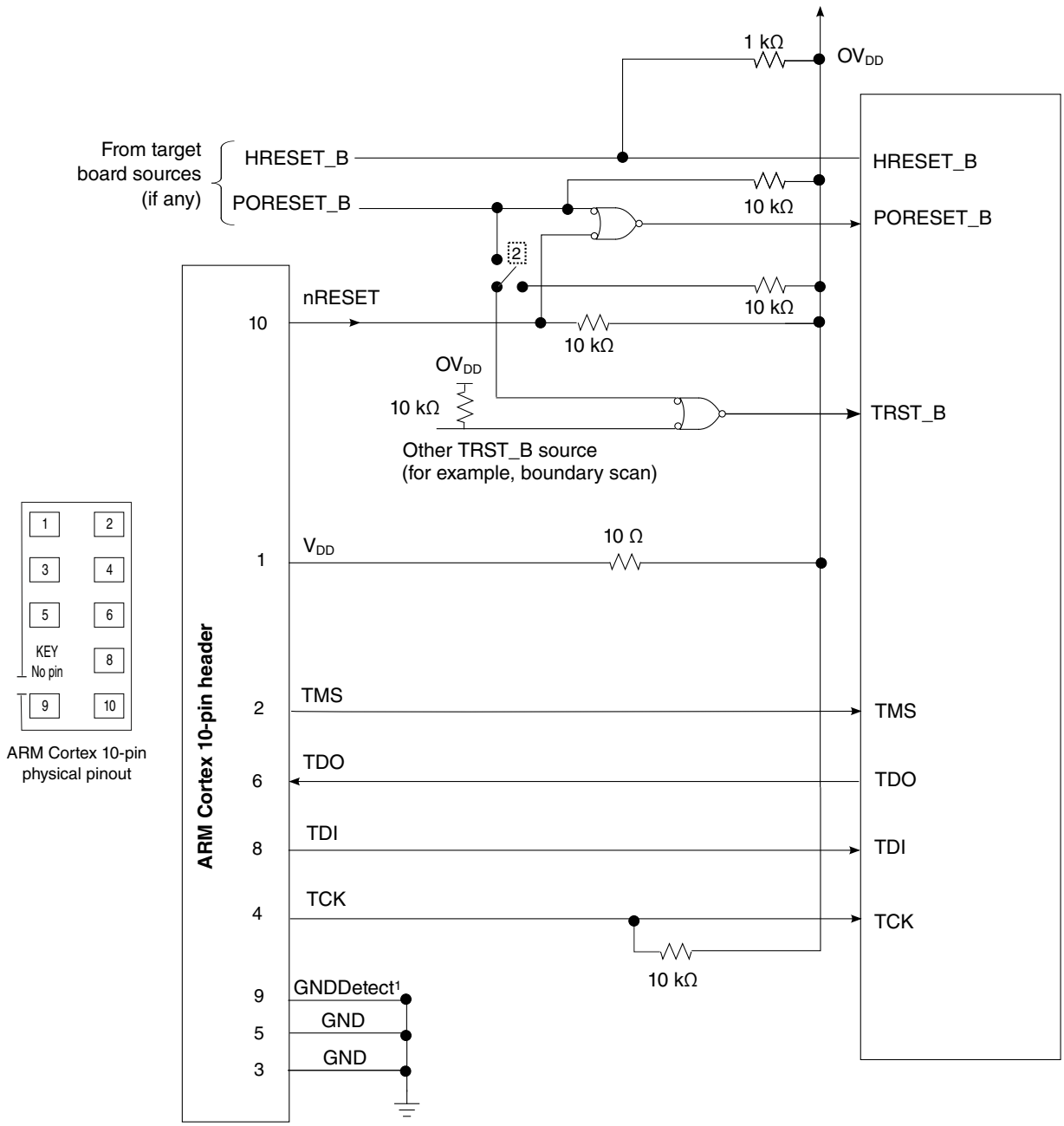
Table 39. JTAG system-level checklist

Item	Completed
ARM®Cortex® 10-pin header signal interface to JTAG port	
Configure the group of system control pins as shown in Figure 18. **NOTE:** These pins must be maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion gives unpredictable results.	
The JTAG port of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The ARM Cortex 10-pin header connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The ARM Cortex 10-pin header interface requires the ability to independently assert PORESET_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the nRESET signals must be merged into these signals with logic.	
Boundary-scan testing	
Ensure that TRST_B is asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation.	
Follow the arrangement shown in Figure 18 to allow the ARM Cortex 10-pin header to assert PORESET_B independently while ensuring that the target can drive PORESET_B as well.	
The ARM® Cortex® 10-pin interface has a standard header, shown in the following figure. The connector typically has pin 7 removed as a connector key. The signal placement recommended in this figure is common to all known emulators.	

Table 39. JTAG system-level checklist

Item	Completed
 **NOTE:** The ARM Cortex 10-pin header adds many benefits such as breakpoints, watch points, register and memory examination/modification, and other standard debugger features. An inexpensive option is to leave the ARM Cortex 10-pin header unpopulated until needed.	

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 18. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion gives unpredictable results.



Note:
1. GNDDetect is an optional board feature. Check with 3rd-party tool vendor.
2. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, ensure this switch is closed.

Figure 18. JTAG interface connection

5.29 Clock pin termination recommendations

Table 40. Clock pin termination checklist

Signal Name	IO type	Used	Not Used	Completed
EC1_GTX_CLK	O	The functionality of this signal is determined by the EC1 field in the reset configuration word (RCW[EC1]). LS1046A has a duty cycle reshaper inside RGMII block. This allows GTX clock from RGMII PHY to be used.	Program as a GPIO and as an output.	
EC1_GTX_CLK125	I			
EC2_GTX_CLK	O	The functionality of this signal is determined by the EC2 field in the reset configuration word (RCW[EC2]). LS1046A has a duty cycle reshaper inside RGMII block. This allows GTX clock from RGMII PHY to be used.	Program as a GPIO and as an output.	
EC2_GTX_CLK125	I			
SYSCLK[1]	I	This is the single-ended primary clock input to the chip. It supports a 100 MHz clock.	This pin should be pulled low through a 2-10 kΩ resistor to GND.	
DIFF_SYSCLK[3]	I	These pins are the differential primary clock input to the chip. These pins support 100 MHz only. When used, these pins should be connected to a 100 MHz differential clock generator. The LVDS receiver for differential sysclk input requires a minimum of 50mV of common mode voltage, so AC couplings cannot be used on board to interface the receiver.	These pins should be pulled low through a 2-10 kΩ resistor to GND, or they can be left floating.	
DIFF_SYSCLK_B[3]	I			
RTC	I	The functionality of this signal is determined by the RTC field in the reset configuration word (RCW[RTC]). RTC is the only clock source for WDOG functionality. To support WDOG functionality RTC required 32 KHz external clock source. Without supplying the 32 KHz external clock source the WDOG functionality will be inoperable.	Pull low through a 2-10 kΩ resistor to GND, or program pin as a GPIO and output.	
DDRCLK[2]	I	The reference clock for the DDR controller supports a 100 MHz input clock.	This pin should be pulled low through a 2-10 kΩ resistor to GND.	

NOTE

1. In the "Single Oscillator Source" reference clock mode supported by LS1046A, DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs are used as primary

clock inputs and SYSCLK is unused. Power-on-configuration signal cfg_eng_use0 selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) clock inputs.

2. In the "Single Oscillator Source" reference clock mode, DIFF_SYSCLK/ DIFF_SYSCLK_B clock inputs can be selected to feed the DDR PLL. RCW bits [DDR_REFCLK_SEL] are used for this selection and DDRCLK is unused. The options for RCW bits 186-187 are as follows:
    a. RCW[DDR_REFCLK_SEL]=00; The DDRCLK pin provides the reference clock to the DDR PLL
    b. RCW[DDR_REFCLK_SEL]=01; DIFF_SYSCLK/DIFF_SYSCLK_B provides the reference clock to the DDR PLL
3. When SYSCLK is chosen as the primary clock input to the chip, these pins are unused.
4. Either of the EC1_GTX_CLK125 or EC2_GTX_CLK125 can be used to clock both the EC interfaces in RGMII mode. The selection can be made through SCFG_ECGTXCMCR[CLKSEL].

5.30 Single source clocking

The chip supports the single source clocking options with single, two, and more reference clocks.

5.31 Single oscillator source reference clock mode

In this mode, single onboard oscillator can provide the reference clock (100 MHz) to the following PLLs:

- Platform PLL
- Core PLLs
- USB PLL
- DDR PLL
- SerDes PLLs

The reset configuration field identifies whether the SYSCLK (single-ended) or DIFF_SYSCLK (differential) is selected as the clock input to the chip.

The RCW[DDR_REFCLK_SEL] bit is used to select clock input (DIFF_SYSCLK or DDRCLK) to the DDR PLL.

The following figure shows the system view of single oscillator source clocking. In this figure, the on-board oscillator generates three differential clock outputs. The first differential output is used to provide the clock to system clock associated PLLs and DDR PLL. However, the second and third differential outputs are used to provide clocks to SerDes PLLs.

A multiplexer between SYSCLK and DIFF_SYSCLK/DIFF_SYSCLK_B is used to provide the USB PHY reference clock to the USB PLL. And, multiplexer between DIFF_SYSCLK/DIFF_SYSCLK_B inputs and DDRCLK is used to provide reference clock to the DDR PLL.

The duty cycle reshaper reshapes the 125 MHz EC*n*_GTX_CLK125 which is fed into frame manager for transmission as EC*n*_GTX_CLK.

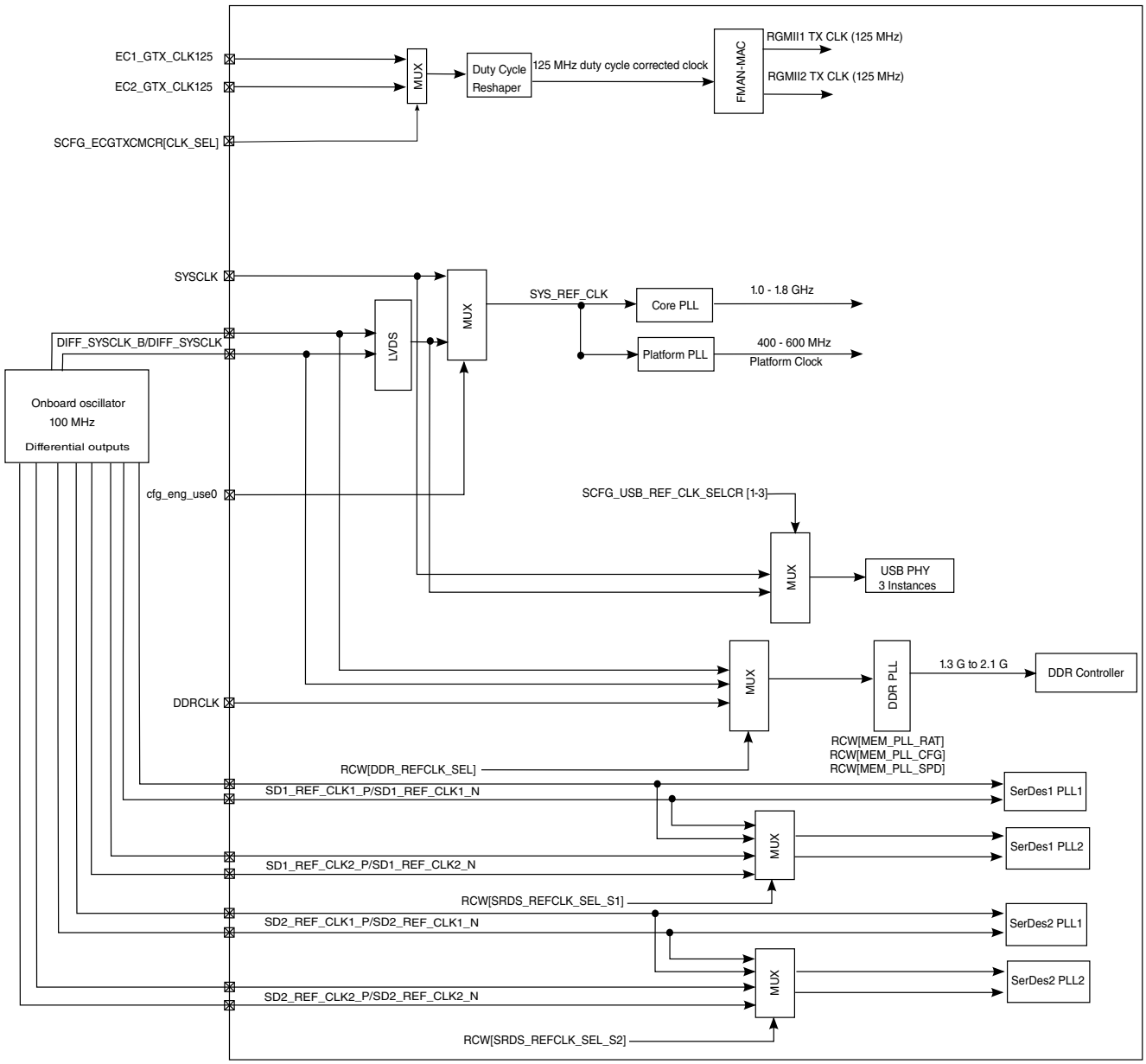


Figure 19. Single oscillator source clocking

5.32 *Single Oscillator Source* clock select

The single oscillator source clock select input, described in this table, selects between SYSCLK (single ended) and DIFF_SYSCLK/DIFF_SYSCLK_B (differential) inputs.

Table 41. Single oscillator source clock select

Functional signals	Reset configuration name	Value (binary)	Options
IFC_WE0_B Default (1)	cfg_eng_use0	0	DIFF_SYSCLK/DIFF_SYSCLK_B (differential)
		1	SYSCLK (single ended)

Table continues on the next page...

Table 41. Single oscillator source clock select (continued)

Functional signals	Reset configuration name	Value (binary)	Options
IFC_OE_B	cfg_eng_use1	0	On-chip LVDS termination disabled
Default (1)	On-chip LVDS termination must NOT be enabled when external (off-chip) termination are active.	1	On-chip LVDS termination enabled
IFC_WP_B[0]	cfg_eng_use2	Don't care	Reserved

5.33 DIFF_SYSCLK/DIFF_SYSCLK_B system-level recommendations

Table 42. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist

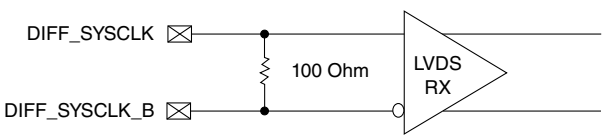
Item	Completed
DIFF_SYSCLK/DIFF_SYSCLK_B can be selected to provide primary clock to the chip. Although it is a Low Voltage Differential Signaling (LVDS) type clock driver but it has AC/DC characteristics identical to the SerDes reference clock inputs which are High-Speed Current Steering Logic (HCSL)-compatible. This eases system design as same clock driver can be used to provide the various differential clock inputs required by the chip  **Figure 20. LVDS receiver**	
Interfacing DIFF_SYSCLK/DIFF_SYSCLK_B with other Differential Signalling levels	
Connection with HCSL Clock driver	

Table continues on the next page...

Table 42. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist (continued)

Item	Completed

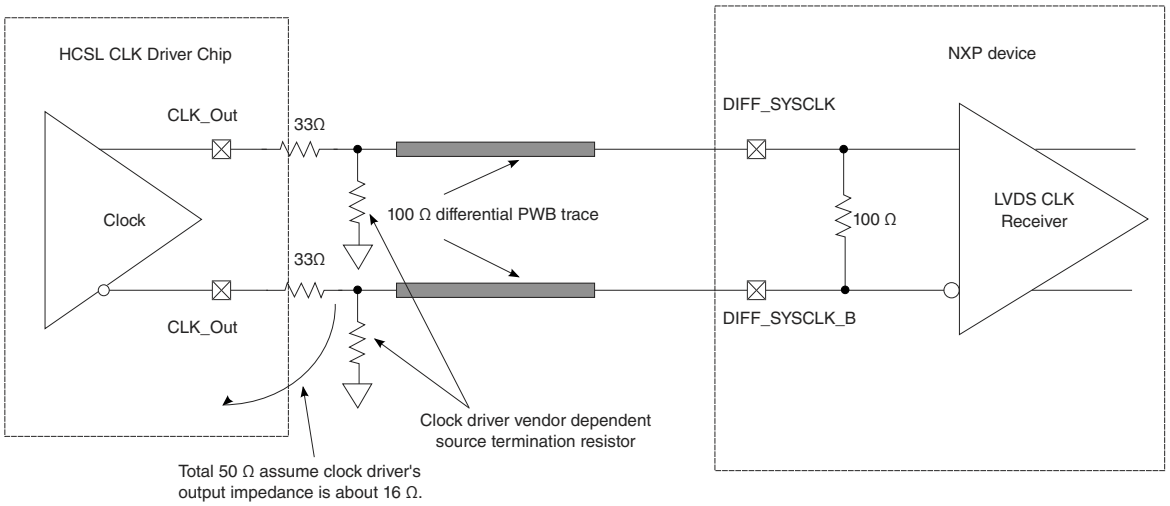



Figure 21. Interfacing with HCSL clock driver (Reference only)	
Connection with LVDS Clock driver	

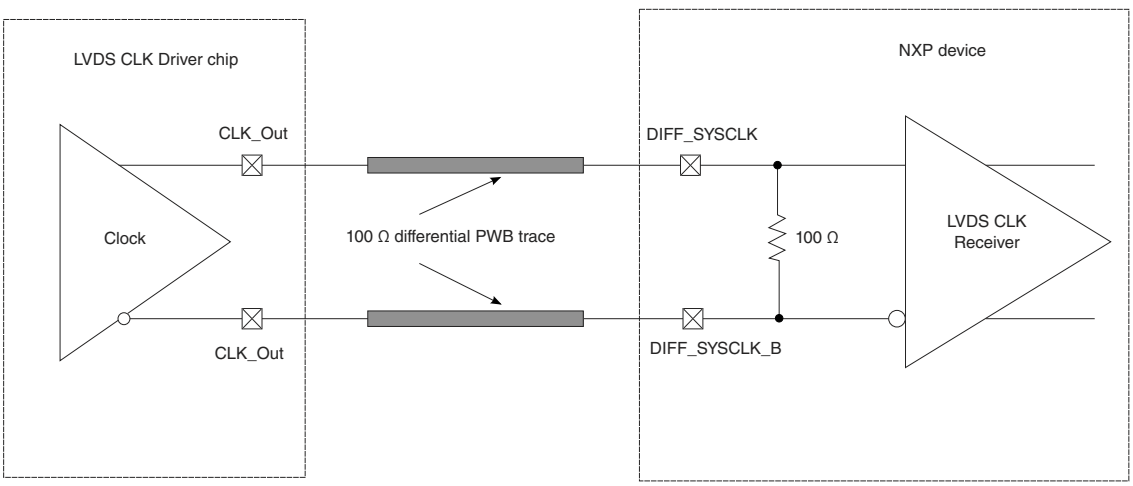



Figure 22. Interfacing with LVDS clock driver (Reference only)	
Connection with LVPECL Clock driver	

Table continues on the next page...

Table 42. DIFF_SYSCLK/DIFF_SYSCLK_B system-level checklist (continued)

Item	Completed

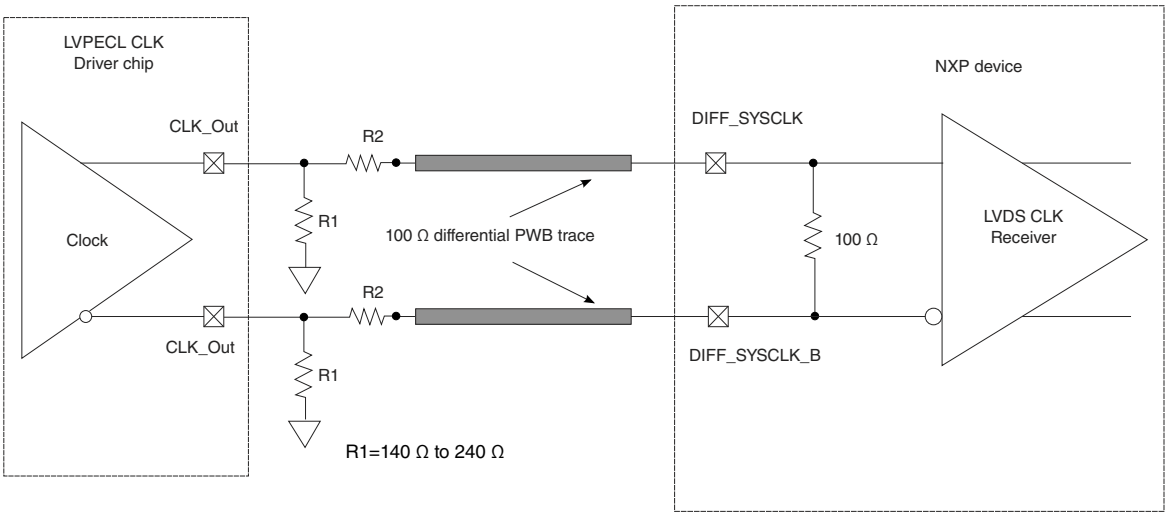
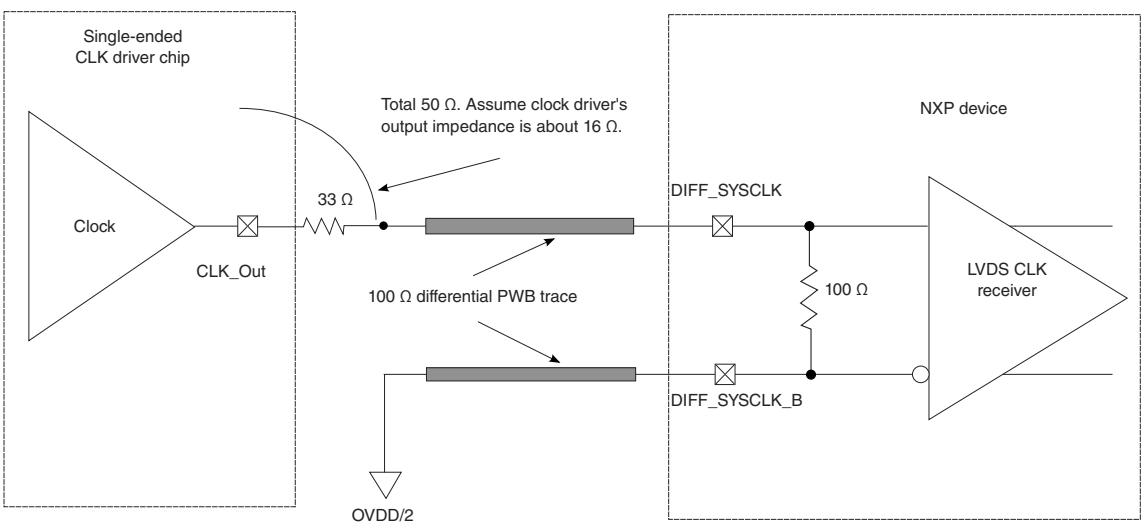



Figure 23. Interfacing with LVPECL clock driver (Reference only)	
Single-Ended Connection with Clock driver The DIFF_SYSCLK_B should be terminated to OVDD/2 	
Figure 24. Single ended connection (Reference only)	

6 Thermal

This section lists the thermal model and management of the chip.

6.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

6.2 Thermal system-level recommendations

Proper thermal control design is primarily dependent on the system-level design — the heat sink, airflow, and thermal interface material.

Table 43. Thermal system-level checklist

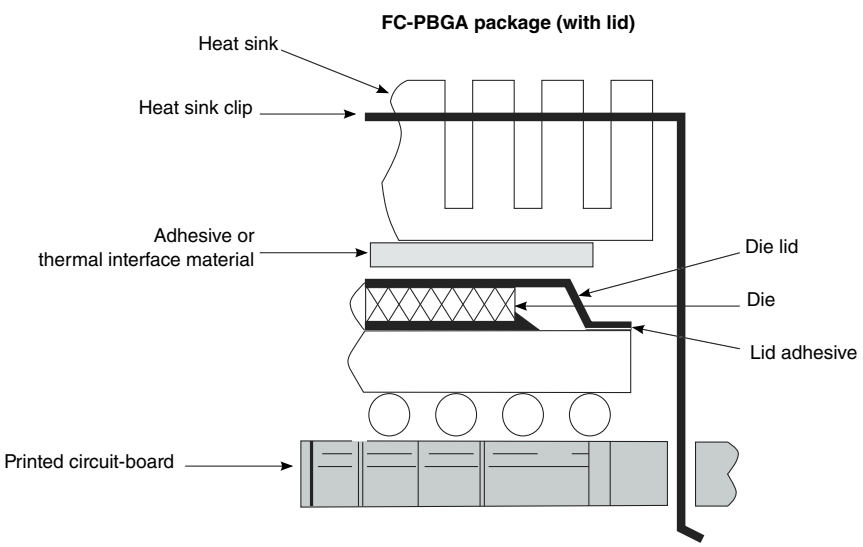
Item	Completed
Use the recommended thermal model. Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.	
Use this recommended board attachment method to the heat sink:[1] The processor heat sink must be connected to GND at one point for EMC performance. GND here specifies processor ground.  **Figure 25. Cross-sectional view of FC PBGA with lid**	
Ensure the heat sink is attached to the printed-circuit board with the spring force centered over the package.[2]	
Ensure the spring force does not exceed 15 pounds force (65 Newtons).	

Table continues on the next page...

Table 43. Thermal system-level checklist (continued)

Item	Completed
A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance.[3]	
Ensure the method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board.	
A thermal simulation is required to determine the performance in the application.[4]	

Notes:

1. The system board designer can choose among several types of commercially available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

2. The performance of the thermal interface materials improves with increased contact pressure; the thermal interface vendor generally provides a performance characteristic to guide improved performance.

3. The system board designer can choose among several types of commercially available thermal interface materials.

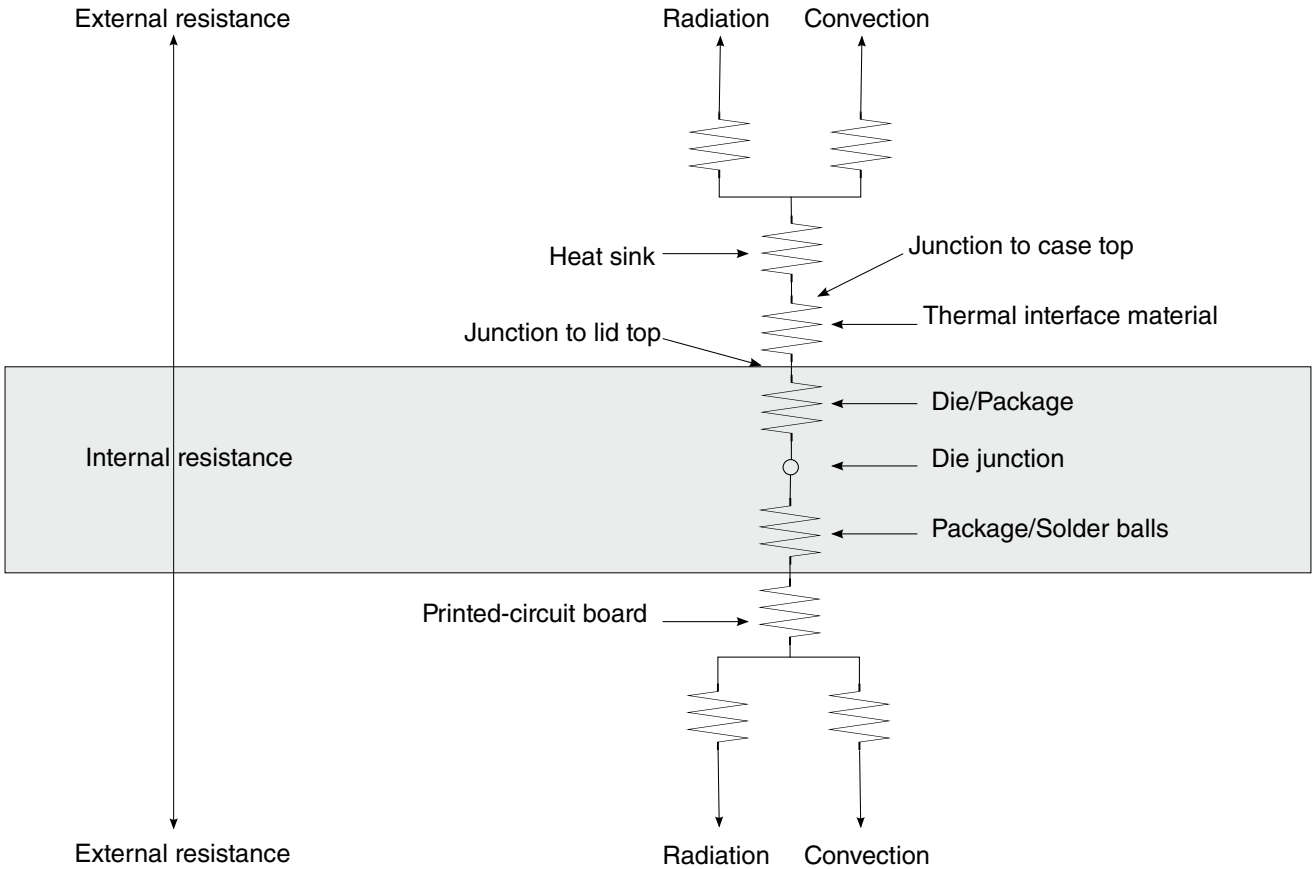
4. A Flotherm model of the part is available.

6.3 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 26. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

7 Revision history

This table summarizes changes to this document.

Table 44. Revision history

Revision	Date	Change summary

2	06/2020	• Added general description for unused pins of different interfaces in Interface recommendations
		• In Ethernet controller pin termination recommendations
		  • Updated description for unused pins
		  • Added "The unused clock pin should be pulled to GND" in the note

Table continues on the next page...

Table 44. Revision history (continued)

Revision	Date	Change summary
		• Updated note 3 as "If RCW[IFC_GRP_A_EXT]=001, IFC_A26 and IFC_A27 should be pulled to GND through 4.7 kΩ resistor. Otherwise these pins should be configured as output GPIOs and left as unconnected" in QSPI pin termination recommendations • Updated note as "For supported voltage/frequency/temperature range options, see the orderable part list of QorIQ LS1046A and LS1026A Multicore Communications Processors at www.nxp.com." in Power pin recommendations

1	11/2019	• Added note below Table 3
		• Updated used instruction for MALERT_B, added note on RAS, CAS, WE and CS in DDR SDRAM memory interface pin termination recommendations
		• Added note below SerDes pin termination recommendations
		• Added note for unused PWRFAULT signal USB PHY pin termination recommendations
		• Added note for unused SDHC_DAT[1:3] signals and updated description of not used SDHC_WP pin in eSDHC pin termination recommendations
		• Removed SPI_BASE field for SDHC_CLK_SYNC_IN/OUT in eSDHC pin termination recommendations
		• Added note 3 in QSPI pin termination recommendations
		• Added note 6 in Table 15 and updated Figure 14
		• Updated JTAG configuration files path in Configuration signals sampled at reset
		• Corrected typo "HRESET_REQ_B" and added note referring AN12081 in Hard-coded RCW
		• Corrected typo "fields" and "LPUART[1:3]_RTS_B" in LPUART pin termination recommendations
		• Changed RCW[IIC2_BASE] to RCW[IIC2_EXT] in I2C pin termination recommendations
		• Updated description for not used IRQ pins in GIC pin termination recommendations
		• Updated description for EVT_B[9], JTAG_BSR_VSEL and TBSCAN_EN_B in Debug and reserved pin termination recommendations
		• Updated IO type of GPIO1_13 from IO to O in General Purpose Input/Output pin termination recommendations
		• Removed "blanked NAND" from note in System control pin termination recommendations
		• Updated description for RTC pin in Clock pin termination recommendations
		• In Ethernet Management Interface 1/2 pin termination recommendations
		  • Updated description for not used EMI1_MDC and EMI2_MDC pins
		  • Corrected typo "LVDD" by "TVDD" in description of used EMI2_MDIO pin
		• In Ethernet controller pin termination recommendations
		  • Updated description for not used EC1_GTX_CLK and EC2_GTX_CLK pins
		  • Changed I/O type of EC2_GTX_CLK from I to O
		• Corrected "configuration signals to the chip when HRESET_B is asserted" to "configuration signals to the chip when PORESET_B is asserted" in Power-on and Reset recommendations
		• Added Figure 2

0	08/2017	Initial release

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