

# Using the MC34845 for Larger LCD Displays

By: Rafael García Mora

## 1 Overview

This document shows how to design and configure the IC to drive more than 16 LEDs on each of the channels, thereby extending its capabilities to backlight larger LCD displays.

## 2 Scope

The MC34845 series features high efficiency LED drivers for use in backlighting LCD displays from 10" to 17"+. Operating from supplied voltages of 5.0 V to 21.0 V, the MC34845 series is capable of driving LED in series, in 6 separate strings with an LED current tolerance within a maximum of  $\pm 2\%$ .

### Contents

<b>1 Overview</b> .....	<b>1</b>
<b>2 Scope</b> .....	<b>1</b>
<b>3 LCD Backlighting and MC34845 Overview</b> ..	<b>2</b>
<b>4 References</b> .....	<b>9</b>

### 3 LCD Backlighting and MC34845 Overview

LED backlights use different architecture depending on the size of the display and features required. For displays in the 7" to 17" range, such as those used in notebooks, edge-lit backlights offer very thin designs down to 2.0 mm or less. The efficiency of the LED backlight also extends battery life in portable equipment compared to CCFL. In large size panels, direct backlights support advanced architectures, such as local dimming, in which power consumption and contrast ratio are drastically improved. Edge lighting can also be used in large displays when low cost is the driving factor.

#### 3.1 Typical Application of the MC34845

The integrated boost converter uses a Dynamic Headroom Control (DHC) loop to automatically set the output voltage needed to drive the LED strings. The DHC is designed to operate under specific pulse width conditions in the LED drivers. It operates for pulse widths higher than 400 ns. If the pulse widths are shorter than specified, the DHC circuit will not operate and the voltage across the LED drivers will increase to a value given by the OVP, minus the total LED voltage in the LED string. It is therefore imperative to select the proper OVP level, to avoid exceeding the max off state voltage of the LED drivers (45 V).

The device has an internally fixed OVP value of 60 V (typical), which serves as a secondary fault protection mechanism, in the event the externally programmed OVP fails (i.e. resistor divider opens up). While the internal 60 V OVP detector can be used exclusively without the external OVP network, this is only recommended for applications where the LED string voltage approaches 55 V or more. The OVP level can be set by using an external resistor divider connected between the output voltage and ground, with its output connected to the OVP pin. The OVP can be set up to 60 V, by varying the resistor divider to match the OVP internal reference of 6.9 V (typical).

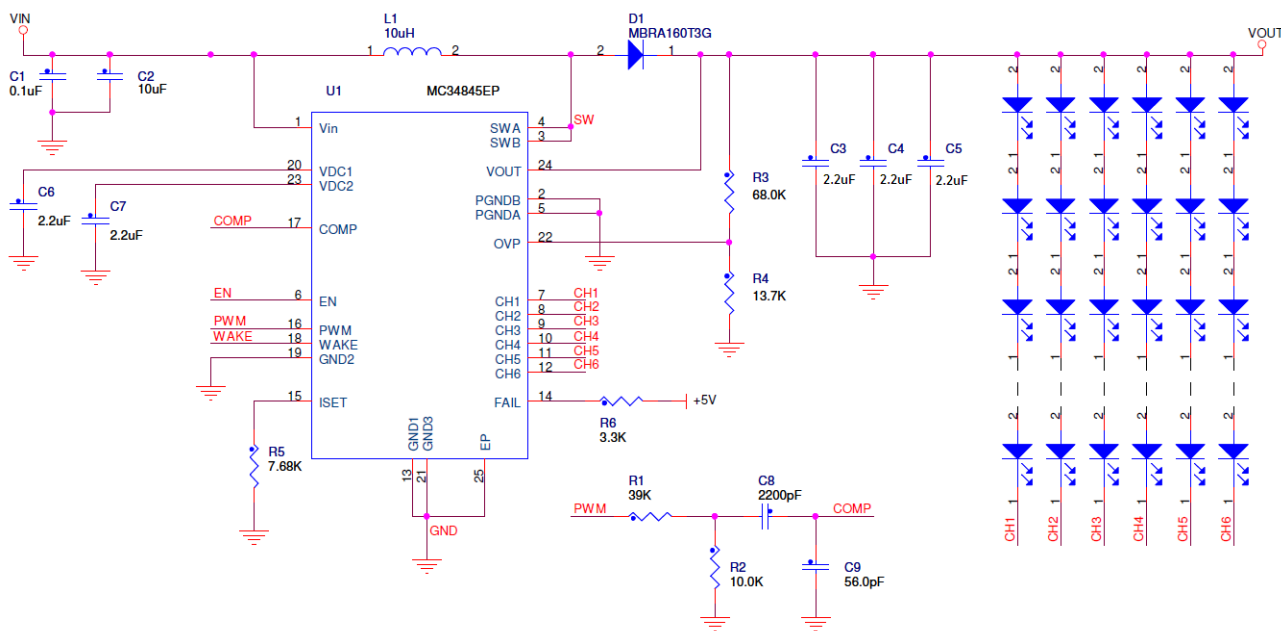


Figure 1. Typical application circuit  $F_{sw} = 600 \text{ kHz}$  ( $V_{in} = 5.0 \text{ V}$ ;  $I_{LED/channel} = 20 \text{ mA}$ ; 12 LEDs/channel;  $OVP=45 \text{ V}$ ;  $V_{PWM}=5.0 \text{ V}$ )

### 3.2 Driving More Than 60 V

Checking the absolute maximum ratings of the device, it can be noted that the internal MOSFET of the boost converter has a Drain to Source breakdown voltage of 65 V (SWA and SWB pins respect to GND). Furthermore, the typical internal over-voltage protection level is limited to 60 V. To err on the side of caution, it is recommended to set the OVP level 5.0 V above the worst case LED string voltage. As a result, the maximum voltage at the output of the boost is limited to 60 V, which gives the possibility of driving up to 16 LEDs in series per string. Driving more LEDs at higher voltages looks impossible due to device limitations. However, there is an attractive alternative to drive circuits at higher voltages and currents, called **cascode connection**, which consists of placing the driving switch in series with a power switch, so that both devices must conduct the same current, as shown in [Figure 2](#).

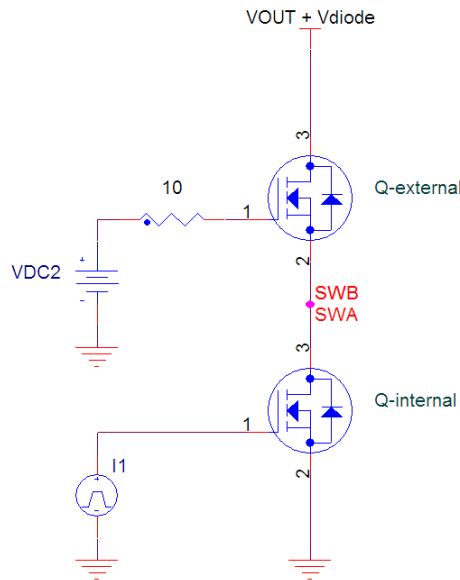


Figure 2. Cascode Driving Configuration

As can be seen in [Figure 2](#), the upper transistor is permanently gate triggered by a constant input voltage, such as  $V_{DC2}$ , but remains off as long as the lower transistor is off as well. Once the lower transistor is switched on, the upper transistor automatically starts conducting the main current. In this configuration, the drain to source off state blocking voltage stress of the internal transistor is considerably reduced, when using an external MOSFET with an equal or larger breakdown voltage capability. The off state drain to source voltage of the lower certainly depends on the gate voltage source of the upper transistor, as the maximum off state drain to source voltage of the lower transistor will be twice the  $V_{DC2}$  voltage. As a result, most of the off state blocking voltage will be present in the drain to source pins of the upper transistor, and give the possibility of driving more than 60 V at the output of the Boost converter.

Similarly, the boost output voltage feedback pin, **VOUT**, is limited to a maximum voltage of 65 V. A higher voltage at this pin will cause the boost converter section to be off at all times. In order to get more than 60 V and fake a normal performance in the feedback pin, it is necessary to add zener diodes between the output voltage of the boost converter and the **VOUT** pin, so that the device “believes” is working well below the maximum rating. The clamping voltage rate of the zeners will depend on the maximum over-voltage protection level expected, so that  $V_{OUT\_MAX} + 5.0\text{ V} - V_{ZENER(S)}$  is lower than the maximum voltage at the **VOUT** pin. Besides, this modification to the application circuit also enables the use of the internal OVP feature as the **VOUT** pin internally works as the triggering variable for the 60V protection. As a result, the resistor divider previously used at the OVP pin will be no longer necessary as shown in [Figure 3](#).

## LCD Backlighting and MC34845 Overview

As the MC34845 employs current mode control, the slope compensation is an important parameter to consider during feedback loop analysis and inductor selection. This parameter is fixed within the IC and could be obtained from:

$$V_{\text{SLOPE}} \approx \frac{V_{\text{OUT}} - V_{\text{IN}}}{2 \times L} \times 0.2$$

As the output voltage needs to be increased to drive more LEDs and the slope compensation parameter is fixed, then the value of the inductor needs to be recalculated accordingly to keep the system working correctly. When doing so, the typical value of the slope compensation shown in the MC34845 datasheet and the worst case operation condition (i.e. minimum input voltage permitted for maximum duty cycle), need to be taken into consideration. An off-the-shelf inductance value should be picked as close as possible to the calculated one.

The value of the output capacitor as well as the network compensation components may change along with the new inductor value. Proceed to verify whether these values really work for the final application, i.e. slight jitter on the switching node waveform, operation in Continuous Conduction mode at 100% duty cycle, and low output voltage ripple. Otherwise, the component calculation section of the MC34845 datasheet must be checked for recalculation of these components.

Practically, the maximum number of LEDs that can be driven per string is limited by any of these conditions:

- a) LED short protection voltage, SFDV .- During the on times of the PWM dimming, if the voltage across the LED driver channel is higher than this parameter ( $6.5V \leq \text{SFDV} \leq 7.5V$ ) the channel is immediately disabled for protection. This voltage drop will heavily depend on the voltage mismatch among the LEDs strings. For this reason, it must be assured that on each channel:

$$V_{\text{OUT}} - (V_{\text{LED1\_PWM-ON}} + V_{\text{LED2\_PWM-ON}} + V_{\text{LED3\_PWM-ON}} + \dots + V_{\text{LEDn\_PWM-ON}}) \leq \text{SFDV}$$

- b) Maximum off state voltage, VMAX .- During the off times of the PWM dimming, if the voltage drop across the LED driver channel is higher than 45V, the device will probably get damaged. A wise approach to get full protection to each of the LED drivers as well as the DC/DC converter could be use the external OVP feature to shutdown the part if any string during the off time goes above 40V. Consider placing a 33V or so Zener from the bottom of each string to a common resistor pull-down. The junction is tied to the OVP pin. Then if the off time voltage goes  $33V + 6.9V \approx 40V$ , the external OVP feature will force the DC/DC converter to stop boosting. As a result, it is possible to get full protection this way: external OVP for LED off time voltage at the LED drivers and internal OVP for output voltage of the DC/DC converter. This implementation is shown in [Figure 3](#).

The next figure shows an application example capable driving up to 26 LEDs at a maximum output voltage  $\approx 78V$ , with an OVP level set at 82.6V, and using two zener diodes connected to the **VOU**T pin.

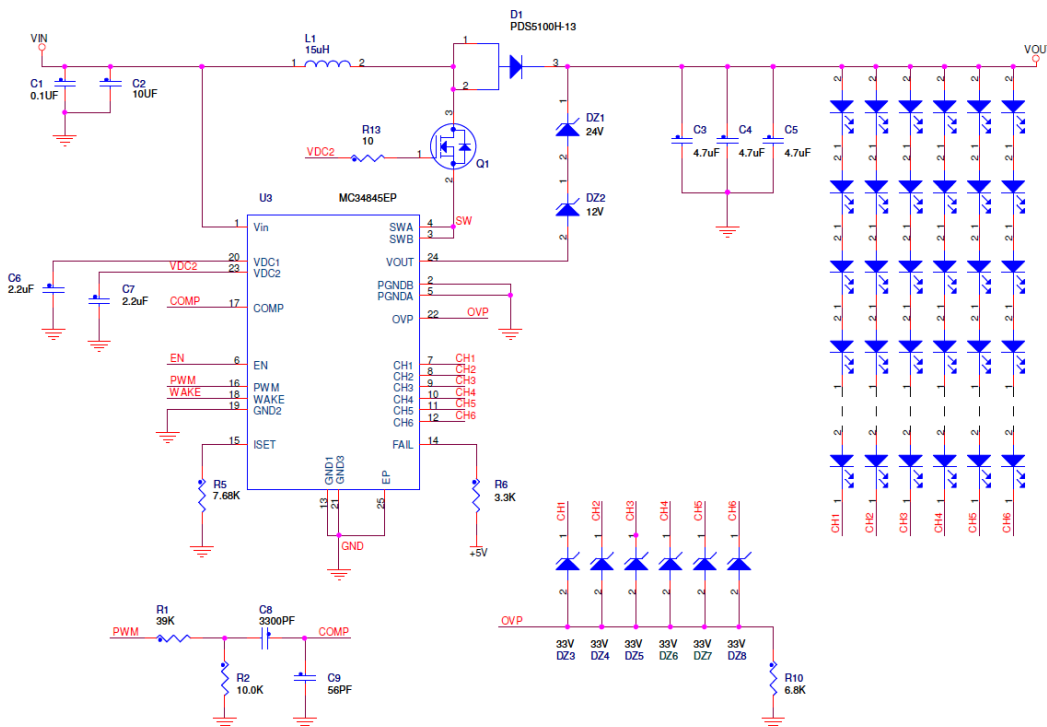


Figure 3. I Application Circuit

Fsw = 600 kHz (Vin = 9.0 V; I<sub>LED/channel</sub> = 20 mA; 26 LEDs/channel; OVP = 82.5 V; V<sub>PWM</sub> = 5.0 V)

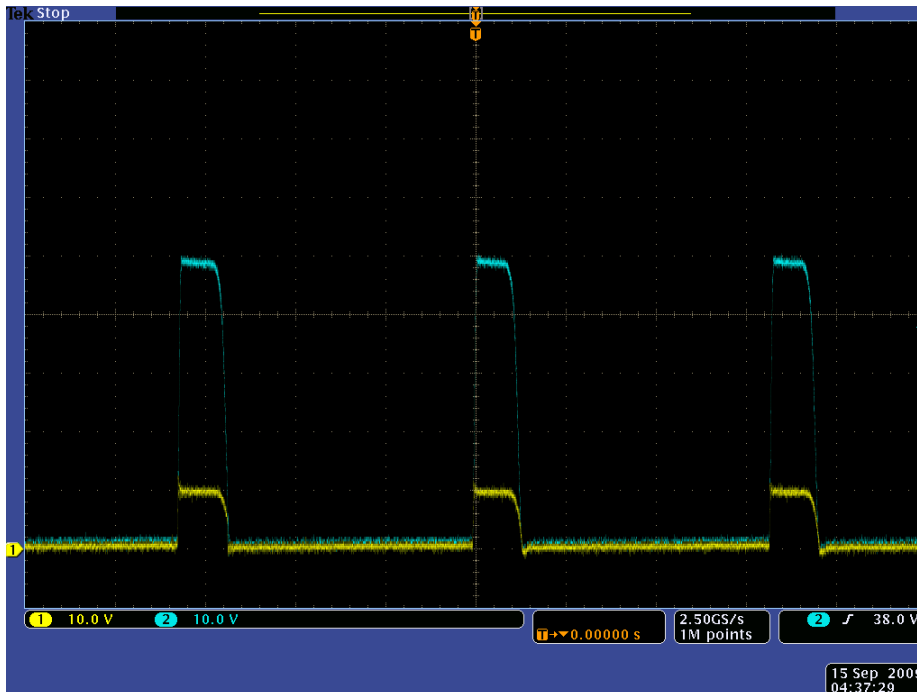


Figure 4. Switching Node Voltage Waveforms when Driving 16 LEDs.

## LCD Backlighting and MC34845 Overview

In [Figure 4](#), the blue waveform is the drain to source waveform from the SW node (48 V) to GND, which implies both MOSFETs are switching. The yellow waveform is the drain to source waveform of the internal MOSFET. Notice that the off state voltage drop is no higher than two  $V_{DC2}$ .

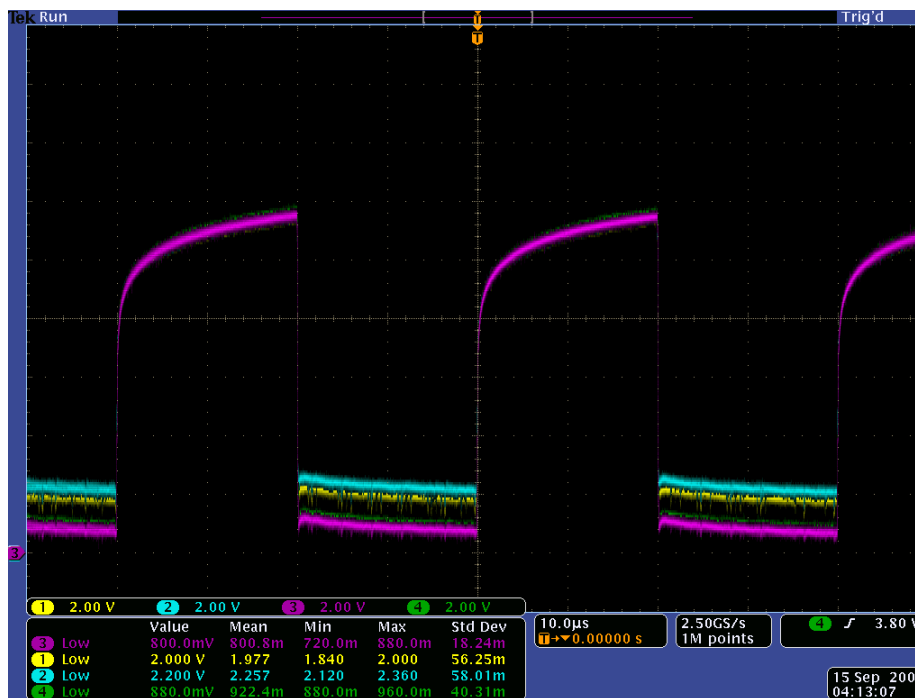


Figure 5. LED Driver Channel Pin Voltages when Driving 16 LEDs

[Figure 5](#) shows the different on state voltage drops at four different LED driver channel pins during PWM dimming. Notice that when the LED channels are off, the voltage at the pins is approximately 12 V, well below  $V_{MAX} = 45$  V. Similarly, when the LED channels are on, the voltage at the pins are between 0.8 and 2.2 V, below the LED short protection voltage,  $S_{FDV}$ .

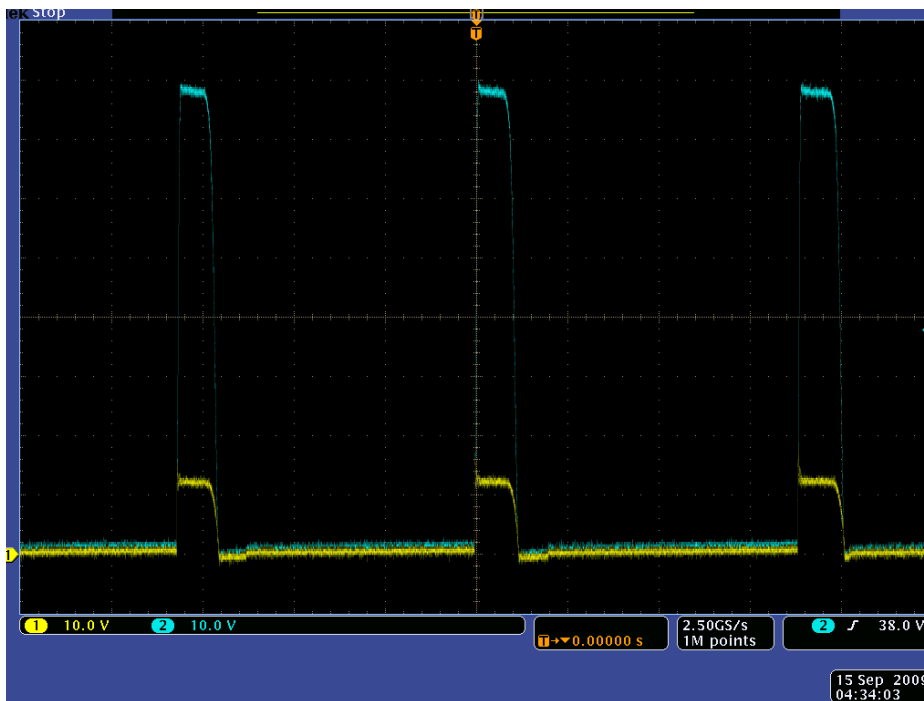


Figure 6. Switching Node Voltage Waveforms when Driving 26 LEDs.

In [Figure 6](#), the blue waveform is the drain to source waveform from the SW node (78 V) to GND, which implies both MOSFETs are switching. The yellow waveform is the drain to source waveform of the internal MOSFET. Notice that the off state voltage drop is no higher than two  $V_{DC2}$ .

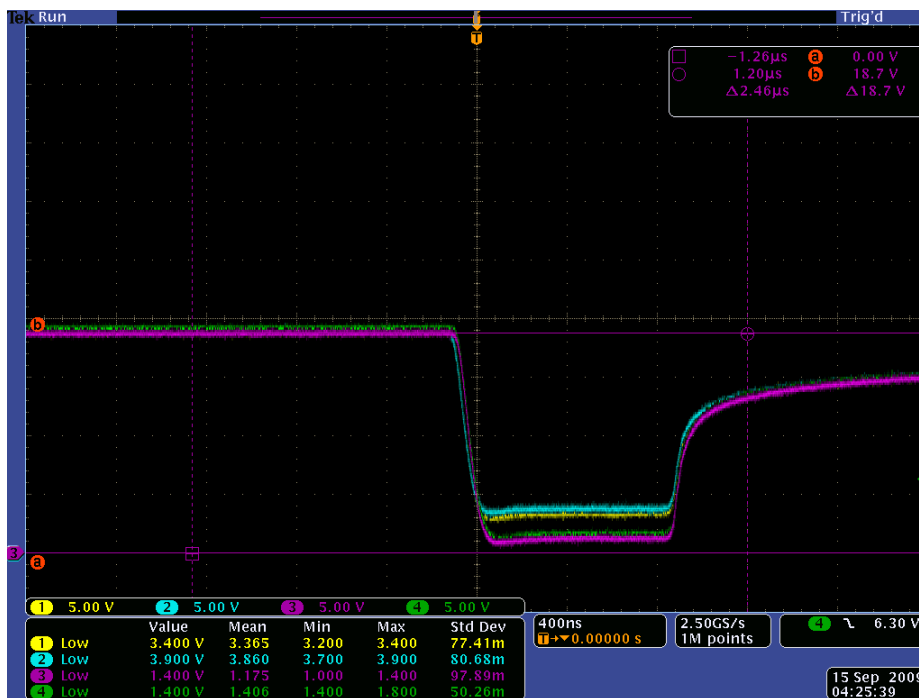


Figure 7. LED Driver Channel Pin Voltages when Driving 26 LEDs

## LCD Backlighting and MC34845 Overview

[Figure 7](#) shows the different off state voltage drops at four different LED driver channel pins during PWM dimming. Once again, when the LED channels are off, the voltage at the pins is approximately 18 V, well below  $V_{MAX} = 45$  V, and when the LED channels are on, the voltage at the pins is between 1.1 and 3.9 V, below the LED short protection voltage,  $S_{FDV}$ .

In summary, the most important features to consider when designing an application with an output voltage higher than 60 V, up to 120 V are:

1. The off state blocking voltage capability of the external MOSFET is recommended to be greater than 100 V for safe operation.
2. The Boost converter diode D1 must have a reverse blocking voltage capability of at least 100 V.
3. The output capacitors must be rated at 100 V for safe operation. If high voltage ceramic capacitors are used, it may be necessary to add more capacitance to the output, as it is well known that some ceramic capacitors drop their capacitance value when increasing the DC voltage across them. If other technology is used (e.g. electrolytic) a single capacitor may be enough.
4. A 10  $\Omega$  resistor should be used at the gate of the external MOSFET to avoid false triggering.
5. Quarter watt zener diodes can be used. Be sure that the clamping voltage of the zeners keep **VOUT** well below 60 V at all times, even at OVP events.
6. The duty cycle of the switching frequency of a Boost converter while in CCM is dictated by the following equation:

$$D = \frac{V_{OUT} + V_D + V_{IN}}{V_{OUT} + V_D - V_{SW}} \times 100\%$$

where:

$V_{OUT}$  = Boost converter output voltage.

$V_{IN}$  = Boost converter input voltage.

$V_D$  = Voltage drop of the diode while conducting

$V_{SW}$  = Voltage drop across the MOSFET while conducting =  $R_{DS-ON} \times$  Current limit

Take into consideration that the maximum duty cycle is limited to 90%. As a result, to get voltages higher than 60 V and keep the system electrically and thermally stable, it will be necessary to increase the input voltage to a proper level, so as to keep the device within the limits.

7. The off state leakage current per channel is 1.0  $\mu$ A. In order to keep the voltage across each of the LED driver channels well below  $V_{MAX}$  during the off times of the PWM dimming, it is recommended to check the minimum voltage drop of the LEDs used, when the forward current is approximately 1.0  $\mu$ A. For this reason, the external OVP protection configuration in [Figure 3](#) for each of the LED driver channels is proposed.
8. These circuit adaptations for driving more than 60V are exclusively recommended to the MC34845 (600kHz version) and the MC34845B (300kHz version) devices in order to keep the power switching losses and EMI emissions within acceptable limits.



## 4 References

- [MC34845 Datasheet](#)
- MOHAN, Ned; Undeland Tore and Robbins William, *Power Electronics, Converters, Applications and Design*. John Wiley and Sons press, 2nd Edition. U.S. 1995.

## How to Reach Us:

### Home Page:

[www.freescale.com](http://www.freescale.com)

### Web Support:

<http://www.freescale.com/support>

### USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### Japan:

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### Asia/Pacific:

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or +1-303-675-2140  
Fax: +1-303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009. All rights reserved.