AN12999

NTAG 22x StatusDetect - Capacitive sensing guidelines

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Application note
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Document information

Information	Content
Keywords	NTAG 22x DNA StatusDetect, NFC capacitive sensing, design guidelines
Abstract	Guidelines for designing-in NFC capacitive sensing based on NTAG 22x DNA StatusDetect product

Revision history

Rev	Date	Description
v 1.3	20220323	Correction of Equation 5
v 1.2	20220207	Editorial updates
v 1.1	20220120	Editorial updates, added chapters
v 1.0	20220218	Initial version

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1 Abbreviations

Table 1. Abbreviations

Acronym	Description
AES	Advanced Encryption Standard
AID	Application IDentifier
APDU	Application Protocol Data Unit
C-APDU	Command APDU
CMAC	MAC according to NIST Special Publication 800-38B
CRC	Cyclic Redundancy Check
CS	Capacitive sensing
CTT	Capacitive Tag Tamper (StatusDetect)
FNMR	False Non-Match rate. Proportion of genuine attempts that are falsely declared not to match a template of the same object.
FMR	False Match Rate. Proportion of impostor attempts that are falsely declared to match a template of another object.
IC	Integrated Circuit
KDF	Key derivation function
LSB	Lowest Significant Byte
LSb	Lowest Significant bit
MAC	Message Authentication Code
NDEF	NFC Data Exchange Format
NFC	Near Field Communication
NVM	Non-volatile memory
PCD	Proximity Coupling Device
PICC	Proximity Integrated Circuit Card
PRF	Pseudo Random Function
R-APDU	Response APDU (received from PICC)
UID	Unique IDentifier
URI	Uniform Resource Identifier
URL	Uniform Resource Locator

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2 About this document

This document addresses developers who are developing applications based on NTAG 22x DNA StatusDetect products.

This application note is a supplementary document for implementations using the mentioned products. It shall be used in addition to NTAG 22x DNA StatusDetect data sheets [1], [2], [3] or [4]. The best use of this application note is achieved by reading the mentioned data sheet in advance. This document represents numerical examples. For more information on security aspects of NTAG 22x DNA StatusDetect, refer to [6]. For more information on Antenna design, refer to [7].

Note: This application note does not replace any of the relevant functional specifications, data sheets, or design guides.

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3 Capacitor and capacitance

A simple capacitor may be defined by two electrodes configured as flat parallel plates with distance *d* and area *A* Figure 1.

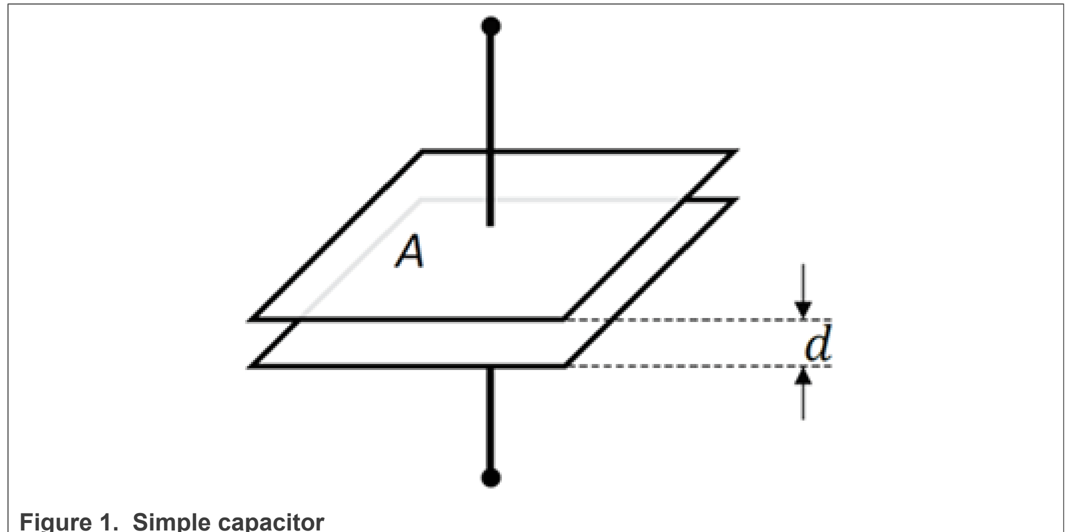

Figure 1. Simple capacitor

For distance *d* being much smaller than the plates dimensions, the capacitance of capacitor may be calculated as:

$$C = \varepsilon_0 * \varepsilon_r * \frac{A}{d} \quad (1)$$

ε_0 is the permittivity of the vacuum (ε_0 = 8.85 $*$ $10^{-12} F/m$). ε_r is the relative permittivity of the dielectric between the two electrodes. The capacitance as given by Capacitance increases with an increase of the effective area *A*. It decreases with an increase of the effective distance *d* and increases with an increase of the relative permittivity ε_r.

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4 Capacitive measuring concept in NTAG

4.1 IC connection

The IC is connected to the capacitor via DP and GND pads.

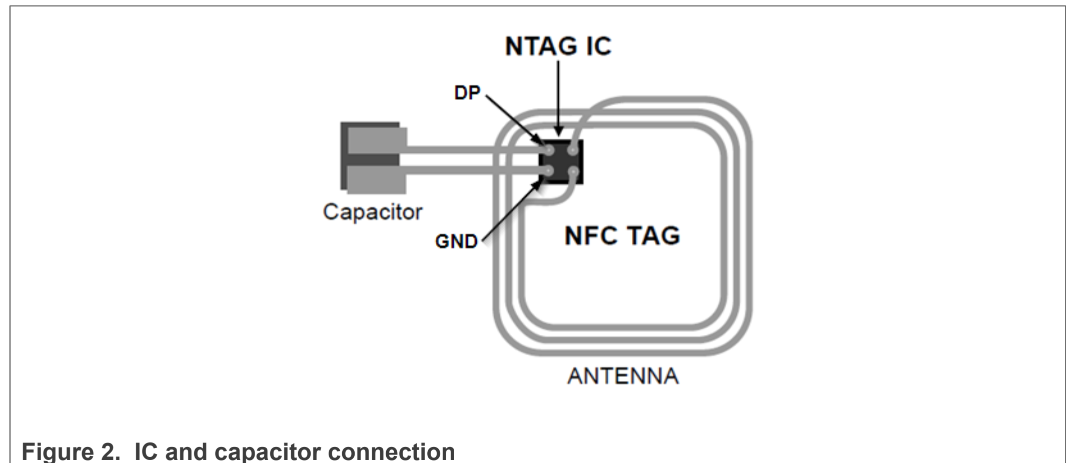

Figure 2. IC and capacitor connection

4.2 Differential measurement principle

The analog part of the Capacitive Tag Tamper (CTT) block works by comparing the slopes of 2 charged capacitors (internal and external one connected between DP and GND pads) and checking how long does it take, until certain thresholds are reached.

This approach lowers the environmental influence on the capacitive measurements. E.g., Internal capacitor will be affected by higher ambient temperature in the same range as the measured external capacitor.

- Charging time (internal counter) of internal capacitor is measured using fixed current to charge
- Charging time ***CounterValue2_ext*** of external capacitor is measured regarding to the adjustable current ***CTT_CURR_TRIM***.
- ***DifferenceMeasurement***is the time difference between the charging time of internal counter and the charging time ***CounterVaue2_ext*** of the external capacitor
  - A positive value of ***DifferenceMeasurement*** (DifferenceMeasurementB on Figure 3) means that the adjusted current is too small → for the next calibration round current (***CTT_CURR_TRIM***) shall be increased.
  - A negative value of ***DifferenceMeasurement*** (DifferenceMeasurementA on Figure 3) means that the adjusted current is too high → for the next calibration round current (***CTT_CURR_TRIM***) shall be decreased.
- Smallest ***DifferenceMeasurement*** (less than 25d) value shall be stored into NTAG's ***CTT_DIFF_CAL*** register.
- With ***MEAS_DBL_Range***, it is possible to do a measurement of the external capacitor using double range (less accuracy) if this external capacitor exceeds 11 pF.
- With ***CTT_CFILT*** , it is possible to enable an internal ballast capacitor inside NTAG (0 - 3 pF) if the external capacitance is too low as defined in [3].

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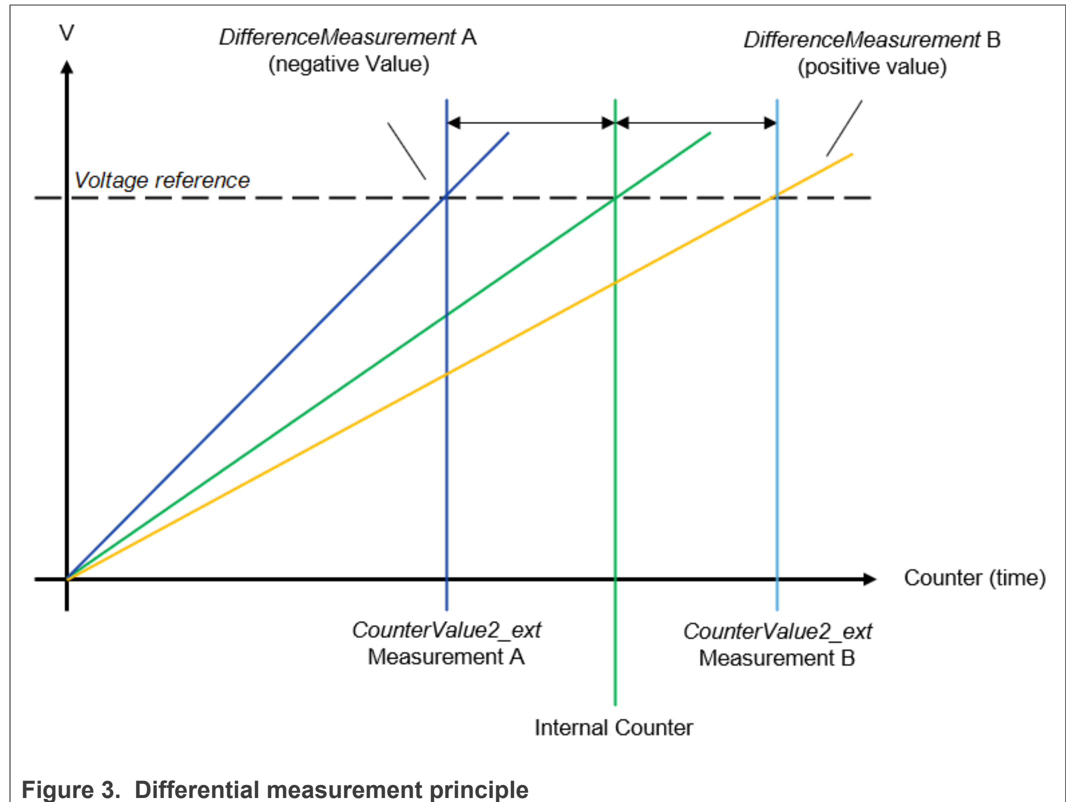

Figure 3. Differential measurement principle

4.3 CTT parameters read out

The Tag Tamper status (parameters) can be read from the Tag and later interpreted by the PCD side by:

- READ_TT_STATUS command or
- ASCII mirror feature including the Tag Tamper status [ASCII mirror described in [5]]

4.4 Capacitive StatusDetect (Tag Tamper) mode

The Capacitive Tag Tamper status is measured at each power-up of the IC. If permanent storage is enabled with the STORE_TT_STATUS bit, the status is permanently unchangeable stored as tampered in EEPROM in case the difference between the measured capacitor value and the reference value exceeds the defined limits. The limits to detect a tamper event in the capacity tag tamper mode are defined with the upper limit in byte CTT_UPPER_LIMIT and the lower limit in byte CTT_LOWER_LIMIT.

To measure the external capacitor connected to DP and GND, the external capacitor is charged with the measurement current. In parallel, an internal capacitor is charged with a fixed current. In order to achieve the highest accuracy the charging time of the internal and external capacitors should be in a similar range. This is done by optimizing the measurement current during calibration in the Capacitive Tag Tamper mode or by choosing the optimum value based on the expected capacitor value in the capacitive sensor mode.

The charging times are measured with counters (10 bit).

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The Capacitive Tag Tamper calibration is necessary for the initialization of the Capacitive Tag Tamper functionality during production in the final application. Calibration delivers a reference result which shall be stored in the EEPROM of NTAG. This reference result is used for detection of a Tag Tamper event at the startup and NTAG can store this information permanently if the STORE_TT_STATUS bit is enabled.

4.4.1 Calibration

Each capacitive tag tamper final product must be calibrated.

Methodology of calibration is to find adjustable current ***CTT_CURR_TRIM*** (most optimal > 15d, to minimize the influence of leakage on measurement) giving ***DifferenceMeasurement*** less than 25d. The goal of the calibration is to keep ***DifferenceMeasurement*** small as possible.

4.4.2 Calibration steps detailed

For the capacitive tag tamper calibration, the following procedure must be executed:

1. Switch to Capacitive Tag Tamper mode (RTT_CTT_SEL bit is set to 1).
2. Write zero value into CTT_DIFF_CALIBRATION byte and STORE_TT_STATUS (default value at delivery).
3. Optional: Activate Double Measurement range (MEAS_DBL_RANGE = 1) if necessary (deactivated at delivery).
4. Write CTT_CURR_ TRIM to 10000b and do the measurement (see step 5 and 6).
5. Start the measurement by switching HF power off and on again.
6. To get the CTT measurement data, Execute READ_TT_STATUS command.
7. For the most optimal current trim setting (CTT_CURR_ TRIM), one of the following shall be used:
    a. Use of the Equation 4.
    b. Successive approximation Section 4.4.4.2. The DifferenceMeasurement is providing a signed value indicating if the difference is + or -. If the DifferenceMeasurement result is negative, remove MSB from CTT_CURR_ TRIM and set next bit according to successive approximation algorithm and write the new value into CTT_CURR_ TRIM. If result is positive, keep MSB on CTT_CURR_TRIM and set the next bit according to successive approximation algorithm and write the new value into CTT_CURR_ TRIM. Redo steps 5., 6. and 7.b 5 times.
8. Write most optimal CTT_CURR_ TRIM found using one of the approaches of step 7. Write the last found DifferenceMeasurement into CTT_DIFF_CAL (important: keep polarity).
9. (Optional) Calculate the capacitance with the Equation 3
10. Write the upper limit into byte CTT_UPPER_LIMIT and the lower limit into byte CTT_LOWER_LIMIT to define the limits for a Tag Tamper event regarding final product qualification.
    - 1 counter value represents a capacitive change of (C + CTT_FILT) / CounterValue2_ext in fF
    - Set CTT_UPPER_LIMIT and CTT_LOWER_LIMIT to a value >= 250 fF + tolerance of external capacitor
11. After the calibration, it is recommended to enable the STORE_TT_STATUS and to lock the CTT calibration values with the LOCK_CTT_CFG bit.

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12. After the final IC configuration, it is recommended to lock in addition the other Tag Tamper settings with the LOCK_USR_CFG and BLOCK_LOCK_TT bit.

At each startup, the NTAG 224 DNA SD executes the capacitance measurement with the calibrated values. If the maximum difference between calibration measurement counter value and capacitive tamper measurement counter value exceeds the CTT_LOWER_LIMIT or the CTT_UPPER_LIMIT, the NTAG 224 DNA TT detects a tag tamper event.

If no tag tamper event has been detected during start-up and SHOW_ STORED_TT_STATUS is enabled:

- The READ_TT_STATUS command response with TTS bits 7-4 as 3h
- If the Tag Tamper ASCII mirror is enabled, the TTS bits 7-4 mirror byte will show 43h (ASCII "C")

Once the tag tamper event has been detected during start-up and STORE_TT_STATUS is enabled:

- NTAG 224 DNA SD stores permanently that the tag tamper event has been detected
- On a READ_TT_STATUS command, the NTAG 224 DNA SD responds with TTS bits 7-4 as Fh if SHOW_ STORED_TT_STATUS is enabled
- If the Tag Tamper ASCII mirror and SHOW_ STORED_TT_STATUS is enabled, the stored TTS mirror byte will show 4Fh (ASCII "O")

If SHOW_ ACT_TT_STATUS is enabled the actual status of the tag tamper event during start-up can be read with:

- READ_TT_STATUS command or
- ASCII mirror feature including the Tag Tamper status

If the actual Tag Tamper status is closed and SHOW_ACT_TT_STATUS is enabled:

- The READ_TT_STATUS command response with TTS bits 3-0 as 3h
- If the Tag Tamper ASCII mirror is enabled, the actual TTS mirror byte will show 43h (ASCII "C")

If the actual Tag Tamper status is OPEN:

- The READ_TT_STATUS command response with TTS bits 3-0 as Fh
- If the Tag Tamper ASCII mirror is enabled, the actual TTS mirror byte will show 4Fh (ASCII "O")

If CTT_SHOW_VALUE is enabled, the capacitance measurement parameters are mirrored by the ASCII mirror feature or can be read with the READ_TT_STATUS command.

4.4.3 Capacitance calculation formula

Current relation to capacitance:

$$C = I * \frac{\mathrm{dt}}{\mathrm{dV}} - \mathrm{CTT_FILT} \quad (2)$$

Equation to calculate capacitance:

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$$C = (0.977 \times (1 + CTT_CURR_TRIM) \times (1 + MEAS_DBL_RANGE * 1.45)) \times \frac{CounterValue2_ext \times \frac{1}{3.39}}{600} - CTT_FILT \quad (3)$$

4.4.4 Optimal current (CTT_CURR_TRIM) determination methods

4.4.4.1 Use of formula (recommended)

This method is the preferred method as it is faster than successive approximation Section 4.4.4.2, as it requires less RF communication and gives reliable results as well.

$$\mathrm{CTT_CURR_TRIM\ (optimal)} = \left(\frac{\mathrm{CounterValue2_ext} \times \mathrm{CTT_CURR_TRIM}}{\mathrm{CounterValue2_ext} - \mathrm{DifferenceMeasurement}} + \frac{\mathrm{DifferenceMeasurement}}{80} \right) \quad (4)$$

4.4.4.2 Successive approximation

Optionally the successive approximation algorithm can be implemented in software to determine most optimal CTT_CURR_TRIM.

DifferenceMeasurement is providing a signed value indicating if the difference is + or -.

- If the DifferenceMeasurement result is negative, then remove MSB from CTT_CURR_TRIM and set next bit according to successive approximation algorithm.
- If the result is positive, then keep MSB on CTT_CURR_TRIM and set the next bit according to successive approximation algorithm.

Write the new value into CTT_CURR_TRIM.

Redo these steps 5 times as CTT_CURR_TRIM is 5-bit value.

4.4.5 Upper and Lower limit

Choosing proper boundaries for final system/application is important. Section 5.4.1 offers notes on the process. On the IC level, area between Upper (CTT_UPPER_LIMIT) and Lower (CTT_LOWER_LIMIT) limit present area where IC will consider CTT measurement as CLOSED. Limits are programmed into IC's memory and are compared during start-up if External capacitor is charged within time limits (CLOSED or not OPENED).

NTAG 22x DNA StatusDetect reports CLOSED state if the following 2 conditions are met:

1. If *Difference measurement >= 0*, then
   Difference measurement <= $Tamper_Threshold_{upper}$ (CTT_UPPER_LIMIT)
2. If *Difference measurement < 0*, then
   (- Difference measurement) <= $Tamper_Threshold_{lower}$ (CTT_LOWER_LIMIT)

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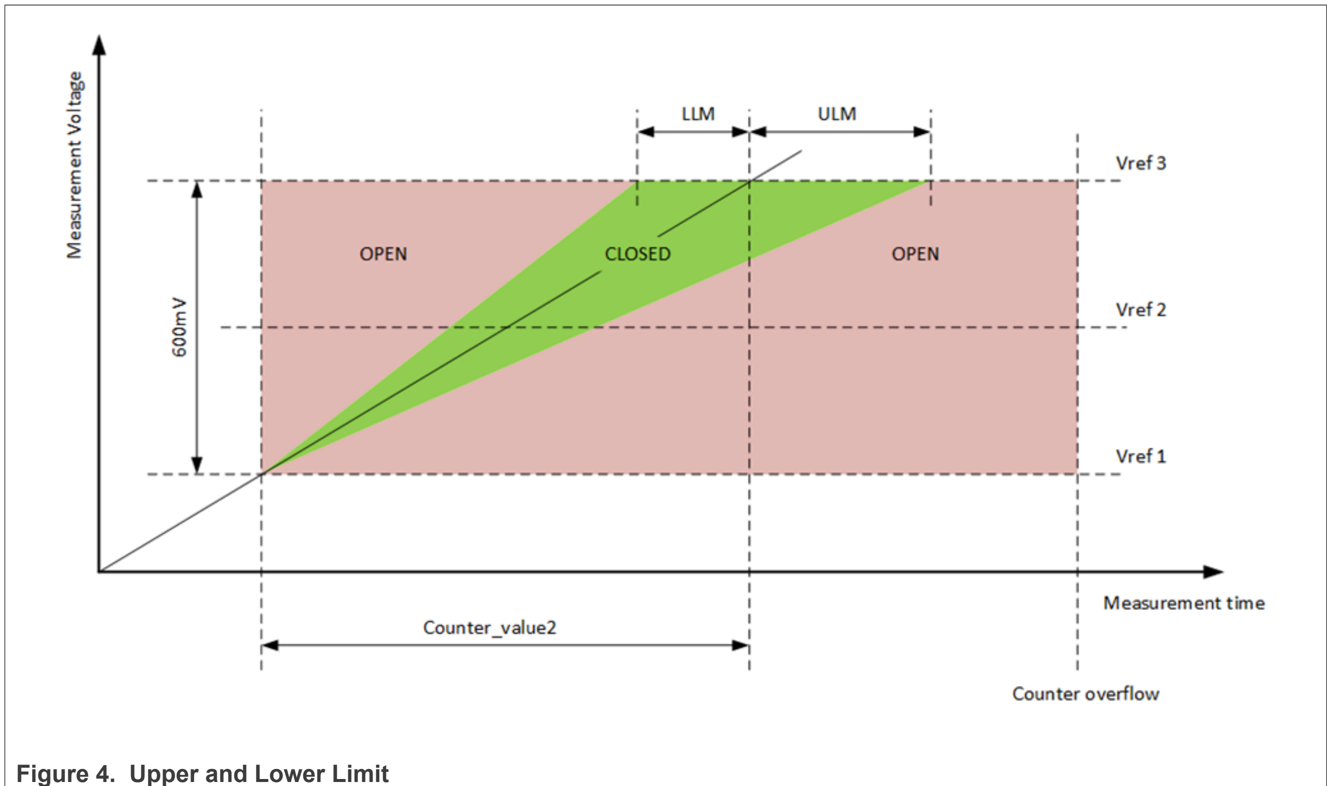

Figure 4. Upper and Lower Limit

4.4.6 Numerical example - calibration with HF ISO14443-3 reader

Note: Following example and values are only for demonstration purposes. Values, even using same capacitor values, are different from application to application.

In this example, an external capacitor of value 3.3 pF is connected between DP and GND pads of NTAG 223 DNA StatusDetect.

NTAG can measure capacitances between 0 pF - 11 pF (or 0 - 22 pF if ***MEAS_DBL_Range*** is enabled) - as referenced in [3] or [4].

4.4.6.1 Calibration with HF ISO14443-3 reader

CTT_CURR_TRIM calculated with Equation 4.

NTAG configuration: Default configuration of NTAG 224 DNA StatusDetect as per [4].

NTAG ISO state: ISO14443-3 Type A — Initialization and anti-collision done. NTAG in ACTIVE state.

Step	Command / Text		Data [HEX]
1	GET_VERSION	>	60
2	Data (Product version information)	<	0004040804000F03

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Step	Command / Text		Data [HEX]
3	0004040804000F03	=	00 Fixed Value 04 Vendor ID: NXP Semiconductors 04 Product Type: NTAG 08 Product subtype: 50 pF, TT 04 Major product version: 223 DNA Status Detect (0x05 would be 224) 00 Minor product version 0F Storage size: 144 Bytes of user memory (0x10 would mean 208 Bytes - Position of Configuration Pages changes from 29h to 39h) 03 Communication protocol type: Support ISO/IEC 14443-3 Type A
4	READ configuration page 29h	=	3029h
5	Data [CFG_B0, TT, MIRROR_PAGE, AUTH0]	<	003C003C (+ 12 bytes of 00)
6	TT = 3C	=	MEAS_DBL_RANGE = 0b CTT_CURR_TRIM = 01111b **RTT_CTT_SEL = 0b** → Resistive Tag Tamper (RTT) detection is set. Switch to CTT. Set this bit to 1b. CTT_SHOW_VALUE = 0b
7	By default Resistive Tag Tamper (RTT) detection is set. Set following: • CTT_CURR_TRIM = 10000b • CTT_RTT_CTT_SEL = 1b • CTT_SHOW_VALUE = 1b Write to Configuration page 29h	>	A2290043003C
8	ACK	<	0A
9	(Optional - as it is default) WRITE zero values to CTT_DIFF_CALIBRATION byte	>	A23900373700
10	(Optional - as it is default) WRITE zero values to STORE_TT_STATUS bit.	>	A22E00000000
11	(Optional) Activate Double Measurement range	>	A22900**B**F003C
	Calibration - Using Equation 4		
12	Start the measurement by switching HF power OFF and ON		
13	ISO14443-3 Type A — Initialization and anti-collision		(details omitted for simplicity reasons)
14	Execute READ_TT_STATUS command	>	A400
15	Data [READ_TT_STATUS response in CTT mode]	<	8088C08233

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Step	Command / Text		Data [HEX]
16	78ECC0883F	=	TT0 = 80 = b'10000000 TT1 = 88 = b'10001000 TT2 = C0 = b'11000000 TT3 = 82 = b'10000010 TT4 = 33 = b'00110011
17	78ECC0883F	=	b'10000000 10001000 11000000 10000010 00110011 CTT_CURR_TRIM = b'10000 MEAS_DBL_RANGE = b'0 CTT_CFILT = b'00 DifferenceMeasurement = b'000000100010 RFU = b'00 CounterValue2_ext = b'1000001011 TT Stored = b'0011 TT Actual = b'0011
18	CTT_DIFF_CALC	=	22 (sign bit + 7 lsb from DifferenceMeasurement)
19	Optimal CTT_CURR_TRIM (using Equation 4)	=	17.425 17d (rounded) = 11h = b'10001
20	(Optional) Calculate capacitance (for notes) using Equation 3	=	4,270 pF
21	Write to Page 39h CTT_CURR_TRIM	>	A2390047003C
22	ACK	<	0A
23	Start the measurement by switching HF power OFF and ON.		
24	Wait 5 ms.		
25	Activate ISO14443-3		
26	Execute READ_TT_STATUS command	>	A400
27	Data [READ_TT_STATUS response in CTT mode]	<	8840007E33
28	8840007E33	=	b'10001000 01000000 00000000 01111110 00110011 CTT_CURR_TRIM = b'10001 (17d) MEAS_DBL_RANGE = b'0 CTT_CFILT = b'00 DifferenceMeasurement = b'000000010000 (16d) RFU = b'00 CounterValue2_ext = b'0111111000 (504d) TT Stored = b'0011 (3h = Closed) TT Actual = b'0011 (3h = Closed)
29	Is -25 <= DifferenceMeasurement <= 25 and CTT_CURR_TRIM >= 15	=	true
30	(Optional) Calculate capacitance (for notes) using Equation 3	=	4,357 pF
31	CTT_DIFF_CAL	=	10 (sign bit + 7 lsb from DifferenceMeasurement)

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Step	Command / Text		Data [HEX]
32	Write CTT_DIFF_CAL value 10h into Page [49h]	>	A24910373700
33	ACK	<	0A

4.4.7 RFIDDiscover interface

NXP RFIDDiscover V5.0.0.0 (and greater) offers an interface to explore all features of NTAG 22x DNA StatusDetect. It is available on NXP's DocStore.

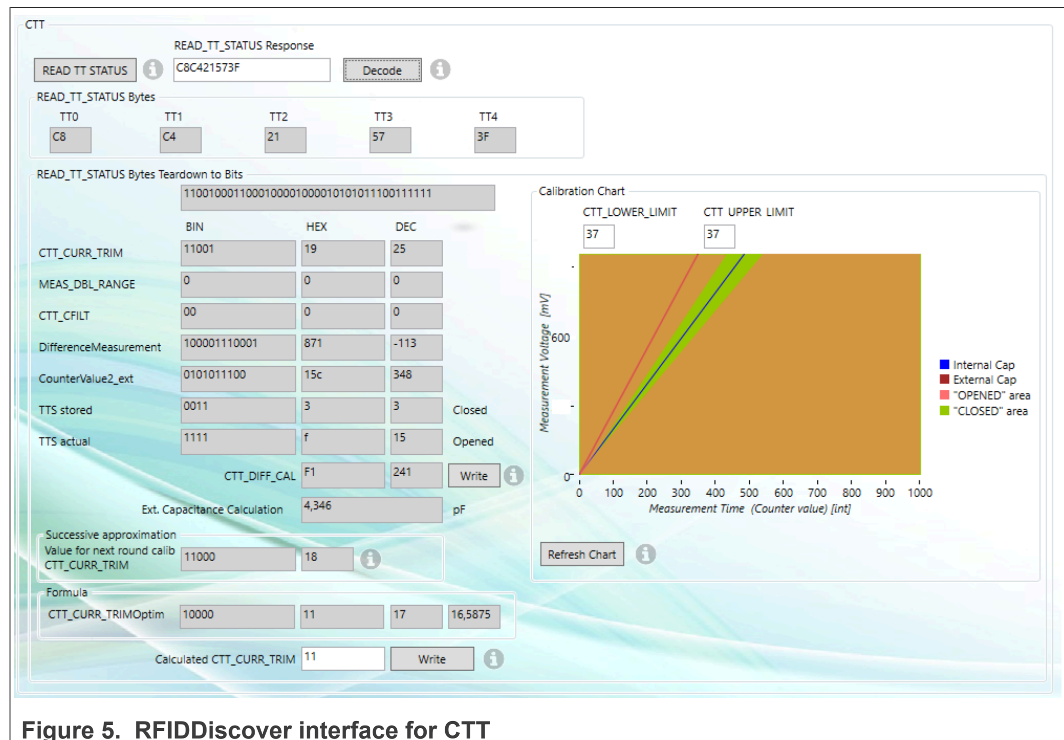

Figure 5. RFIDDiscover interface for CTT

4.5 Capacitive sensor mode

Sensing capacitance - ignore CTT_UPPER_LIMIT and CTT_LOWER_LIMIT thresholds. Check deviation from calibration value (difference measurement) and calculate capacitive change based on the difference measurement.

Sensing range is from 0 - 11 pF as per [3].

The capacitive sensor mode works similar to the Capacitive Tag Tamper mode, but in this mode the CTT_UPPER_LIMIT, CTT_LOWER_LIMIT and STORE_TT_STATUS are not required if Capacitive Tag Tamper functionality is not needed.

In the capacitive sensor mode is executing a measurement of the connected capacitance with the programmed parameters.

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4.5.1 Calibration of capacitive sensing mode

The most accurate measurement is achieved following the procedure similar to the calibration of the capacitive tag tamper by adjusting the measurement current as described in Section 4.4.2.

To calculate the difference capacitance value after calibration, data can be fetched from the tag (Section 4.3). Response from the tag can be interpreted and by use of the formula Equation 5, the difference between the calibrated and actual measurement can be detected.

4.5.2 Capacitance calculation in capacitance-sensing applications

To calculate the difference between the calibrated and actual measurement use the following formula. Note that *DifferenceMeasurement* replaces *CounterValue2_ext* from formula Equation 3.

$$Cdiff = (0.977 \times (1 + CTT_CURR_TRIM) \times (1 + MEAS_DBL_RANGE * 1.45)) \times \frac{\mathrm{DifferenceMeasurement} \times \frac{1}{3.39}}{600} \quad (5)$$

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5 Capacitance sensing principles

Final Capacitive sensing or Tag Tamper application design must determine which factors will influence the change in capacitance.

$$C = \varepsilon * \frac{A}{d} \quad (6)$$

Considering simplified capacitance formula [Equation 6], following changes can be sensed by capacitance measurement:

- Change the distance between the electrodes (change of *d*) Figure 6
- Changing the effective area of the electrodes (change of *A*) Figure 7
- Change of dielectric between the electrodes (change of ε) Figure 8. Dielectric is also a function of temperature, therefore temperature may also be measured via permittivity change

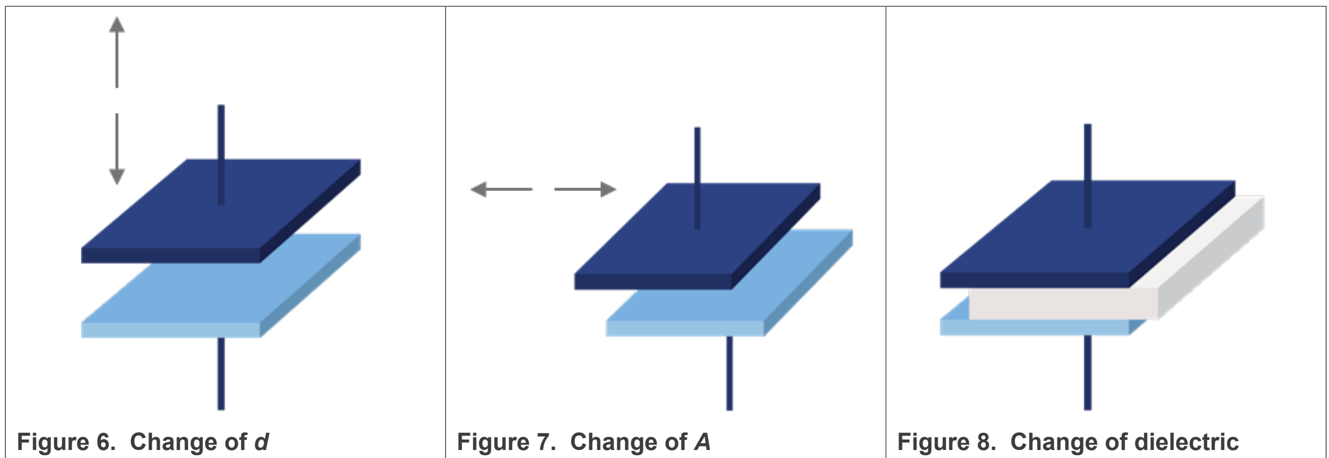

Figure 6. Change of *d*

Figure 7. Change of *A*

Figure 8. Change of dielectric

5.1 Principles explained

5.1.1 Change of distance between capacitance electrodes

As an example, the measurement capacitor is configured as illustrated in Figure 9. Two electrodes configured as flat parallel plates of area $A1$, spaced by a gap g are fully covered by a flat metal plate of area $A2$ at distance d. The capacitance structure can be simplified as illustrated by the right side Figure 9, forming two series connected capacitors. The middle plate can be neglected as it is at constant distance to bottom and top plate.

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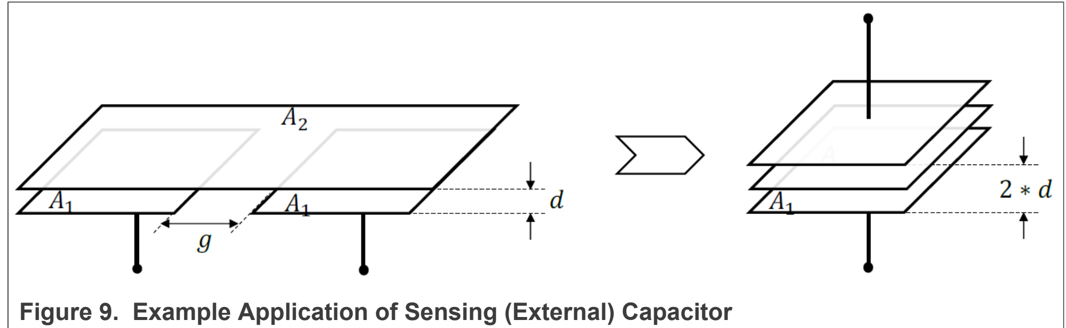

Figure 9. Example Application of Sensing (External) Capacitor

For distance d being smaller than the plates dimensions, gap g being much larger than distance d, and area A_2 circulating the two electrode-plates of area A_1, the capacitance of that capacitor may be calculated as

$$C = \varepsilon_0 * \varepsilon_r * \frac{A}{2 * d} \quad (7)$$

For example, application the distance d between the plates of area A_1 and the opposing plate of area A_2 varies and shall be calculated from the capacitance that develops between the two electrodes. The distance d may be calculated as

$$d = \varepsilon_0 * \varepsilon_r * \frac{A}{2 * C} \quad (8)$$

In a practical implementation, the two electrodes of area A_1 may be covered by an insulating layer of thickness d_1 and of a material having a relative permittivity of εr_1, and air having a relative permittivity of εr_2 may fill the distance $2 * d_2$ between the insulating material and the opposing plate of area A_2 as illustrated by Figure 10.

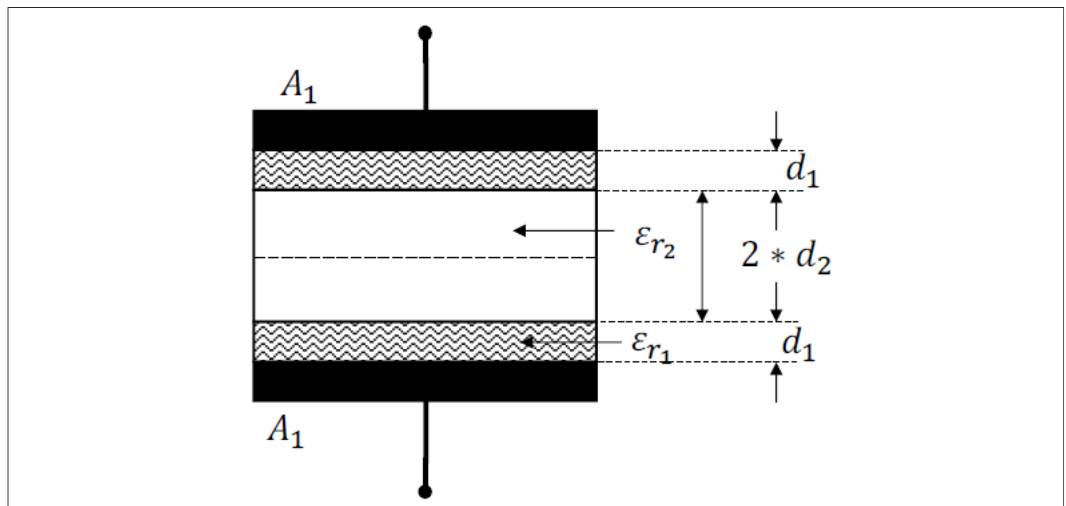

Figure 10. Sensor Capacitance Stack with Insulator

With stacked dielectrics, capacitance calculation may become quite complex, therefore an approach is applied to correct the distances d_1 and d_2 for vacuum by applying the related relative permittivity εr_1 and εr_2, yielding the corrected distances d'_1 and d'_2.

A layer of a material having a relative permittivity εr having a thickness d may be corrected for the relative permittivity of vacuum yielding.

$$d' = \frac{d}{\varepsilon r} \quad (9)$$

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The capacitance of the capacitor may therefore be calculated as

$$d' = \frac{d}{\varepsilon_r} \quad (10)$$

$$d_1' = \frac{d_1}{\varepsilon r_1} \quad (11)$$

$$d_2' = \frac{d_2}{\varepsilon r_2} \quad (12)$$

$$C = \varepsilon_0 * \frac{A}{2*(d_1' + d_2')} \quad (13)$$

The capacitor Figure 10 with corrected layer thicknesses is illustrated by Figure 11.

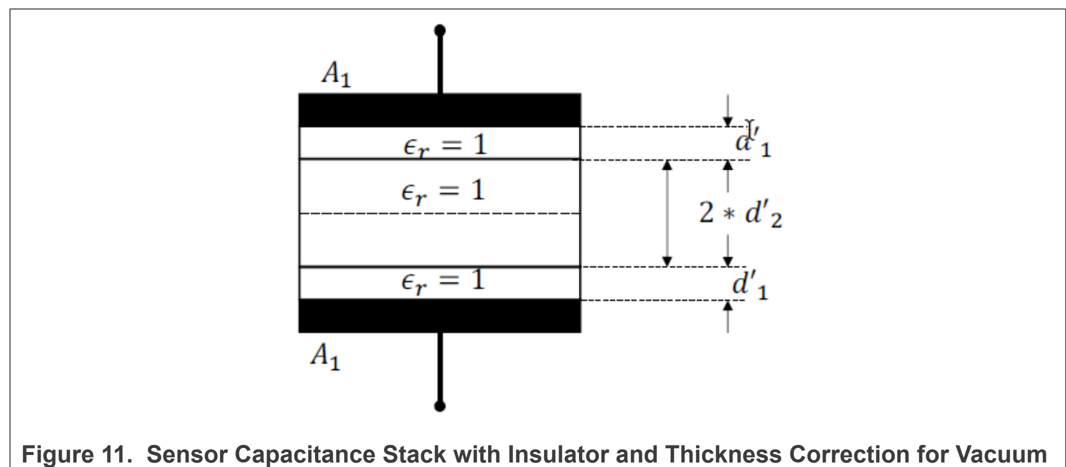

Figure 11. Sensor Capacitance Stack with Insulator and Thickness Correction for Vacuum

In the main application of CTT, distance $d2$ must be measured, it is calculated by application as Equation 17

$$d_2' + d_1' = \varepsilon_0 * \frac{A}{2*C} \quad (14)$$

$$d_2' = \varepsilon_0 * \frac{A}{2*C} - d_1' \quad (15)$$

$$d_2 = \left(\varepsilon_0 * \frac{A}{2*C} - d_1' \right) * \varepsilon r_2 \quad (16)$$

$$d_2 = \left(\varepsilon_0 * \frac{A}{2*C} - d_1 * \varepsilon r_1 \right) * \varepsilon r_2 \quad (17)$$

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5.2 Error sources

When measuring the distance $d2$, errors may affect the measurement result. These errors may e.g. have a systematic, an environmental or an algorithmic background. Examples for such errors are listed by Table 2.

Table 2. Error types

Error origin	Error	Affects	Impact
Device	Measurement Resolution	Offset Error	Significant
	Reference sources	Range Error	Medium
	Supply Ripple	Random Error	Small
	Device Spread	Random Error	Small
Environment	Humidity	Range Error	Significant
	Temperature	Range Error	Medium
	Pressure	Range Error	Small
Algorithmic	Computation Resolution	Offset Error	Small

Range and Offset errors may be reduced by suitable calibration means, while random errors are difficult to compensate – oversampling would be a suitable counter measure. If the remaining errors become too large, required error rates such as an FNMR of 0.1 % may not be supported.

5.3 Error-Rate evaluation

Open/closed status detect state must be identified by means of an air capacitor at minimal error rates.

The decision system of CTT has been analyzed for error rates that must be considered during specification and testing. Evaluation is needed to investigate significant error rates that apply to CTT, to analyze their impact and propose test methods that are suited to support the error rates claimed by the product specification.

The error rates FNMR (False Non-Match Rate) and FMR (False Match Rate) have been defined for CTT. The FNMR indicates the proportion of genuine products that are falsely identified as fake products, while the FMR indicates the proportion of fake products that are not correctly identified as fake products.

The error rates CTT shall be targeted at FNMR=FMR=0.1 %.

The FMR of 0.1 % represents a tight target, that may require additional design effort to cope with the expected device/system/application/environmental errors.

The FMR is a performance parameter that can easily be observed by done tests.

Due to the small FMR, ≈3000 tests must be performed and shall not produce any errors (aka rule of three) to support the claim rate of 95 %. To confirm the claim of <=1 %, 3000 samples shall be taken from a batch. If there are no FNMR errors detected, the batch can be released. The batch shall be dropped, if there is at least one error [8].

It is proposed, to implement an FMR line-test at the production line, to verify that the CTT tag has been applied and working correctly.

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5.4 Decision system

5.4.1 Confidence Interval Checking

CTT can be treated as a capacitance measurement system. From an application perspective, it is obliged to provide a clear yes/no (genuine/fake) decision without any intermediated states. It is expected to have a reliable information on detecting counterfeited products, injected into genuine sales / logistic channels. Anyway, NTAG's CTT application can only provide probabilities for yes and no. These probabilities may be overlapping.

The decision system as integrated in CTT is illustrated by Figure 12. A suitable capacitive sensor is evaluated by a Capacitance-to-Digital Conversion Unit, which provides a digital representation of the sensor’s capacitance. The digital representation is post-processed to prepare a representation that can be range-compared against stored reference capacitance values defining the lower and/or upper boundary of a confidence interval. The confidence interval boundaries may be set during product configuration or may be enrolled empirically, either during chip configuration or during tag manufacturing.

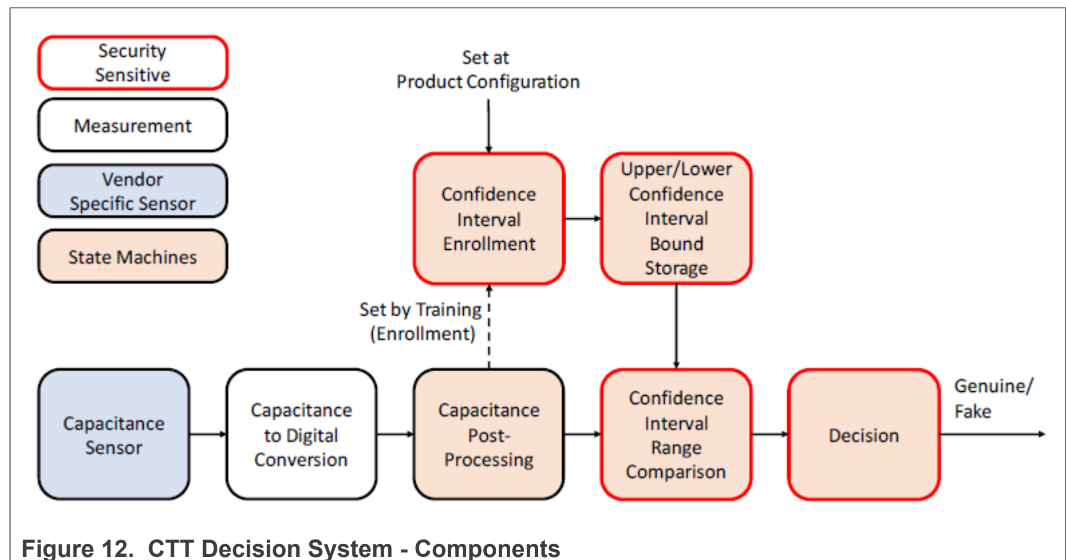

Figure 12. CTT Decision System - Components

Specifying parameters of such a decision system requires a corresponding measurement method of verifying that specification parameter. Such measurement may never provide the same result; therefore, a series of measurements may provide e.g. normal-distributed capacitance measurement results or binomial-distributed decision results. If a confidence level is defined, the corresponding confidence interval can be determined. For e.g. a confidence level of 95 %, a confidence interval of $\pm 1.96\sigma$ around the expected mean can be determined. Therefore, it is a good approach to define the upper and/or lower bound of the confidence interval rather than checking for just a single value. By narrowing or extending the confidence interval, the resulting error rates can be managed.

5.4.2 Environmental Impact on Capacitance Measurement

A maximal error rate claimed by a device specification must be verified by a suitable test method. Field tests shall provide a solid statistical base to measure the error rates. It is therefore required, to define test methods that model the field application including e.g. environmental or application-related conditions as good as possible. A challenge of

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low error rates is the large number of individual Bernoulli Experiments that need to be performed to verify a claimed error rate. One of known method is Zero Defect Analysis, where a certain failure rate may be supported by a limited number of tests.

Next known method is the "rule-of-3". This method requires to confirm a claimed error rate by 3*1/rate tests with positive result, means: if 100 claimed devices are with no error, 300 devices must be tested showing no error, to achieve 95 % confidence.

The multiplier 3 is calculated by -ln(1-0.95) for 95 % confidence interval. 95 % confidence interval means that 95 % of all tests with a sample size of 3*1/rate confirms the claimed error rate [8].

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6 Frequently asked questions

1. Why is the calibration needed?
   - Since a certain capacitive range is supported, the trimming routine allows configuring each IC for optimum performance. The smaller the initial measurement difference is, the less is the variation over ambient conditions in the field (temperature, humidity, aging).
   - In the calibration, the CTT_CURR_TRIM value is changed until the difference measurement is minimized (< 25d). Once this is done, the difference measurement will be stored as the calibration difference and can then be included in the calculation of the measurement difference.
2. Why do we need to calibrate each sample?
   - Since each IC and each attached external capacitor have manufacturing tolerances, it is important to trim each sample individually. This gives optimum performance.
   - If the capacitor value is < 6 pF and therefore can be trimmed without using double range (CTT_CURR_TRIM < 31)
3. How can we simplify the calibration?
   - The calibration can be performed using a successive approximation method in Section 4.4.4.2. With 5 trim bits, the optimum calibration value can be found with 5 measurements.
   - Faster method is using the formula in Section 4.4.4.1, which calculates optimal current trim based on one measurement.
4. Why do some tags give open when they are closed?
   - The decision if a tag is considered “open” or “closed” depends on the configuration. In order to avoid this problem, the CTT_UPPER_LIMIT and the CTT_LOWER_LIMIT must be set correctly, so that in physically OPEN state, the absolute of the DM (positive value) is more than the CTT_LOWER_LIMIT (CTT_UPPER_LIMIT can be set symmetrically) and in physically CLOSED state the absolute of the DM is always less than the CTT_LOWER_LIMIT (again CTT_UPPER_LIMIT can be set symmetrically).
   - To choose the correct value, a wide range of samples need to be investigated to see what the tolerances are and if there is sufficient difference in the DM value in physically OPEN and CLOSED state.
   - Use higher number of samples to get better statistical results.

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7 References

[1] Product data sheet - NTAG 223 DNA (NT2H2331G0) - NFC T2T compliant IC

[2] Product data sheet - NTAG 224 DNA (NT2H2421G0) - NFC T2T compliant IC

[3] Product data sheet - NTAG 223 DNA StatusDetect (NT2H2331S0) - NFC T2T compliant IC with StatusDetect feature

[4] Product data sheet - NTAG 224 DNA StatusDetect (NT2H2421S0) - NFC T2T compliant IC with StatusDetect feature

[5] Application note - AN12998 NTAG 22x DNA (StatusDetect) - Features and hints

[6] NTAG 22x DNA StatusDetect Information on Guidance and Operation, doc.no. 7088xx[1]

[7] Application note - AN11276 NTAG Antenna Design Guide, Rev. 1.8, doc.no. 2421xx

[8] Best practices in Testing and Reporting Performance of Biometric Devices, version 2.01, A.J. Mansfield, J.L. Wayman, National Physical Laboratory, Queens Road, Teddington, Middlesex

1 xx … document version number

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