

AN11755

PN7150 Antenna Design and Matching Guide

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Application note
COMPANY PUBLIC

Document information

Info	Content
Keywords	PN7150, NFC, Antenna Design, Antenna matching/tuning
Abstract	<p>This application note is intended to provide some guidelines regarding the way to design an NFC antenna for the PN7150 chip. It also provides guidelines on how to properly match this antenna to PN7150.</p> <p>Standalone antenna performances evaluation and final RF system validation (PN7150 + tuning/matching network + NFC antenna within its final environment) are also covered by this document.</p>



Revision history

Rev	Date	Description
1.7	20190710	<ul style="list-style-type: none">Fixed typo errorFixed error in register default valuesRemoved useless register definition
1.6	20181117	<ul style="list-style-type: none">Fixed error in register default valuesAdded description of registers
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1.2	20160706	<ul style="list-style-type: none">Fixed CLIF_ANA_CLK_MAN_REG bits description error and added register default value
1.1	20160523	<ul style="list-style-type: none">Added note about TX/RX connection recommendationSecurity status changed into "COMPANY PUBLIC"
1.0	20151123	First official release of the document

Contact information

For additional information, please visit: <http://www.nxp.com>

1. Introduction

The PN7150 is a highly integrated NFC transceiver IC for contactless communication at 13.56MHz. This transceiver IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

It can operate both in reader mode and in card mode.

The PN7150 is intended to be connected to an external coil antenna through a specific matching/tuning network.

The purpose of this document is first to provide some guidelines regarding the design of the NFC antenna to be connected to the PN7150.

It then depicts a measurement method in order to evaluate the performances of the antenna prior to connecting it to the NXP NFC chip.

The next chapter explains how to determine the matching network to be placed between a given antenna and the PN7150 (based on the antenna electrical equivalent circuit)

Then, an RF performance validation procedure is proposed.

Finally, an example of PN7150 antenna and tuning design is given as reference.

In this document the term „MIFARE card“ refers to a contactless card using an IC out of the MIFARE Classic, MIFARE Ultralight or MIFARE DESFire product family.

2. Antenna Design

Some of the design rules are very common for NXP NFC designs, i.e. they depend neither on the used standard (ISO, NFC or EMVCo) nor on the NXP Reader IC but rather on physical or technical basics.

2.1 Standard antenna design

PN7150 can be connected to a standard antenna commonly used on the market today. Those antennas are typically made of a spiral loop (*single loop antenna*). The outline dimensions, the number of turns, the copper track thickness, width and spacing define the antenna characteristics (inductance value and characteristics i.e. serial resistance, parallel capacitance). Typically, we recommend a 40 mm x 40 mm antenna for PN7150 applications.

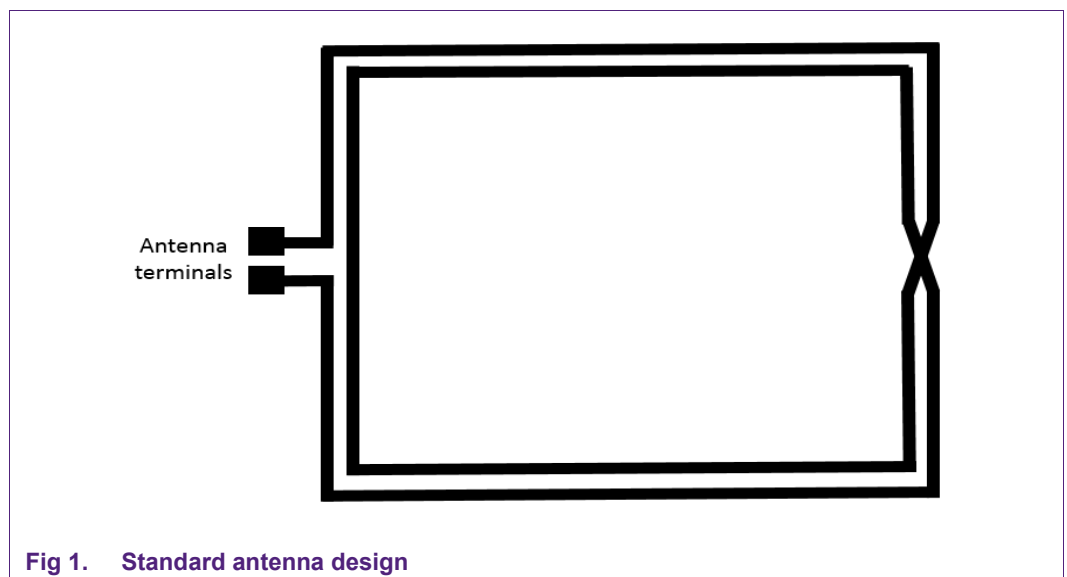


Fig 1. Standard antenna design

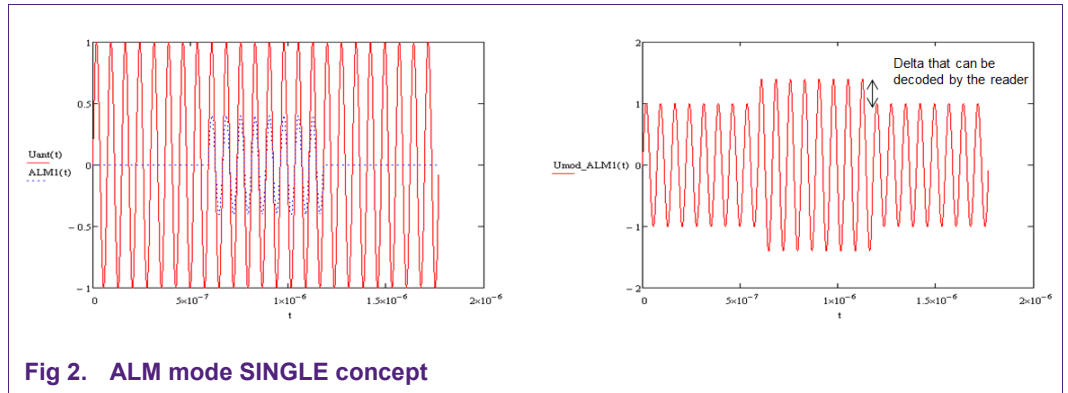
2.2 Single loop antenna dedicated for Active Load Modulation

PN7150 was designed for Active Load Modulation (ALM) concept. ALM provides high performances and significant margins to NFC standard criteria. It also allows the use of smaller antenna.

In CARD mode, PN7150 provides 2 different modes to generate LMA respectively mode 1 (SINGLE), mode 2 (DUAL). These 2 modes can be set by software.

The LMA is doubled by passing from mode 1 to mode 2.

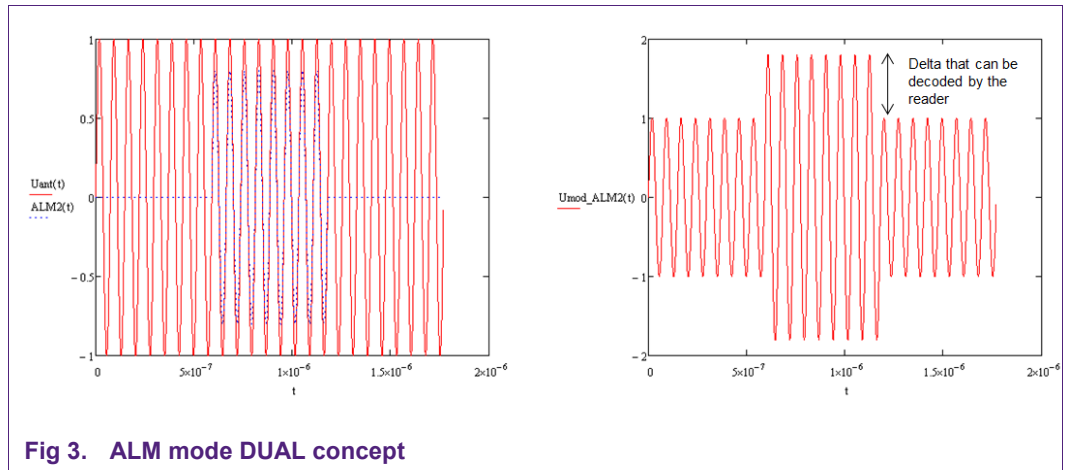
ALM Mode (SINGLE):



On the left graph the red 13.56MHz signal shows the voltage at the NFC antenna which is induced by the reader field, the blue curve shows the modulation pattern. This modulation pattern is generated by actively driving 13.56MHz with TX1 or TX2 while the other TX pin (TX2 or TX1) is kept silent.

On the right we can see the modulated reader field.

ALM Mode (DUAL):



In this mode the modulation pattern is generated by actively driving 13.56MHz with TX1 and TX2. The modulation depth observed is twice the modulation depth of mode 1.

2.2.1 Single Loop ALM Antenna

In CARD mode, the Single Loop Antenna is simultaneously used for receiving the signal from the reader, synchronizing to it (clock recovery), and generating the Load modulation back to the reader. To prevent from potential phase shift due to the superimposing of the incoming signal and the transmitted, the clock recovery is done before the data exchange (i.e. before the modulated signal is transmitted) and is frozen during the transmission.

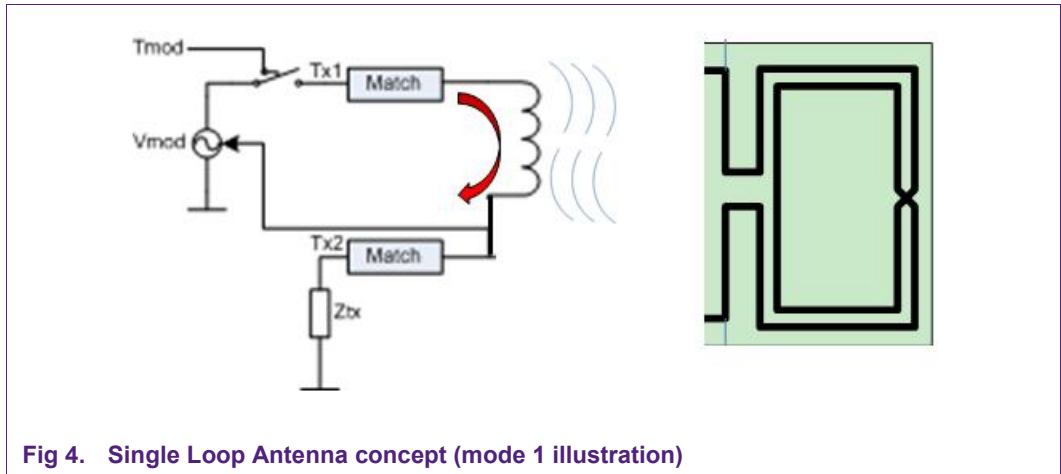


Fig 4. Single Loop Antenna concept (mode 1 illustration)

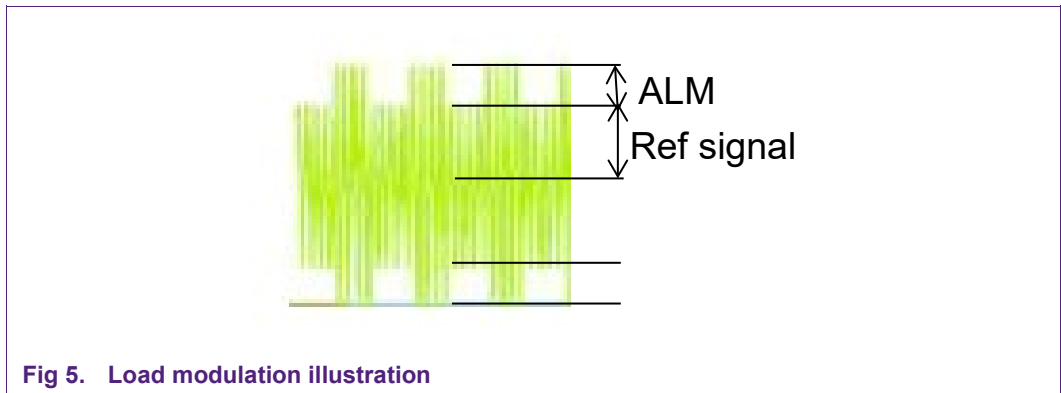


Fig 5. Load modulation illustration

The phase shift error can be defined as follow:

- 1- The Static phase shift error is the one that can be observed after having defined the optimized HW tuning and phase clock register setting. This error is almost stable vs. the field strength of the reader, when coupling factor with reader can change it. It can be considered as similar for dual loop or single loop antenna. This phase clock error is observed on sub modulated carrier.
- 2- The Dynamic phase shift error is coming from ALM signal generation by addition on both signals. This error is maximum for low field strength (high distance), when ALM level is comparable to reader field strength. This error is affecting the 13.56 MHz carrier.

On Fig 6 below LMA result examples are shown for Upper Side Band and Lower Side Band in the 2 modes available for PN7150 (respectively mode 1, mode 2).

In order to minimize the phase error, it is necessary to limit the level of the load modulation amplitude (LMA) and to adjust the balance of the Side Bands when the field strength is low.

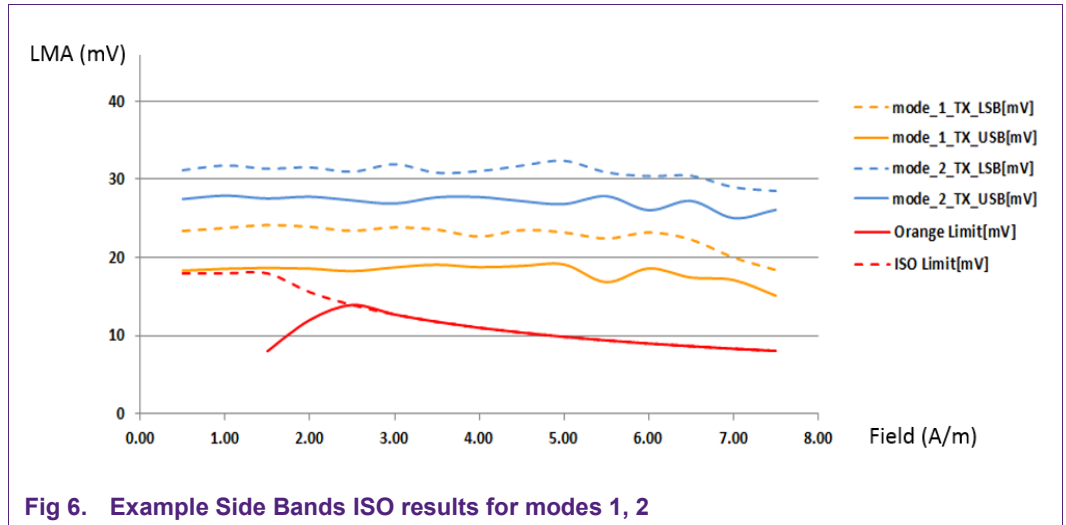


Fig 6. Example Side Bands ISO results for modes 1, 2

This can be done by optimizing the phase setting in the following conditions:

- Use reader with low coupling factor (ISO test bench or Pegoda reader as example). In this condition, the best setting is the one(s) that is providing:
 - o The minimum field strength response for ISO test bench (<1A/m - 0.5 A/m typical)
 - o The maximum communication distance with Pegoda reader (>5cm)
- Use EMVCo test bench where Load Modulation Amplitude is tested at different distance and position:
 - o This test should confirm the best setting, taking into account coupling factor impact:
 - Optimized setting should provide full passed EMVCo test.
 - In this condition, and depending on the HW tuning, it can happen that min field strength (and then communication distance) is not the optimum, but final performance should be still under the limit (<1 A/m)

In these conditions, Interoperability with various readers should be optimum.

2.3 Shielding and environment impact

The PN7150 and the associated NFC antenna are intended to be integrated into a system.

Those devices are composed of metallic parts such as the battery, the PCB, electronic components and even sometimes the chassis.

If metal is placed close to the NFC antenna the alternating magnetic field generates some eddy currents in the metal.

These eddy currents create a magnetic field in opposite direction; it absorbs power, and leads to detuning of the antenna due to a decreased inductance and quality factor.

Therefore, for proper operation in close metallic environment, it is necessary to shield the antenna with a ferrite sheet.

The following figures are intended to highlight this phenomenon based on antenna field distribution simulation results. In order to simplify the simulation, the below results are based on a circular antenna with a radius of 7.5 cm with 1 turn and a copper wire of 1mm thickness.

The right part shows the field distribution and the left part shows the magnitude of the field strength H over the distance d .

The minimal field strength of $H_{MIN} = 1.5 \text{ A/m}$ defined by ISO/IEC 14443 is marked with dotted vertical line.

Fig 7 shows the field distribution around the antenna wire in an ideal environment without any metal near the antenna.

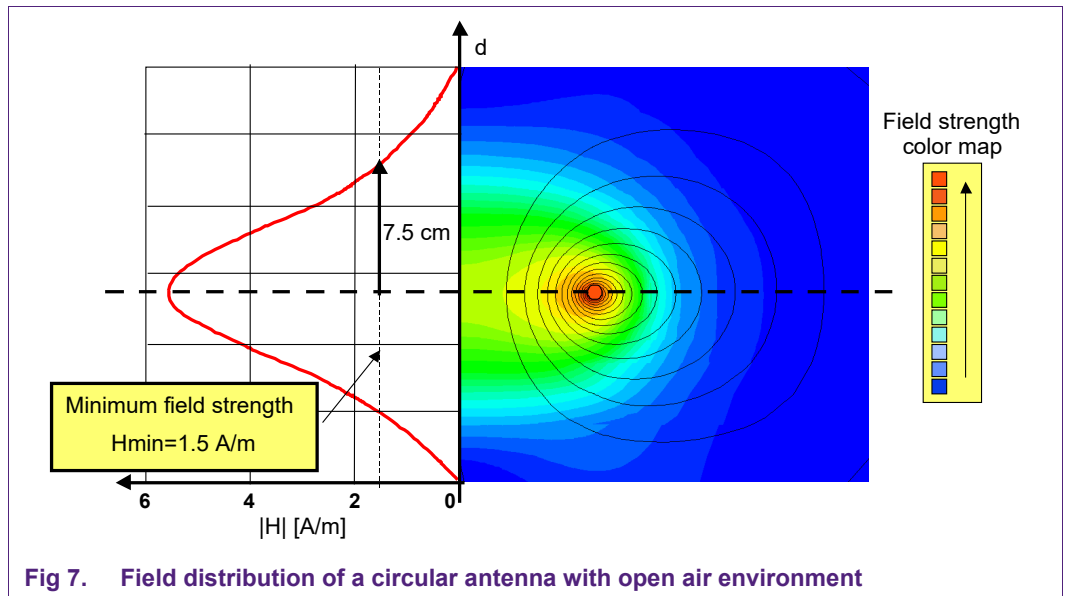


Fig 8 shows the field distribution of the same antenna but with a metal plane near to it. The magnitude of the field strength has significantly decreased compared to the open air case which leads to a decreased operating distance.

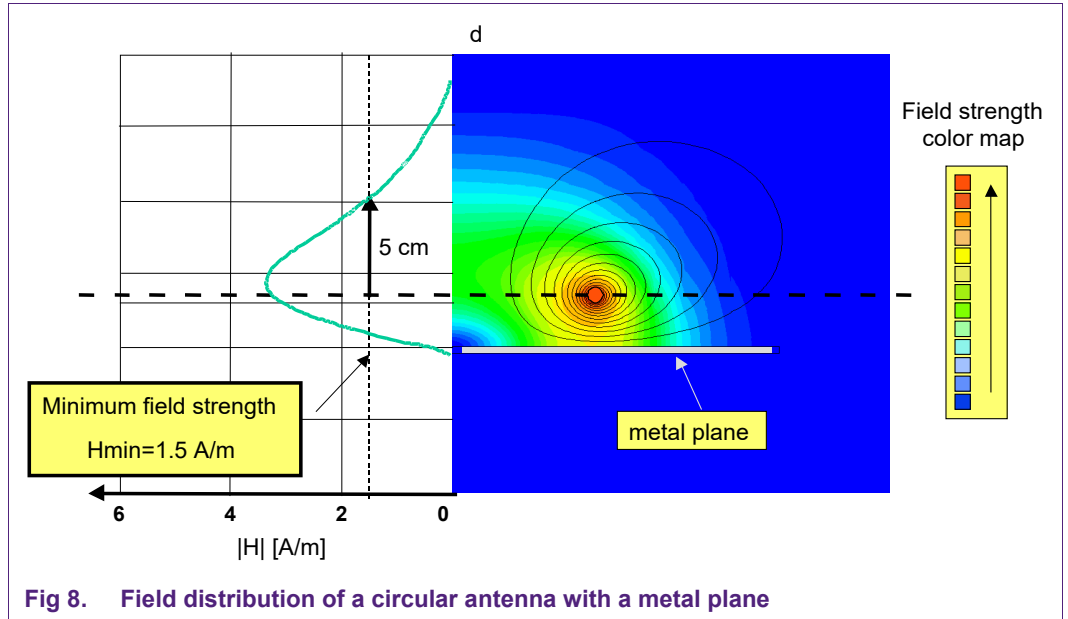
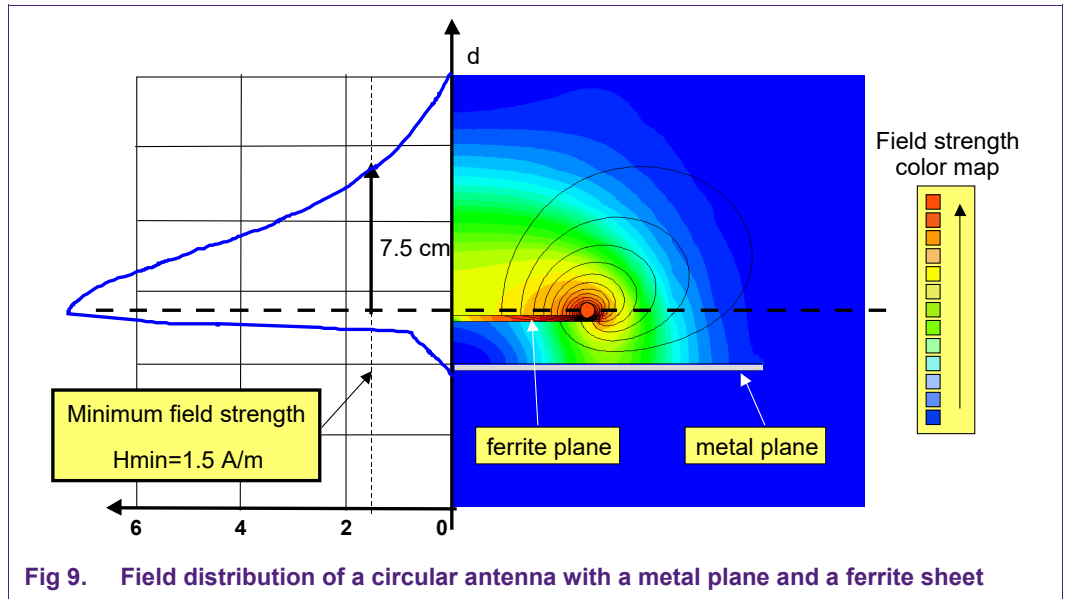


Fig 9 shows the effect of adding a ferrite plane ($\mu_R=40$) between the metal plane and the antenna coil itself. The field distribution is still modified but the operating distance recovers its original open air level.



The simulation shows that the use of a ferrite reduces the generated eddy currents in a metal plane. The ferrite sheet changes the antenna environment characteristics, which results in a fixed detuning of the antenna itself. This shielding will significantly impact the antenna electrical equivalent model so it is key that when doing PN7150 tuning/matching network calculation, the antenna model is measured with the ferrite already in place (when applicable).

2.3.1 Ferrite shielding recommendation

In order to reach a proper shielding, the ferrite sheet must at least fully cover the antenna surface. It is even needed to have an overlay but not too much because otherwise it would tend to reduce the stray field strength. This trade-off is illustrated by the picture below:

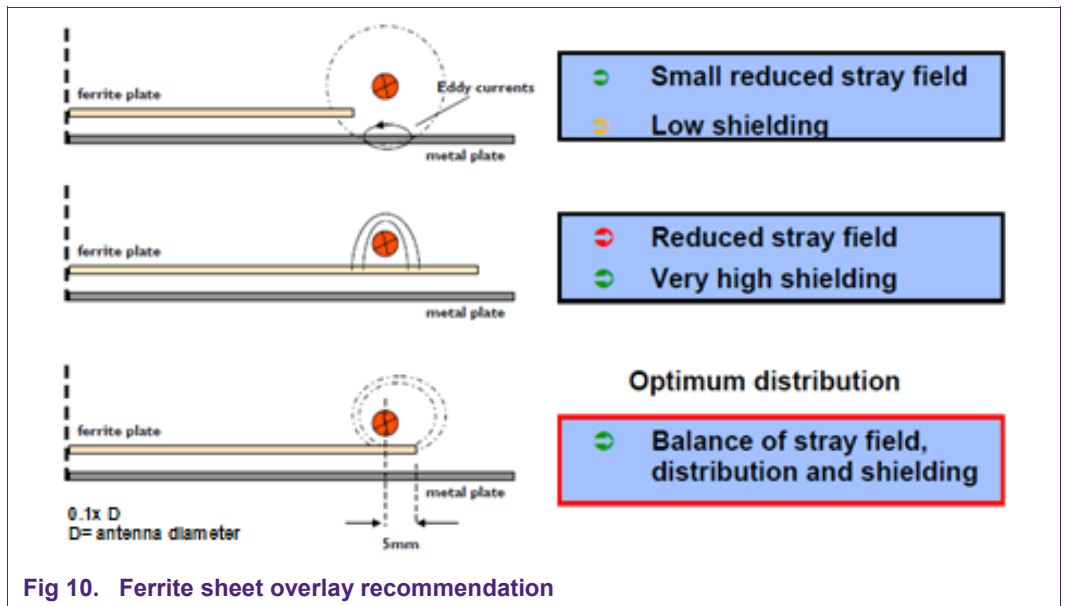


Fig 10. Ferrite sheet overlay recommendation

The Ferrite quality is also a key parameter which needs to be taken into account to assess the effectiveness of the shielding. A high relative permeability (μ_r) is recommended because it allows to achieve a good shielding with a lower ferrite sheet thickness. The material has to be specified for a high magnetic permeability in the frequency range that is involved in NFC operation, i.e. 13.56MHz. The relative magnetic permeability of a material is made of two parts:

- μ_r' is the real part of relative permeability ($\mu_r' > 40$ at 13.56MHz)
- μ_r'' is the imaginary part it reflects the magnetic losses in the material (μ_r'' as small as possible).
- At 13.56MHz we recommend $\mu_r''/\mu_r' < 0.1$

Please note that the level of shielding not only depends on the material used but also on the thickness of the ferrite sheet. For a given permeability, the thickest sheet provides the strongest shielding.

3. PN7150 Antenna matching

3.1 Antenna matching circuit

On this chapter we will show the different blocks in order to do the antenna matching. Below diagram depicts typical matching circuit related to PN7150 design.

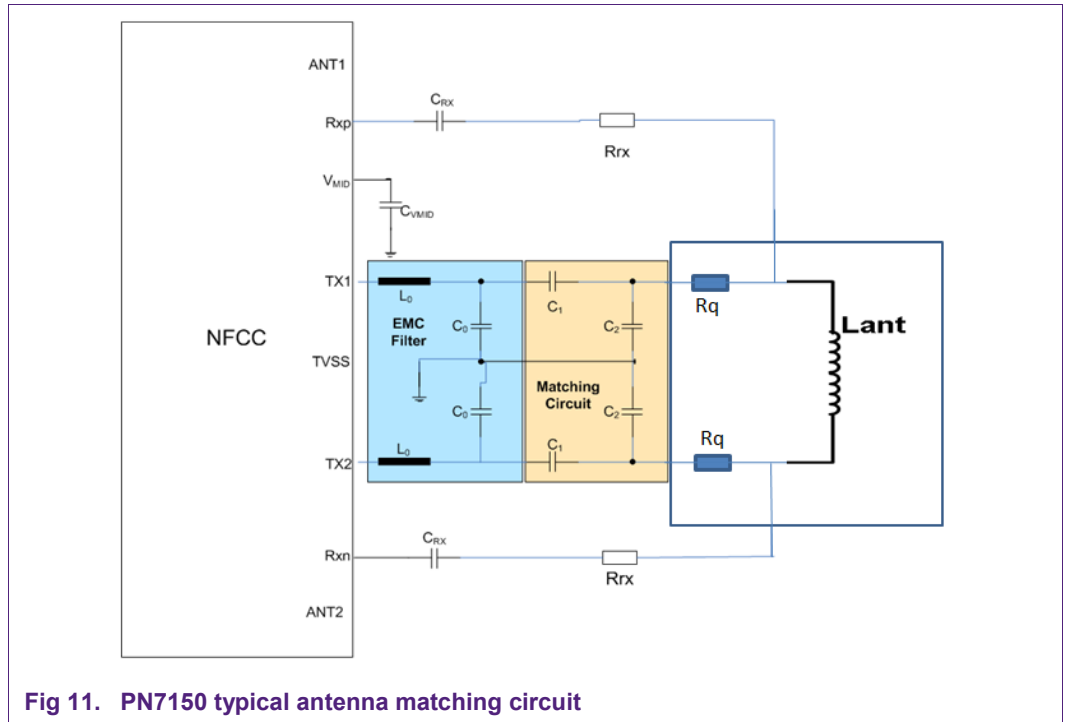


Fig 11. PN7150 typical antenna matching circuit

Although the recommendation is the combination TX1/RXN and TX2/RXP, the inverse (TX1/RXP and TX2/RXN) does not have any impact on PN7150 functionality.

The matching procedure can be summarized in 4 steps. :

- 1) Determine antenna coil characteristics
- 2) Determine EMC filter cutoff frequency
- 3) Determine the matching circuit between the antenna and the EMC filter for Reader Mode.
- 4) Determine the Reception block

Please note that in Active Load Modulation the matching is the same between Card mode and Reader mode

3.2 Antenna tuning/matching procedure overview

An overview of the antenna tuning/matching procedure is depicted on the following figure:

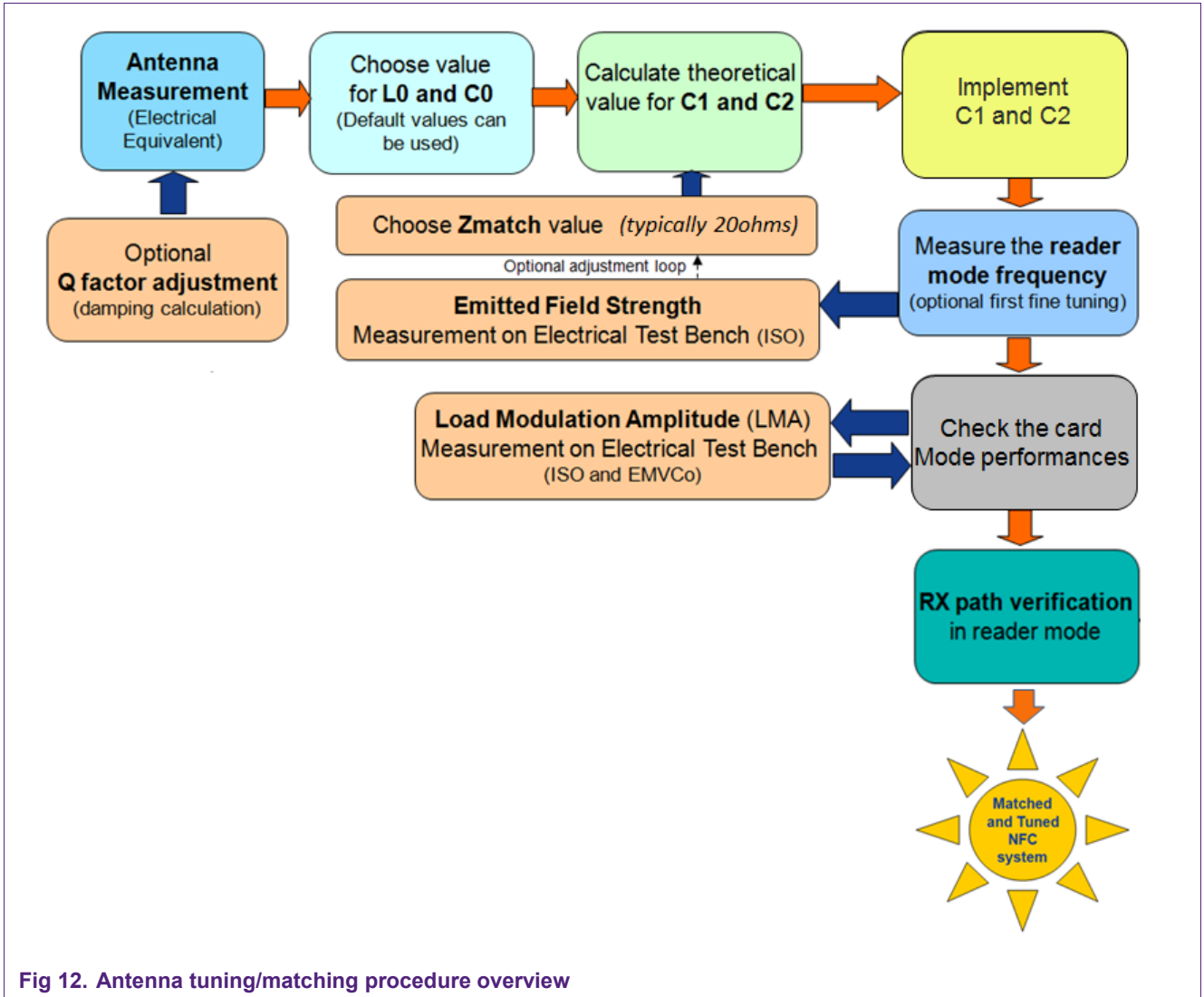


Fig 12. Antenna tuning/matching procedure overview

3.3 Step 1: Antenna model measurement

Based on the antenna physical characteristics, its electrical equivalent model can be measured and computed.

For this, the antenna has to be connected to an impedance analyzer or a network analyzer to measure the series equivalent components.

Please note that the antenna equivalent circuit must be determined under the final environmental conditions especially when the antenna will be operated in metal environment or when a ferrite sheet shall be used for shielding.

The target of this modeling step is to get the L, R, C equivalent of the antenna.

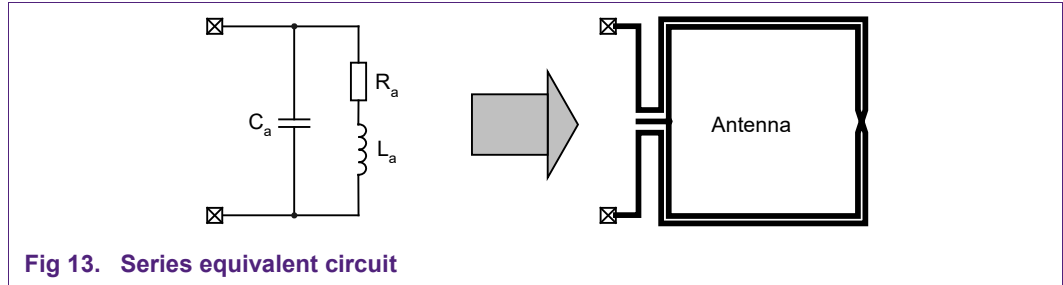


Fig 13. Series equivalent circuit

Recommended values:

$$L_a = 0.3...3\mu\text{H}$$

$$C_a = 3...30\text{pF}$$

$$R_a = 0.1...2\Omega$$

$$f_{ra} \text{ (self-resonance frequency of the antenna)} = 25\text{MHz or above}$$

The antenna parasitic capacitance C_a should be kept low to achieve a self-resonance frequency > 25 MHz as the relation linking those 2 parameters is:

$$C_a = \frac{1}{(2 \cdot \pi \cdot f_{ra})^2 L_a}$$

In order to get these antenna electrical equivalent parameters, 2 methods are proposed below depending on the available equipment:

3.3.1 Measurement method with impedance analyzer

Some impedance analyzers like Agilent 4294A or 4395A can determine directly the series or parallel equivalent circuit by measuring the magnitude and the phase of the impedance of the connected antenna.

The antenna has to be at the final mounting position to consider all parasitic effects like metal influence on quality factor, inductance and additional capacitance.

The antenna needs to be connected to the analyzer by using an appropriate test fixture that does not influence any antenna parameters.

The analyzer has to be calibrated (open, short and load compensation at the calibration plane) and the test fixture needs to be compensated (open, short compensation at the connection points) before each measurement.

Settings: $|Z|$, \ominus

Start frequency: 1 MHz

Stop frequency: above self-resonance frequency of the antenna (point where antenna impedance is real: pure resistance)

Advantages:

- Fast and simple method

Disadvantages:

- High-end equipment required
- Low accuracy of the measurement which especially results from the loss resistance for high quality factor coils ($Q > 60$).

3.3.2 Measurement method with any network analyzer

Alternatively, a network analyzer without any equivalent circuit functionality can be used in combination with some calculation to determine the antenna electrical equivalent.

The antenna needs to be connected to the analyzer by using an appropriate test fixture that does not influence the antenna parameters.

The analyzer has to be calibrated (open, short and load compensation at the calibration plane) and the test fixture needs to be compensated (open, short compensation at the connection points) before each measurement.

Settings: S11

Chart: Smith Z

Start frequency: 1 MHz

Stop frequency: above self-resonance frequency of the antenna

4 parameters must be extracted from the above measurement in order to get the serial equivalent circuit of the antenna:

All 4 parameters are due to the geometry of the antenna, R_s is mainly defined by the thickness of the copper wire, R_p is mainly defined by the skin effect and can be changed by thickness and distance between the turns, and L_a of the antenna is a geometrical value.

Basically, increasing the number of turns increases the Q factor but decreases the effective antenna area and reduces its field strength.

R_s Equivalent resistance at $f = 1\text{MHz}$

L_a Equivalent inductance at $f = 1\text{MHz}$

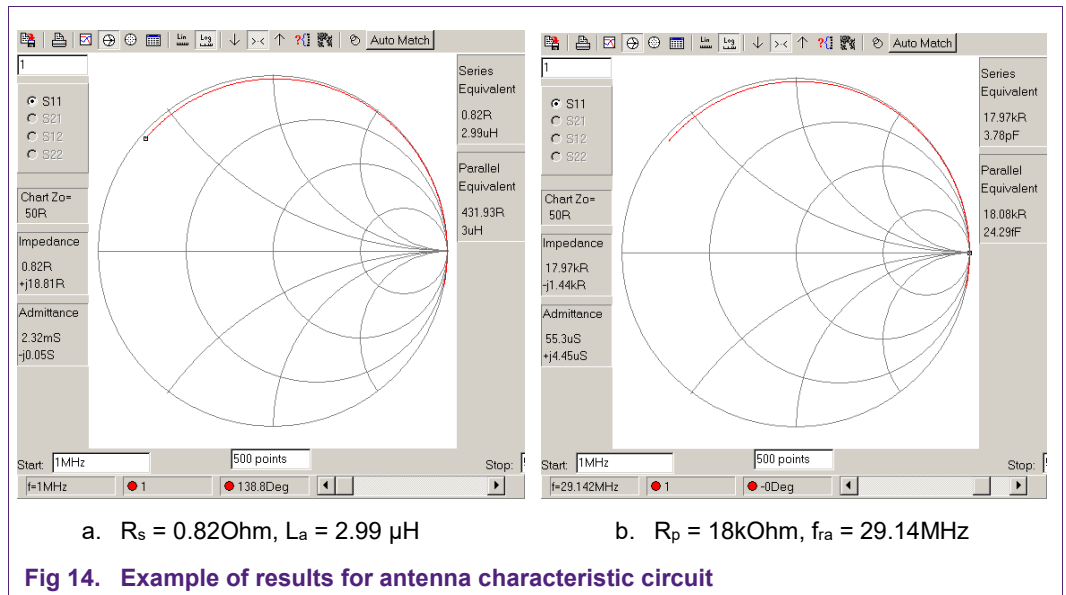
R_p Equivalent resistance at the self-resonance frequency

f_{ra} Self-resonance frequency of the antenna

First the antenna capacitance C_a can be calculated with:

$$C_a = \frac{1}{(2 \cdot \pi \cdot f_{ra})^2 L_a}$$

Fig 14 illustrates the antenna characteristic circuit determination based on the Smith chart:



The series equivalent resistance R_a of the antenna at the operating frequency $f_{op} = 13.56\text{MHz}$ can be calculated out of the characteristic circuit.

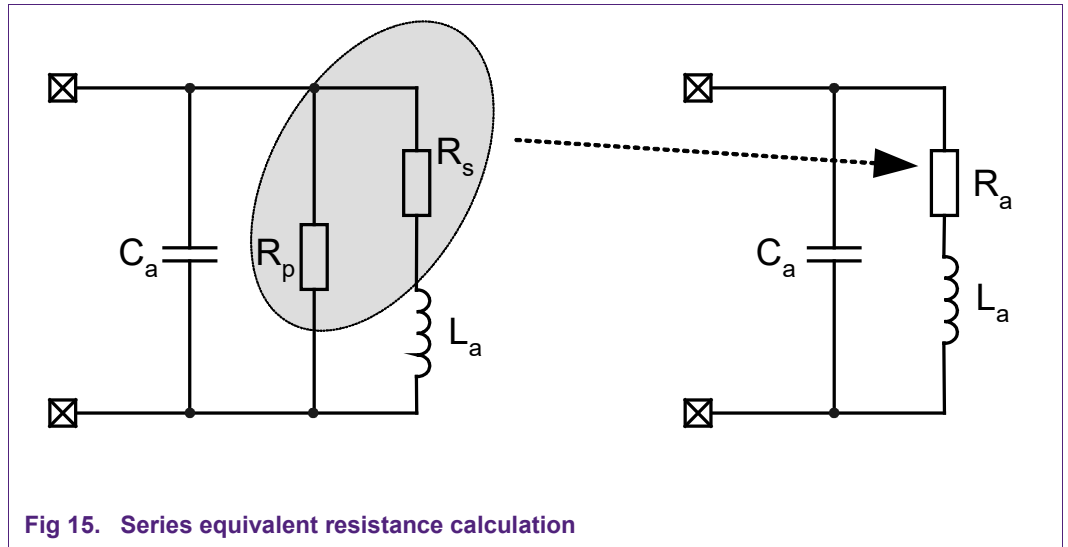


Fig 15. Series equivalent resistance calculation

$$R_p(13.56MHz) = \frac{R_p(fra)}{\sqrt{\frac{13.56}{fra}}}$$

$$R_a = R_s + \frac{(2 \cdot \pi \cdot f_{op} \cdot L_a)^2}{R_p(13.56MHz)}$$

The parallel resistance $R_p(fra)$ obtained by measurements has to be calculated to the parallel equivalent value at 13.56MHz. This is accomplished in first equation.

R_a in second equation is then calculated by using $R_p(13.56MHz)$.

Please note that this equivalent resistor value is then only valid at 13.56MHz.

3.3.3 Optional Quality factor adjustment

The Q factor of the antenna depends on its inductance value and serie impedance (see equation below). It measures the selectivity of the antenna. If the Q factor is too high the antenna can be too selective which can result in too narrow bandwidth of the resonance and can also impact the shaping of the NFC signal. Therefore we recommend the Q factor of the antenna not to exceed 35.

In case the measured antenna quality factor is above this value, R_Q resistors in series can be used to damp it.

The following calculation method can then be used to determine the damping resistor value. The quality factor of the antenna is calculated with

$$Q_a = \frac{\omega \cdot L_a}{R_a}$$

The value of R_Q needed to reach 35 (resistors in series at each side of the antenna) is calculated by

$$R_Q = 0.5 \cdot \left(\frac{\omega \cdot L_a}{35} - R_a \right)$$

Practical consideration:

In an embedded environment where ferrite shielding is required, a quality factor above 35 is very unlikely. In this case, when Q is lower than 35, damping resistor can be skipped.

A correct range for the Q-factor is 20-35.

3.3.4 Determination of the parallel equivalent circuit:

The parallel equivalent circuit of the **antenna together with the optionally added external damping resistors R_Q** has to be calculated as explained below:

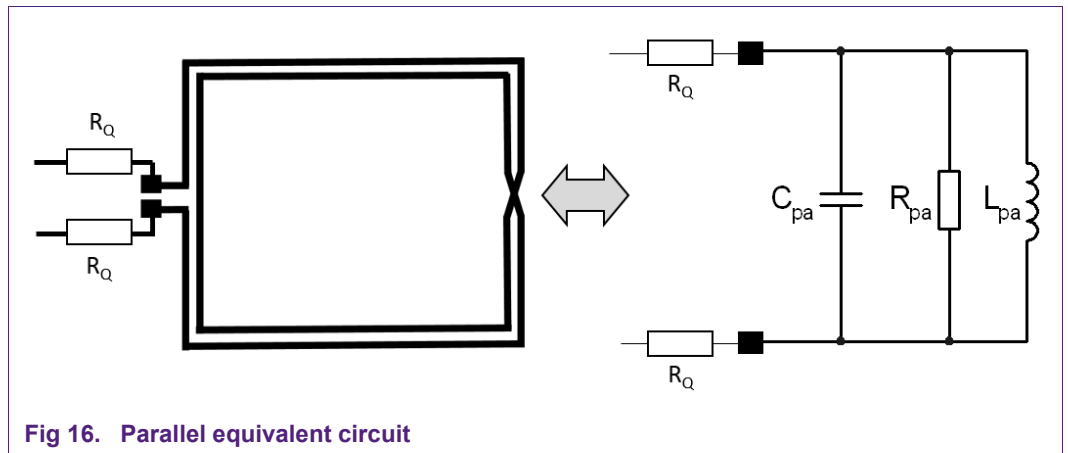


Fig 16. Parallel equivalent circuit

The following formula applies

$$L_{pa} \hat{=} L_a$$

$$C_{pa} \hat{=} C_a$$

$$R_{pa} \hat{=} \frac{(\omega \cdot L_a)^2}{R_a + 2 \cdot R_Q}$$

3.4 Step 2: EMC filter design (L₀ and C₀ definition)

The EMC filter circuit for the PN7150 fulfills two functions: the filtering of the signal and impedance transformation block.

The main properties of the impedance transformation are:

- Decreasing rise time after a modulation phase (reader mode)
- Increasing the receiving bandwidth

L₀ and C₀ value definition:

$$L_0 = 160\text{nH} - 560\text{nH}$$

Filter resonance frequency $f_{r0} = 15.5\text{MHz} \dots 17\text{MHz}$, => C₀

$$C_0 = \frac{1}{(2 \cdot \pi \cdot f_{r0})^2 L_0}$$

The EMC filter resonance frequency f_{r0} has to be higher than the upper sideband frequency determined by the highest data rate (848 kHz sub carrier) in the system.

Example:

A recommended value of 160nH for L₀ is chosen to calculate the capacitance C₀.

$$L_0 = 160\text{nH}$$

$$f_{r0} = 15.5\text{MHz}$$

$$C_0 = 659\text{pF} \rightarrow \text{chosen: } 560\text{pF}$$

The EMC filter and the matching network must transform the antenna impedance Z_{match}(f) to the required TX matching resistance R_{match} at the operating frequency of f = 13.56 MHz.

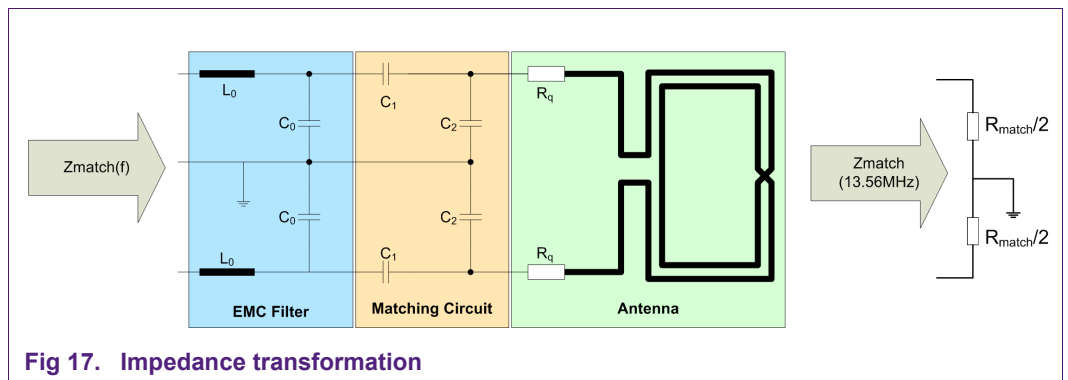
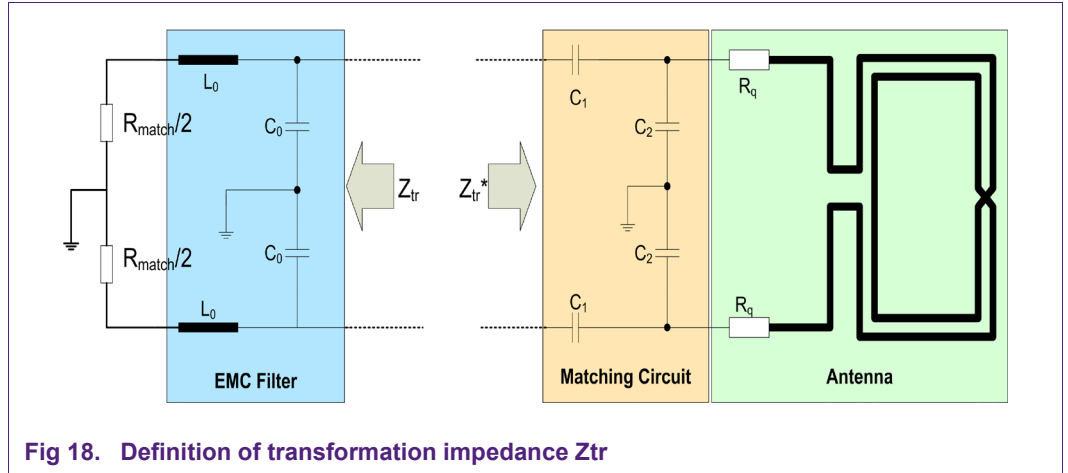


Fig 17. Impedance transformation

The measured $Z_{\text{match}}(f)$ can be modeled in an equivalent circuit loading each TX pin with $R_{\text{match}}/2$ at 13.56MHz.

By cutting the circuitry after the EMC filter and by using the precondition $R_{match}/2$, the remaining components C_1 and C_2 can be calculated.

Please note that $R_{match}/2$ does not correspond to the driver output impedance



$$Z_{tr} = R_{tr} + jX_{tr} \tag{1}$$

$$Z_{tr}^* = R_{tr} - jX_{tr} \tag{2}$$

$$R_{tr} = \frac{R_{match}}{\left(1 - \omega^2 \cdot L_0 \cdot C_0\right)^2 + \left(\omega \cdot \frac{R_{match}}{2} \cdot C_0\right)^2} \tag{3}$$

$$X_{tr} = 2 \cdot \omega \cdot \frac{L_0 \cdot \left(1 - \omega^2 \cdot L_0 \cdot C_0\right) - \frac{R_{match}^2}{4} \cdot C_0}{\left(1 - \omega^2 \cdot L_0 \cdot C_0\right)^2 + \left(\omega \cdot \frac{R_{match}}{2} \cdot C_0\right)^2} \tag{4}$$

3.5 Step 3: Reader mode matching (C₁ and C₂ definition)

C₁ and C₂ are used in combination with the EMC filter to tune the antenna to 13.56MHz and at the impedance value R_{match}.

The resulting Smith card (S11 measured between TX1/TX2 pins) could look as in the figure below for a 30Ω symmetrical tuning.

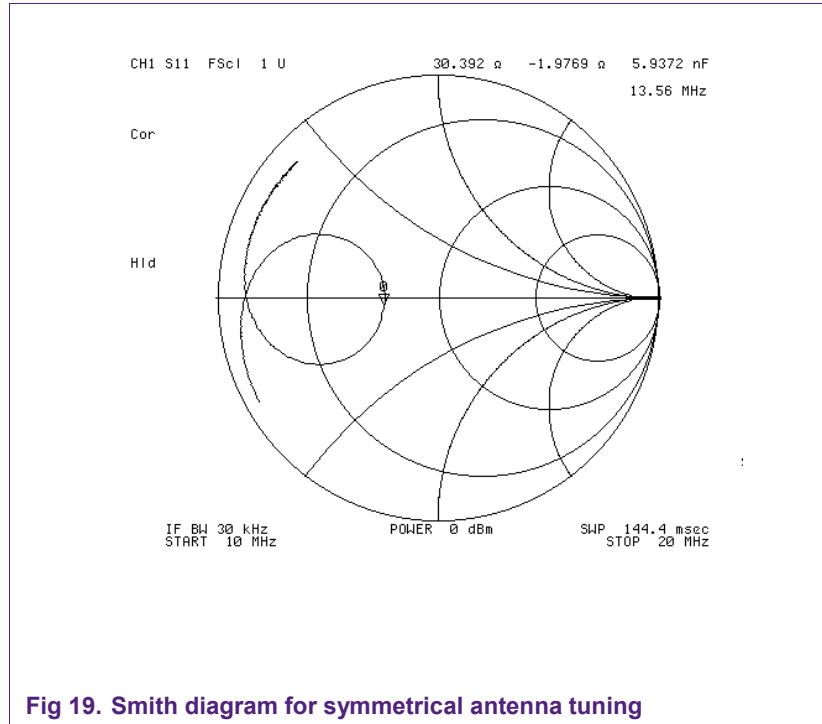


Fig 19. Smith diagram for symmetrical antenna tuning

The reason for the higher cut-off frequency of the EMC filter is a higher stability with close coupling devices in reader mode: less impact of detuning effect on power consumption increase.

The following formulas are then used to calculate the series (C₁) and parallel (C₂) matching capacitances:

$$C_1 \approx \frac{1}{\omega \cdot \left(\sqrt{\frac{R_{tr} \cdot R_{pa}}{4}} + \frac{X_{tr}}{2} \right)} \tag{5}$$

$$C_2 \approx \frac{1}{\omega^2 \cdot \frac{L_{pa}}{2}} - \frac{1}{\omega \cdot \sqrt{\frac{R_{tr} \cdot R_{pa}}{4}}} - 2 \cdot C_{pa} \tag{6}$$

Where L_{pa} , C_{pa} and R_{pa} come from the measured antenna parallel electrical equivalent (see step 1) and R_{tr} and X_{tr} are coming from the EMC filter components value definition (see step2).

The matching circuit elements C_1 and C_2 must be chosen to get the required matching resistance R_{match} at 13.56MHz at the PN7150 TX pins.

Based on the value calculated with the above formula, the matching impedance $Z_{match} = R_{match} + jX_{match}$ must be measured with an impedance or network analyzer. The TX1 and TX2 pins of the PN7150 are the probing points for the network/impedance analyzer to measure Z_{match} .

The optimum R_{match} value for the PN7150 is 30 ohms for small antenna requiring higher current in Reader

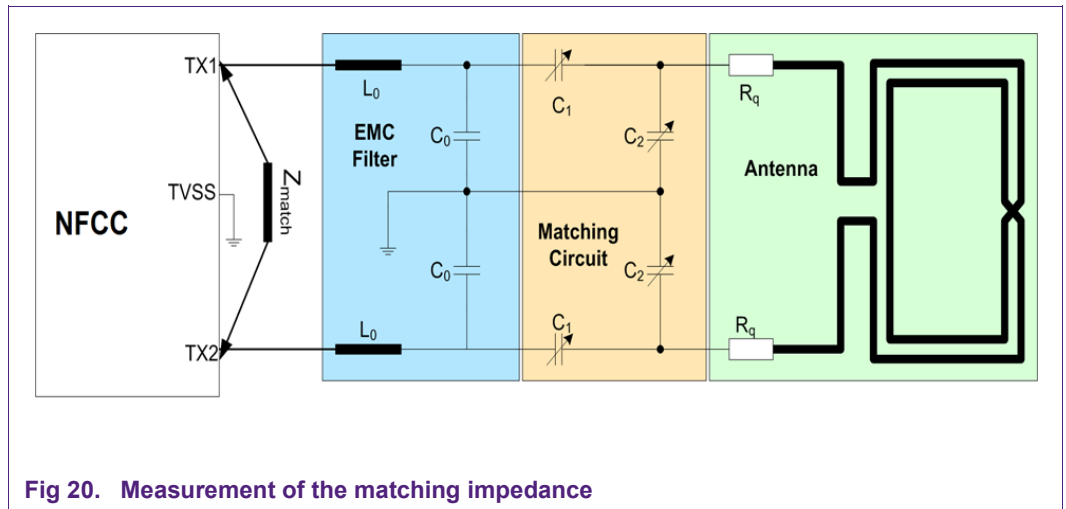


Fig 20. Measurement of the matching impedance

All tuning and measurement of the NFC antenna has to be performed at the final mounting position to consider all parasitic effects like metal which influences the quality factor, the inductance and parasitic capacitance.

Those theoretical values for C_1 and C_2 calculated from formulas 12 and 13 need to be applied on a real circuit and the resulting Smith chart should be measured.

The components values can then be adjusted in order to fine tune the system. (Theoretical values contain some model uncertainty and antenna measurement uncertainty as well).

3.6 Step 5: Rx path tuning (R1 & Crx definition)

3.6.1 Receiver Block functionality

The Rx block consists of an AGC which regulates in order to reach the optimum receiver input voltage. To achieve this, the AGC can attenuate the Rx signal coming from the antenna thanks to a voltage divider. The series resistance is external to the chip, the shunt resistance is in the Rx block, switchable in a certain range.

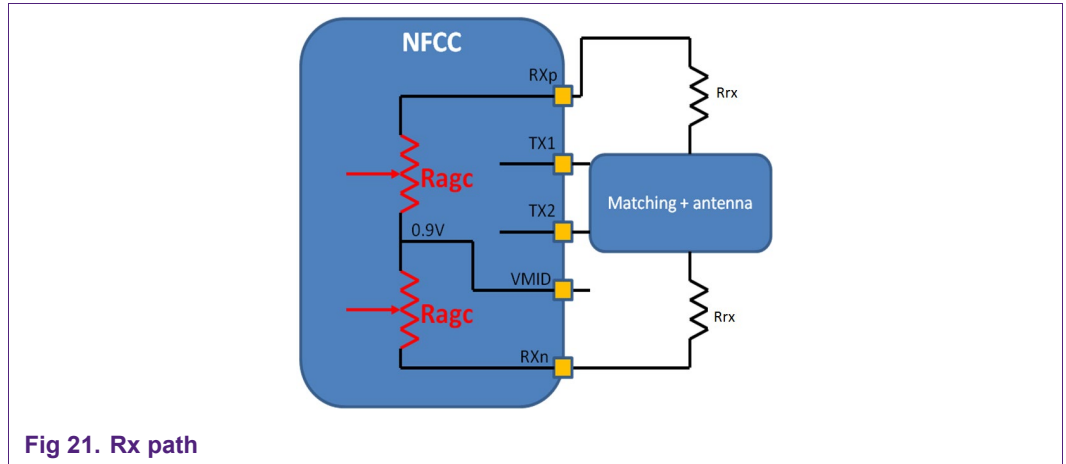


Fig 21. Rx path

On the graph below the AGC role is shown. The oscilloscope snapshot gives the typical 13.56MHz sinewave expected on the Rx pin (on a 0.9V DC bias).

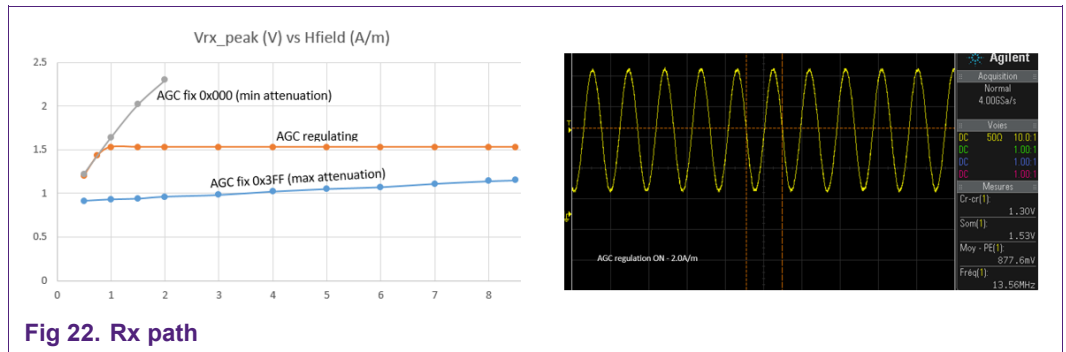


Fig 22. Rx path

The orange curve shows the Rx peak voltage (probed on the Rx pin with a low capacitance oscilloscope probe) when the device is placed on an ISO bench generating the expected H field. We can see that above 1A/m the Rx voltage is regulated to approximately 1.55V (target is 1.6Vpk). Below 1A/m the signal received at the antenna is not enough to be regulated up to this optimal value.

The grey curve gives the Rx Vpeak value when the AGC is not regulating but fixed to its minimum attenuation (code=0x000). It is not recommended to have a signal above 2Vpeak.

The blue curve gives the Rx Vpeak value when the AGC is not regulating but fixed to its maximum attenuation (code=0x3FF). Here the signal is too much attenuated and stays in a 1Vpk range.

3.6.2 Rx connection

As shown at the beginning of this chapter, two configurations are possible for the Rx path components.

- 1- The first one consists in connecting an R, C serial network between the Rx pins and the EMC filters termination point.
- 2- The second connection path is a direct connection of the RX circuit at the antenna pads. In this case, the Crx AC coupling capacitor can be removed but we advise to keep it connected to avoid to decrease too much the Q factor of the antenna

The purpose of the Crx capacitors is to provide an AC coupling of the Rx signal. A value of 1nF can generally be used.

R1 (Rrx) resistor provides a voltage attenuator bridge (made of R1 series + R_{agc} shunt) to adjust the Rx voltage swing.

- 1- The first stage of the Rx path tuning process is to define which Rx path connection is the best.

Direct Rx path tuning allows to reach a better sensitivity in card mode but the direct connection at the antenna connections tends to reduce the quality factor of the antenna which affects the reader mode performances (due to larger transmission losses) and the transmission strength in card mode.

This is particularly the case when the value of the RX resistor is low.

In order to determine where to connect the Rx path, the Rx circuitry must be disconnected and the voltage amplitude must be measured at the 2 possible connection points in reader mode and under an external RF field of 1.5A/m in card mode:

- a. If the voltage at the EMC filter in card mode is big enough (@1.5A/m ~ 1V or more) use the EMC filter as starting point for the RX path tuning
- b. If the voltage is not large enough the RX path has to be connected to the antenna

For small ALM antennas, it is strongly advised to connect the Rx Path directly to the antenna since due to low antenna coupling the signal amplitude at the EMC filter is likely to be smaller than 1V.

- 2- Once the RX connection point has been defined, R1 value must be carefully adjusted to be close to the edge of the allowed input range under worst case conditions. Otherwise, the reception capabilities of the device could be reduced (if R1 is too high, H_{min} in card mode will be reduced).

For the RX path tuning process, both reader mode and card mode must be considered and R1 value must be defined for the highest voltage measured.

- a. In card mode, the worst case conditions are met when an external RF field of 7.5A/m is applied on the device. These conditions can be easily obtained with an *ISO10373-6 [1]* assembly PCD test bench.
- b. In reader mode, the worst case conditions are antenna dependent and they are linked to the tag load applied. Therefore it is recommended to switch-on the PN7150 RF field and to try different tag load to determine the maximum amplitude that can be reached on the RX connection point.

Table 1. Rx connection pros and cons

	Pros	cons
Rx connected to EMC filter	- The Rx path connection doesn't decrease the Q factor -Recommended connection for big antenna	Amplitude signal might be not enough to guarantee good performances especially with small antenna and ALM
Rx connected to Antenna	Maximize the signal captured by the Rx path=> useful for clock recovery accuracy for ALM	The Rx resistor value impacts the Q factor

The NXP recommendation is to use an antenna connection for small antennas (typ. smaller than 800mm²) and an EMC connection for big antenna (typ. larger than 800mm²).

3.6.3 Rx resistance selection process:

Here is the proposed Rx resistor selection procedure:

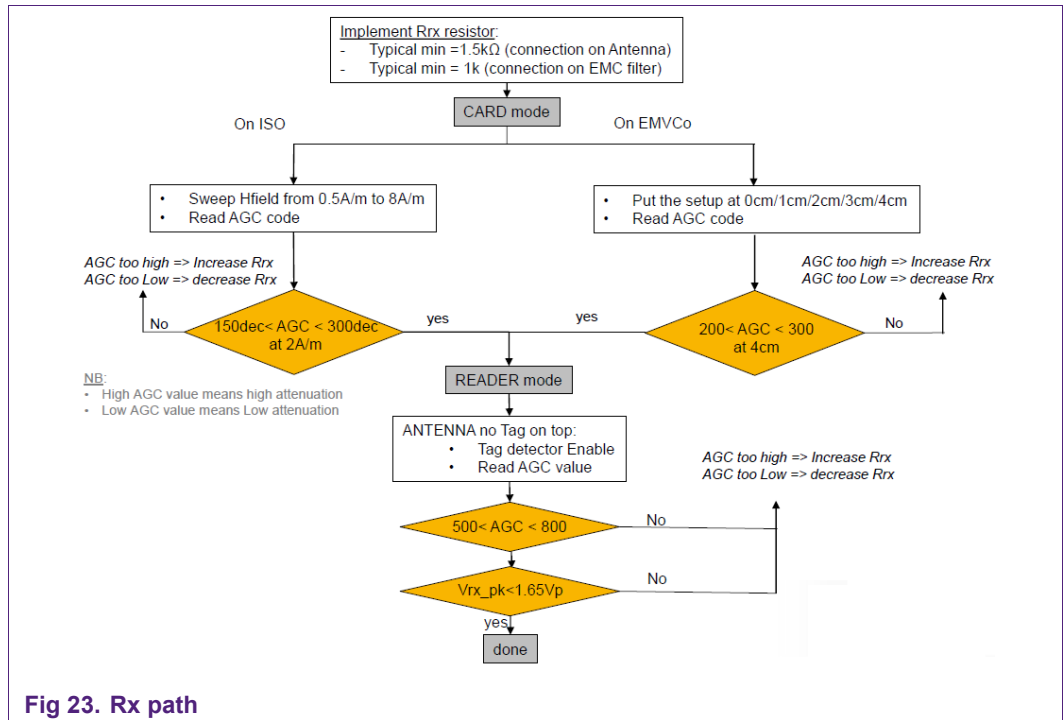


Fig 23. Rx path

3.6.4 Read AGC values

3.6.4.1 Reader mode

Reading the AGC value in READER mode is done using Low Power Card Detector trace mode. This feature is further described in PN7150 User Manual (see [5]).

First, this must be enabled within parameter TAG_DETECTOR_CFG before starting the discovery loop.

In an Android or Linux based device this is insured by defining the following configuration to *libnfc-nxp.conf* file:

```
#####
# NXP Proprietary core configuration extensions
# For more details refer to the NFC Controller User Manual
NXP_CORE_CONF_EXTN={20, 02, 09, 02,
    A0, 5E, 01, 01,
    A0, 40, 01, 81
}
```

Then, at each loop, RF_LPCD_TRACE_NTF notification will be raised indicating the AGC value measured.

From logs, user can filter out the NCI response starting with “6F 13”

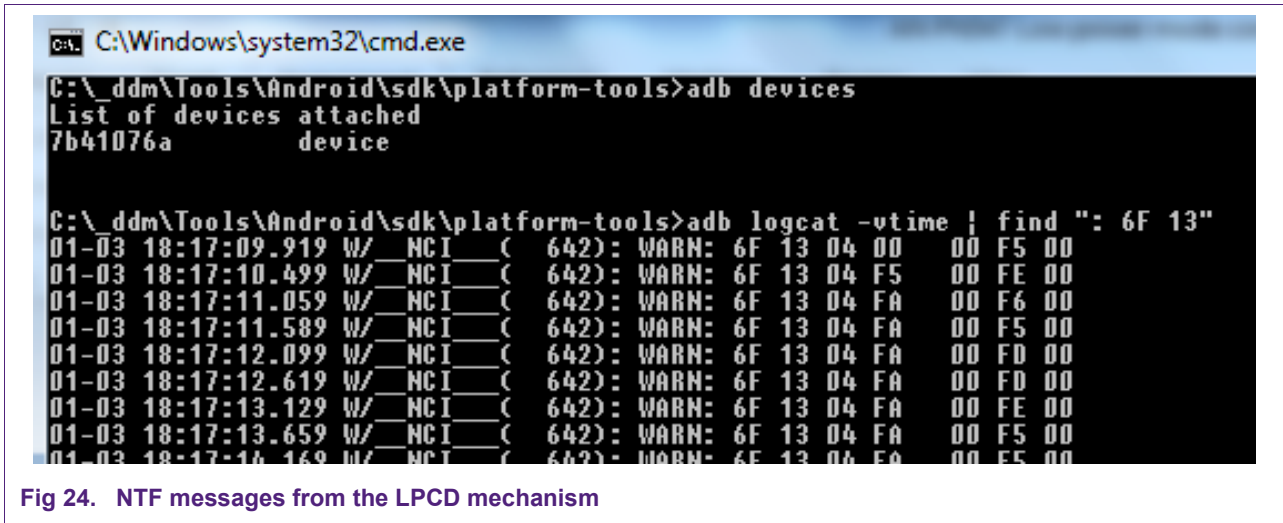


Fig 24. NTF messages from the LPCD mechanism

Useful information are 6th & 7th bytes (last 2 bytes) of the Notification.

For example:

NTF: “6F 13 04 F5 00 **FE 00**”

AGC Read value to be used is “**FE 00**” => 0x00FE => 254 in decimal

3.6.4.2 Card mode

Reading the AGC value in CARD mode is done using TEST_GET_REGISTER_CMD (“2F 33 04 40 00 40 D8”). This feature is further described in PN7150 User Manual (see [5]).

In an Android or Linux based device this is insured by defining the following configuration to *libnfc-nxp.conf* file:

```
#####
# Disable          0x00
# Enable          0x01
NXP_AGC_DEBUG_ENABLE=0x01
```

This will trigger a periodic read of AGC register as soon as RF field is detected.

NCI Test command is “2F 33 04 40 00 40 D8”.

From logs, user can filter out the NCI response starting with “4F 33”

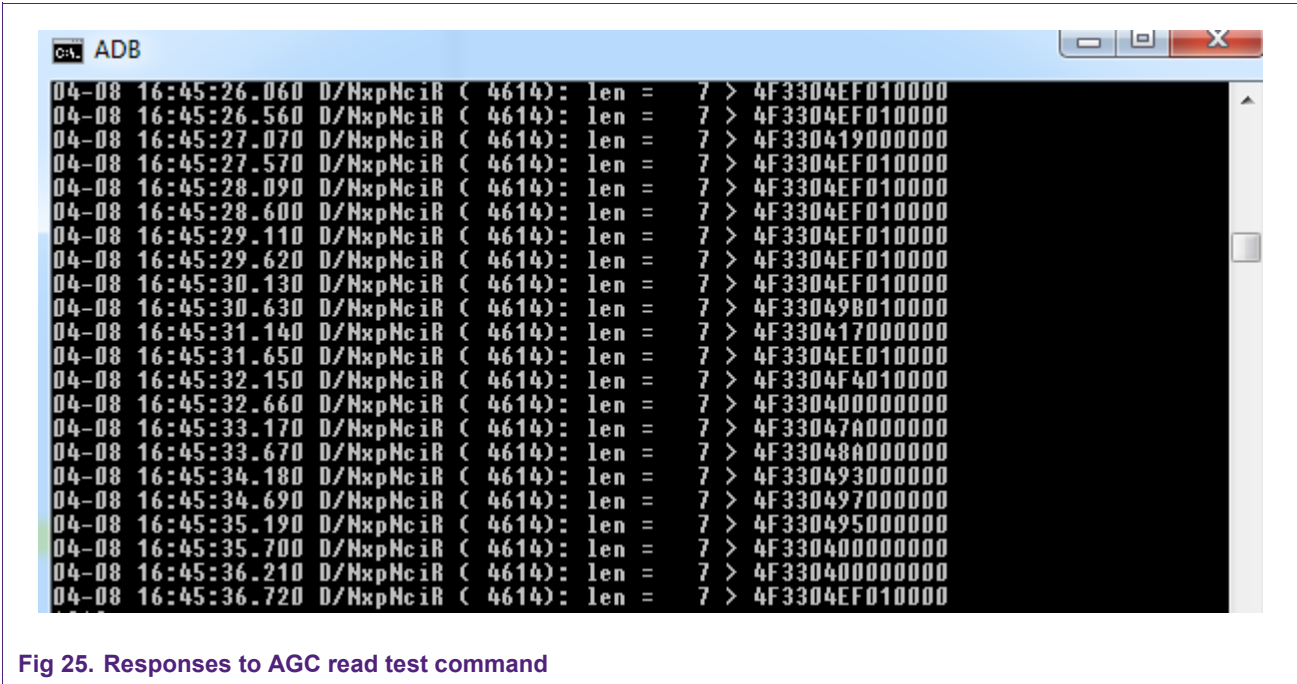


Fig 25. Responses to AGC read test command

Useful information are 4th & 5th bytes of the Test Command Response.

For example:

CMD: “2F 33 04 40 00 40 D8”

RSP: “4F 33 04 **93 00** 00 00”

AGC Read value to be used is “**93 00**” => 0x0093 => **147** in decimal

3.7 Components characteristics

Table 2. Components characteristics

Component	Maximum tolerance	Type	Maximum rating
L ₀	5%	Murata LQW18 (wire wound) TDK MLJ1608 (Multi Layer Ferrite)	210mA at least at 13.56MHz
C ₀	5%	NP0 - COG	16V at least
C ₁	2%	NP0 - COG	50V or 25V(*)
C _{2a}	2%	NP0 - COG	50V or 25V(*)
C _{2b}	2%	NP0 - COG	50V or 25V(*)
R _q	5%	N/A	N/A
R ₁	5%	N/A	N/A
C _{RX}	5%	X7R	50V or 25V(*)
C _{VMID}	10%	X7R	4V at least

(*) the choice of the voltage 50V or 25V is depending on the antenna characteristics and the operating conditions: the voltage at antenna terminals should be measured in the worst case conditions e.g. measurement in card mode by using the [ISO10373-6 \[1\]](#) assembly PCD test bench to generate a field strength of 12A/m.

4. Matching/Tuning verification

The antenna has first to be matched to the PN7150 as described in the previous chapter. Then the steps described below can be followed to verify the antenna matching/tuning. During the antenna matching process the PN7150 IC is not powered.

In order to guaranty the correct functioning of the device in all conditions a matching impedance of the antenna of 30Ω is recommended. Indeed, due to antenna detuning when approaching a tag, the PN7150 will see a lower load which can alter its correct functioning and expected performances.

However, in some conditions a 25Ω can be used.

The functional limit being 20Ω it is not recommended to target it in production as due to component spread the performances cannot be guaranteed in all conditions.

In the table below the simulation results of the impact of C1 and C2 components on impedance matching are given. Of course not all simulation corner cases have been simulated, but this gives a good idea of the importance of the matching component values accuracy.

Table 3. Impact of C1 and C2 component errors on matching impedance

C1/C2 deviation	-5%	-2%	0%	+2%	+5%
Impedance @13.56MHz	16.5Ω	26Ω	30Ω	24.5Ω	20Ω

Moreover, as illustrated on the figure below the tuning is no more real.

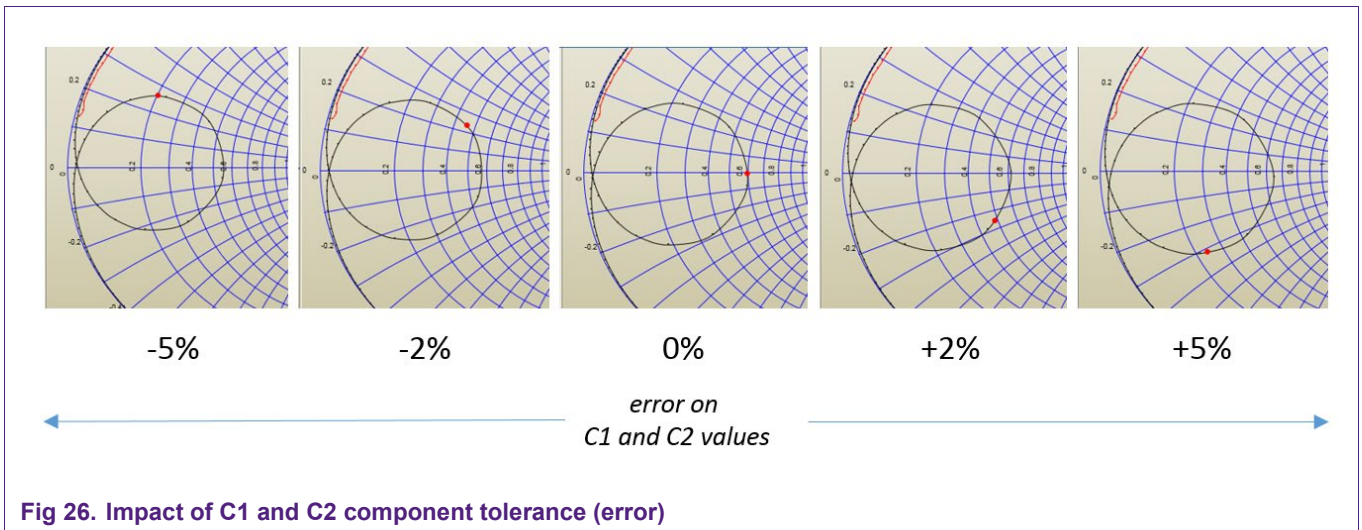


Fig 26. Impact of C1 and C2 component tolerance (error)

4.1 Impedance matching verification for TVDD=3.3V

For a standard setup where the TXLDO is set to 3.3V or below (generating a TVDD=3.3V) a symmetric impedance curve with $R_{match}=30\Omega$ at 13.56 MHz shall be seen on the network analyzer as on the figure below.

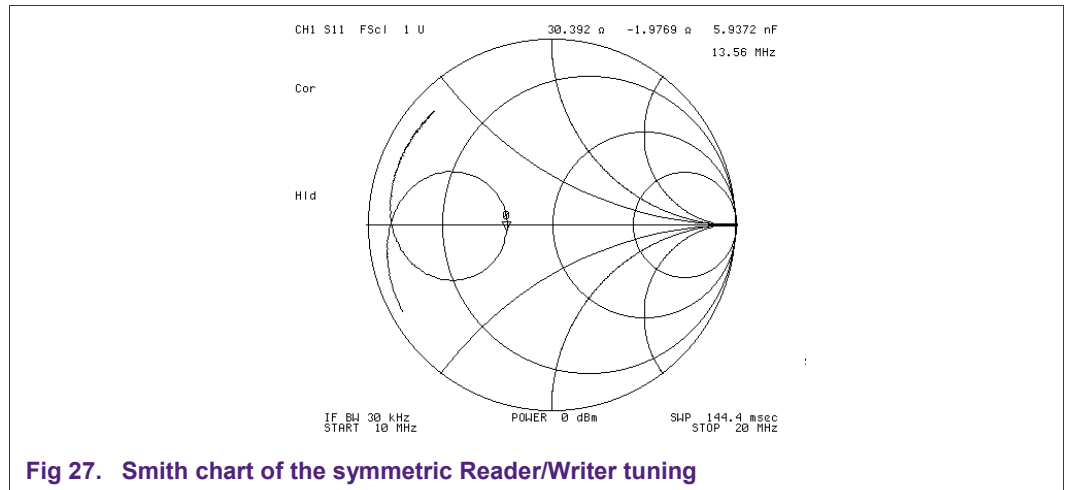


Fig 27. Smith chart of the symmetric Reader/Writer tuning

Practical considerations:

The target of the matching/tuning is to find the right component values such that:

- Reader/Writer mode → $R_{match}=30\Omega$ at 13.56 Mhz
- Card mode → the smith chart is the same.

Remark:

The value of C_1 changes the magnitude of the matching impedance. After changing C_1 the imaginary part of Z_{match} must be compensated by adjusting C_2 as well.

C_2 changes mainly the imaginary part of Z_{match} .

Here are some typical behaviors that can be observed on the network analyzer while playing on C_1 , C_2 and C_0 :

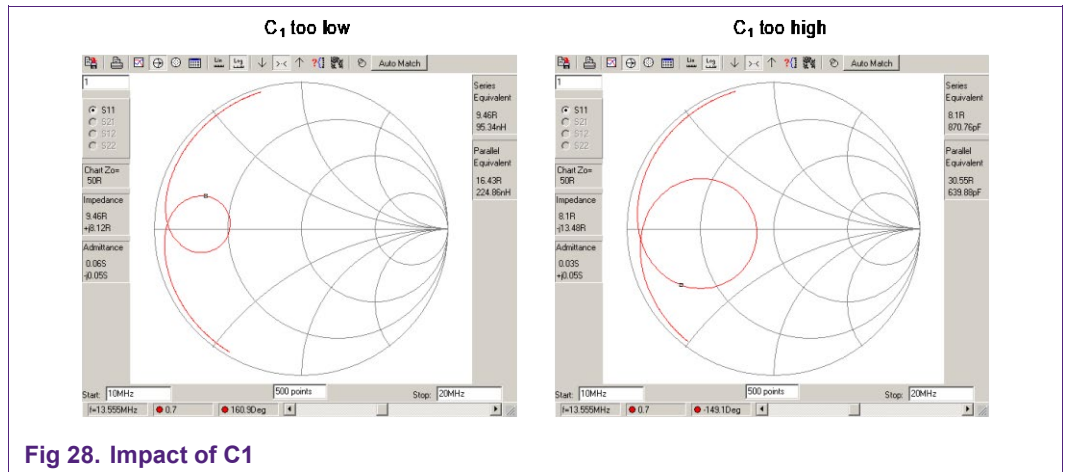
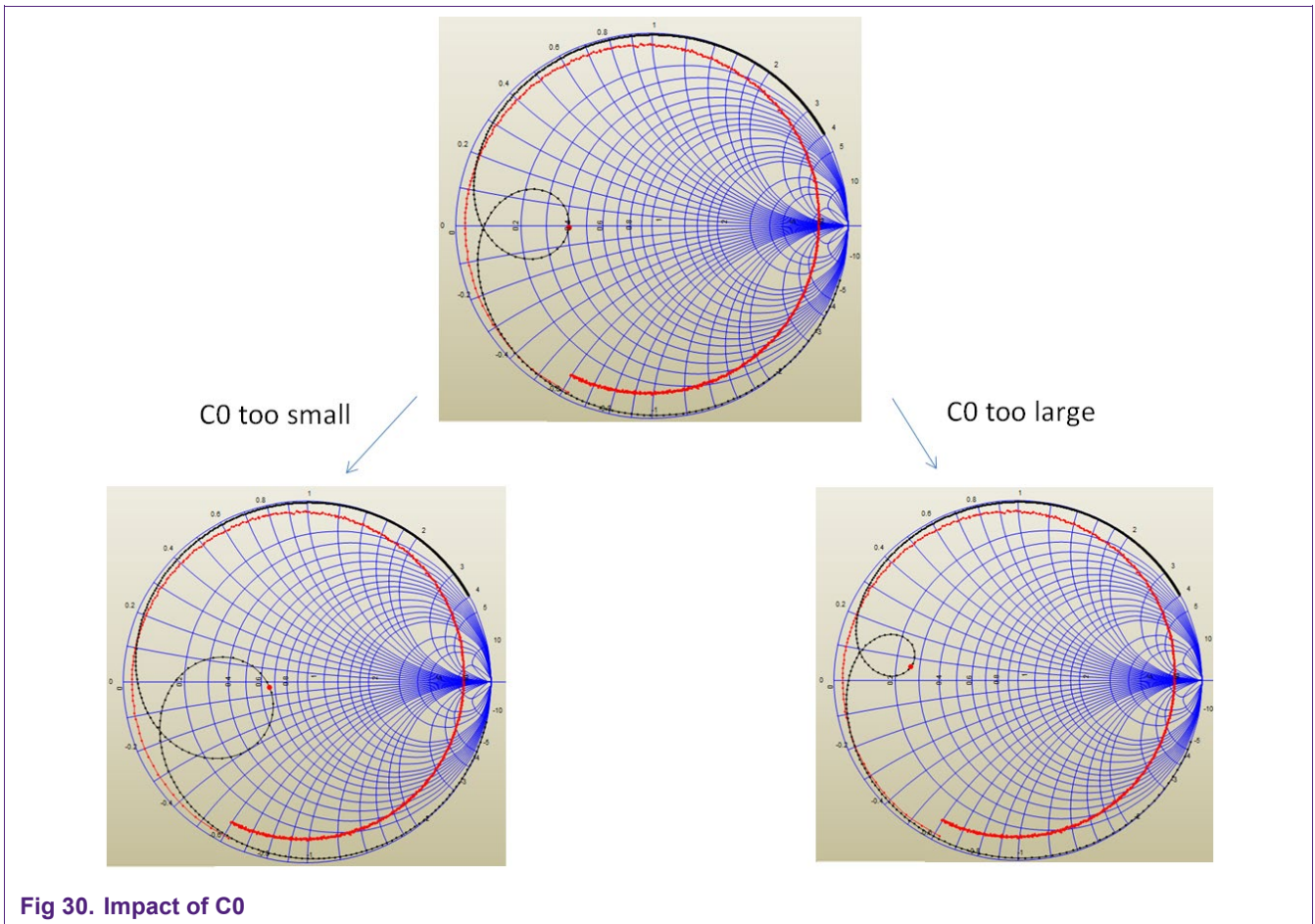
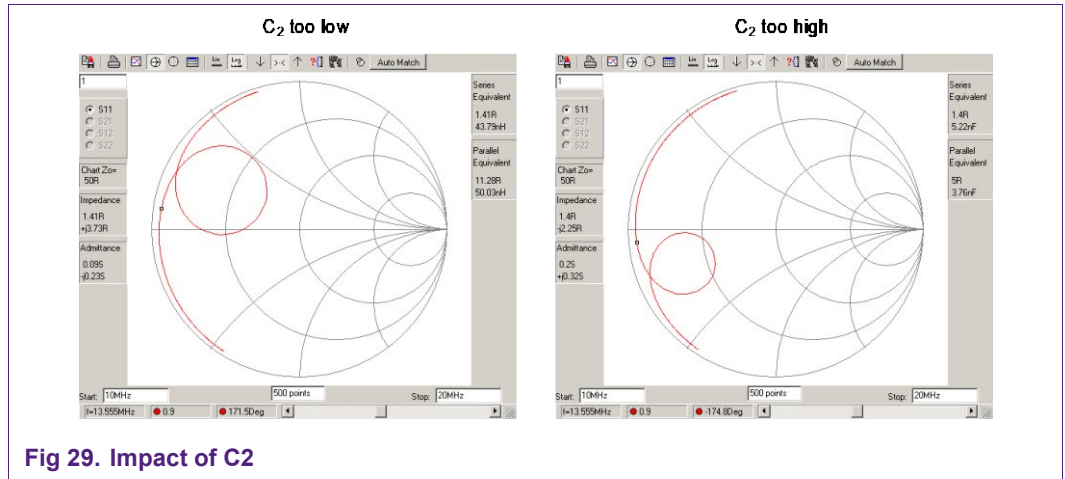


Fig 28. Impact of C1



4.2 Impedance matching for TVDD=4.7V

When the chip is used with TXLDO set to 4.7V or more generally using a TVDD at 4.7V or 5V (using external 5V DCDC) the target matching is $R_{\text{match}}=30\Omega$ at 13.56 MHz asymmetric tuning. It shall be seen on the network analyzer as on the figure below.

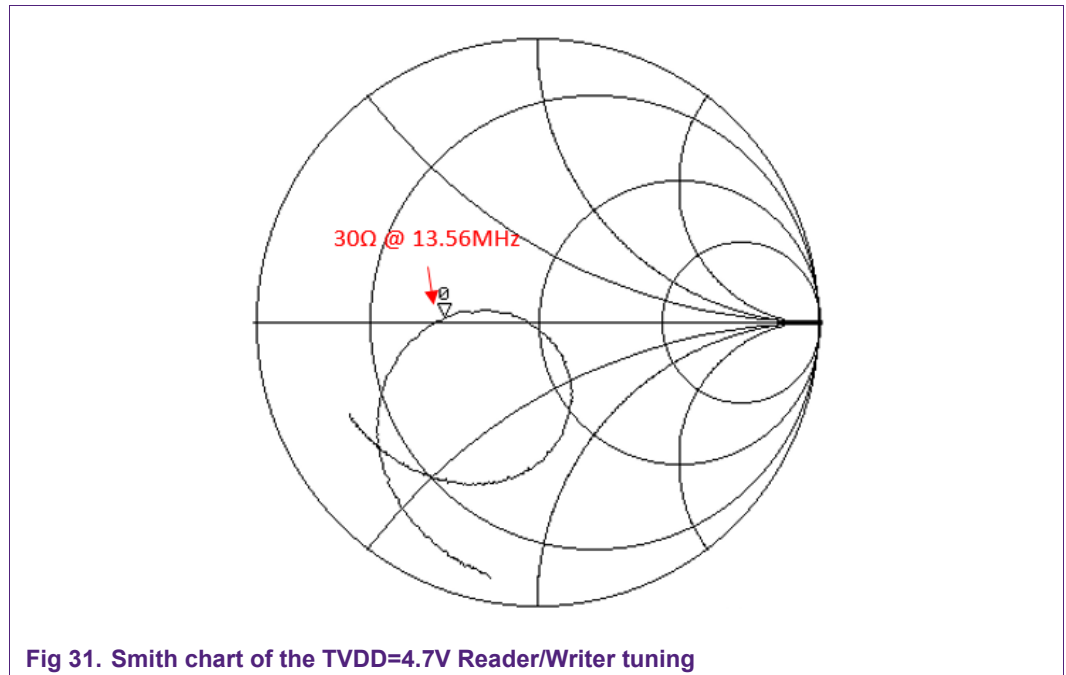


Fig 31. Smith chart of the TVDD=4.7V Reader/Writer tuning

5. Performance verification and fine tuning

This section will show you on how to verify the performance of your device after the matching done. This verification gives only an overview of the performance of the system once a register tuning is also request to achieve the optimal performance.

There is two possibilities to check the performance of your antenna. The first method is to compare the interoperability with other devices. For example on card mode you can measure the communication distance with a reader from the market, on reader mode you can check the communication distance with well-known cards.

A second option is to check the performance of your device against a contactless standard. Currently 3 standards are the most common in the contactless world. There is not a rule to know which standard you must follow, but for payments purpose the EMV Co standard will be most commonly used. To check the interoperability with mobiles the NFC Forum can be a good option. For other kinds of applications the “ISO” specification is the most common used.

5.1 Main specifications

5.1.1 ISO/IEC 14443 specifics

The ISO/IEC 14443 (called “ISO” in the following, details see [ISO/IEC14443 \[2\]](#)) specifies the contactless interface as widely being used with contactless smartcards like e.g. MIFARE cards.

The ISO/IEC 14443 defines the communication between a reader (“proximity coupling device” = PCD) and a contactless smartcard (“proximity chip card” = PICC). In four parts it describes the physical characteristics (i.e. the size of the PICC antennas), the analog parameters like e.g. modulation and coding schemes, the card activation sequences (“Anticollision”) and the digital protocol.

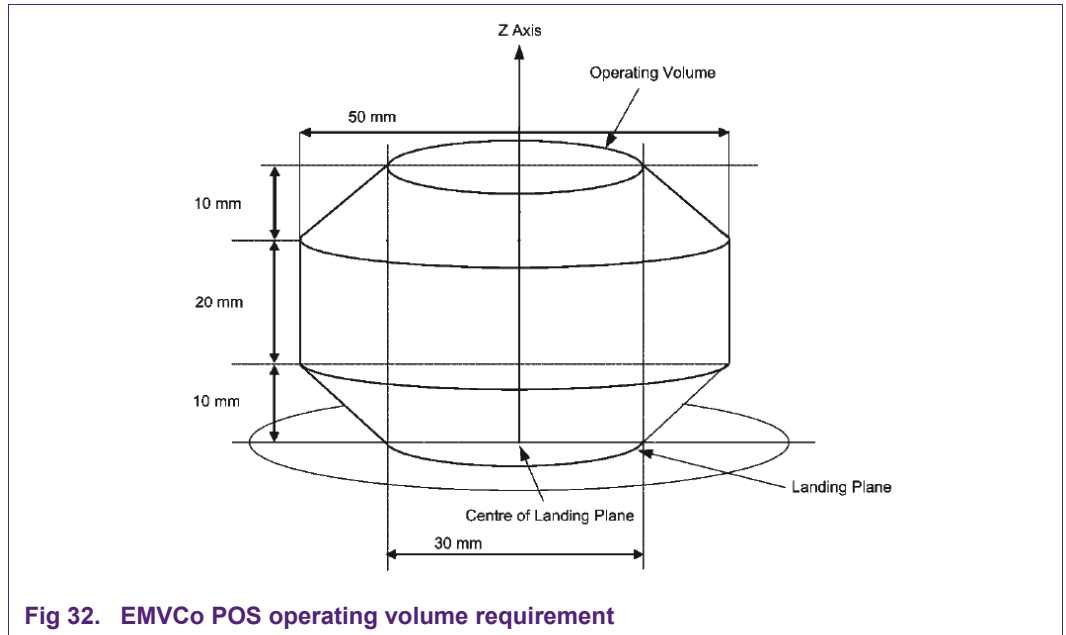
The ISO/IEC 10373-6 [1] describes the test setup and all the related tests for cards and the reader to test the ISO14443 requirements.

This specification covers only Type A and Type B communications.

5.1.2 EMVCo specifics

EMVCo standard [3] it is the most used standard used for contactless payments purpose. It specifies a contactless interface for point of sales (POS) terminals (= PCD) and the corresponding contactless payment cards or mobiles (= PICC). This interface is very similar to the one defined ISO/IEC 14443, but it uses its own set of requirements and specification details. The EMVCo test equipment and way of testing is quite different from the test specification as defined in ISO/IEC 10373-6 [1].

One main difference for the tests is the definition of an operating volume, as shown in *Fig 32*.

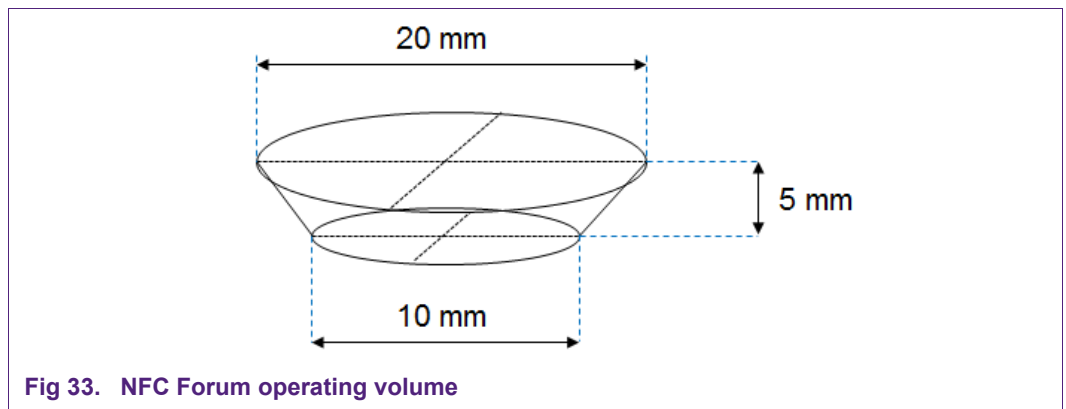


Within this volume the given parameters need to be fulfilled. This specification covers only Type A and Type B communications.

5.1.3 NFC Forum specifics

The NFC Forum is a standard created to promote the use of NFC technology in consumer electronics, mobile devices, PCs, and more.

The standard NFC Forum device needs to fulfill the reader mode (Poller), and card mode (listener). One of the differences between this standard and the others is the use of 3 different protocols during test, the NFC-A, NFC-B and NFC-F and 6 different antennas for testing (3 for Poller tests and 3 for listener tests). Once again the NFC Forum test equipment and way of testing is quite different from the test specification as defined in ISO/IEC 10373-6 and EMV Co. Additionally the NFC Forum specifies an operating volume as shown in Fig 33.



5.2 Performance check against standards

During this section we will show the basics measurements that can be done to check the performance of your device.

We will show the measurements for reader mode and card mode using an EMV Co test bench. For every measurement we will give you the equivalent measurement on other standards.

5.2.1 Reader Mode measurements

The reader mode measurements will be divided in two parts: The transmission part and the reception part.

For the transmission this part the most relevant tests will be:

1. Field strength measurement
2. Waveform measurement

We will show how to perform this measurements using an EMV Test PICC, "ISO" Reference PICC and the NFC Forum Reference Listeners. These hardware can be bought from one of the accredited laboratories.

For the reception part, some specific test are described on these specifications. However we will not cover these tests on this document. To the test the reception part we will perform some functional tests.

5.2.1.1 Field strength measurement

When the PN7150 is configured in READER mode, the strength of the emitted RF field can be measured by using a Reference PICC that is placed at a short distance from the PN7150 antenna. The reference PICC is calibrated on the relevant test bench: its output voltage corresponds to well-defined field strength.

The output voltage of the Reference PICC can be measured with an oscilloscope or directly measured with a voltmeter if the PN7150 is configured to emit a continuous RF field.

Based on the targeted standard compliance, the Reference PICC to be used can be different.

a. EMVCo example

The *EMVCo standard [3]* for payment applications defines a specific Reference PICC and a large operating volume is required: up to 4cm distance.

This operating volume specified can usually not be met by an embedded equipment application.

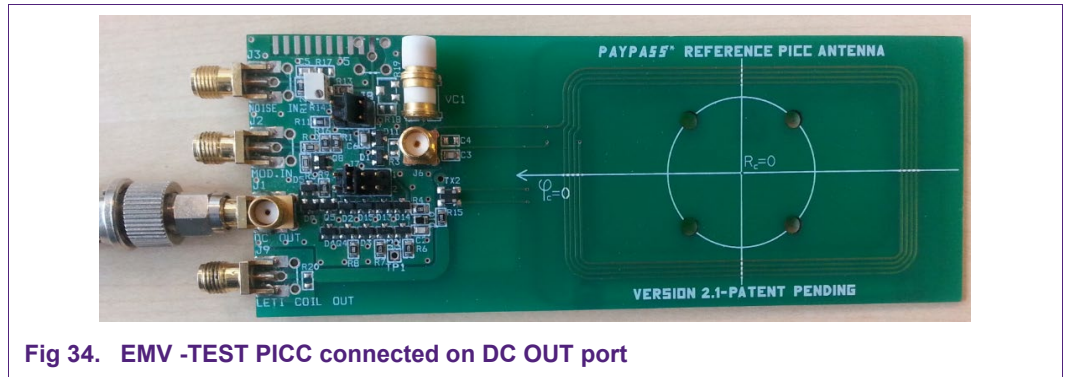


Fig 34. EMV -TEST PICC connected on DC OUT port

Steps:

- 1) Connect the output J1 to an oscilloscope (1Mohms)
- 2) Set the jumper J8 in position 1-4, jumper on the “antenna side”
- 3) Place the EMV - Test PICC in one position of the operating volume
- 4) Set your device to send continuous RF carrier
- 5) Measure the mean value using an oscilloscope
- 6) Check the min and max values against EMV Co specification.

b. ISO example

The Reference PICC to be used to check compliance with the ISO/IEC14443 [2] standard is described in the ISO/IEC10373-6 [1] standard.

Here is the specification of the field strength required by the ISO/IEC14443 [2] standard:

- No operating volume (i.e. area providing a field strength greater than 1.5A/m) is required
- a minimum field strength of 1.5A/m must be achieved
- the maximum field strength must not exceed 7,5A/m

This requirement is usually met at short distance (<2cm) in case of an embedded equipment application.

This test was divided in two different tests H max and H min.

For Hmax test:

- 1) Tune the ISO Reference PICC to 19 MHz
- 2) Adjust the R2 load to obtain 3V measured on the connector CON3 when the TEST PCD assembly produce the H max
- 3) Place the ISO Reference PICC in a test position on the device under test
- 4) Set your device to send continuous RF carrier
- 5) Measure the DC output of the DC output CON3
- 6) The DC voltage at CON3 shall not exceed 3V

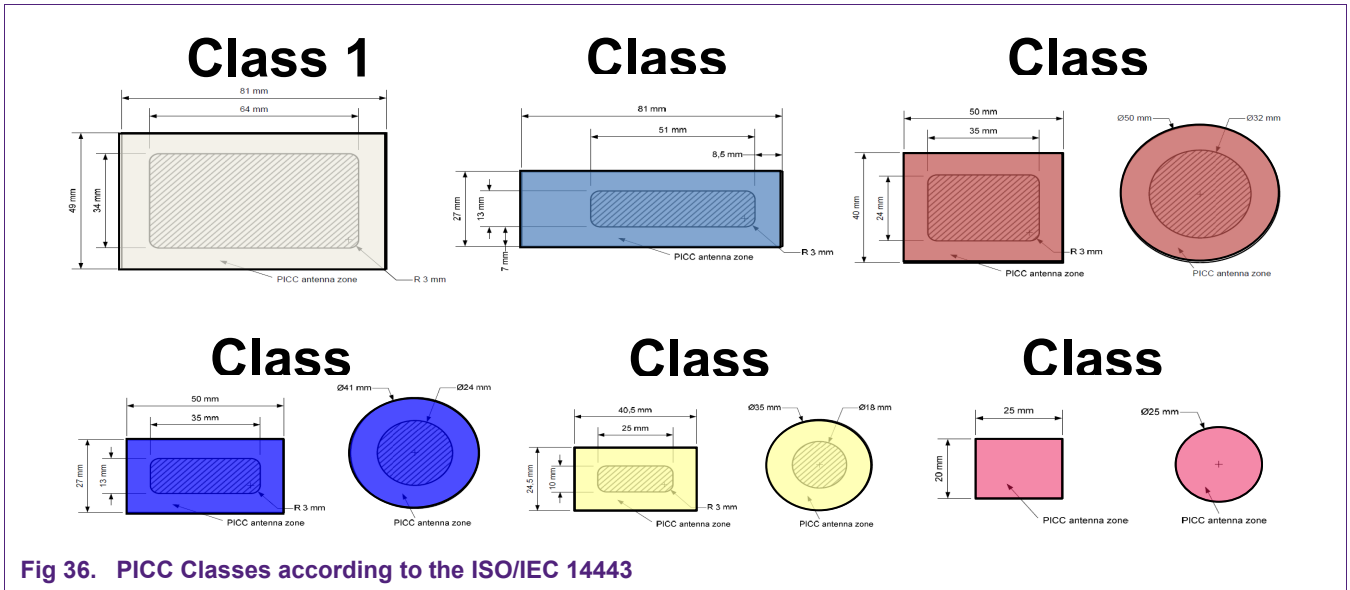


Fig 36. PICC Classes according to the ISO/IEC 14443

c. NFC Forum example

The *NFC Forum standard [4]* defines 3 different Reference PICCs so-called reference listeners: reference Listener 1, reference Listener 3 and reference Listener 6.

The required operating volume is much smaller than EMVCo: the distance is up to 0.5cm only. A test center can be defined for each Listener if the distance between the 3 tests centers can be inside a circle of 20 mm diameter.

The power emission test is divided in two different tests, one for minimum requirements and a second for maximum requirements.

For Minimum Power Emission Measurement:

- 1) Set the load of the reference Listener to 820 ohms
- 2) Place the Reference Listener in a test position on the device under test
- 3) Set your device to send continuous RF carrier.
- 4) Measure the DC output on the connector J1
- 5) Repeat this measurement for all test positions and all reference listeners
- 6) The DC voltage must be inside minimum and maximum limits

For Maximum Power Emission Measurement:

- 1) Set the load of the reference Listener to 82 ohms
- 2) Place the Reference Listener in a test position on the device under test
- 3) Set your device to send continuous RF carrier.
- 4) Measure the DC output on the connector J1
- 5) Repeat this measurement for all test positions and all reference listeners

- 6) The DC voltage must be inside minimum and maximum limits

5.2.1.2 NFC Signal shaping verification

The following verifications provide a quick way to check the shaping of the generated RF signal when the PN7150 is configured in READER mode. An oscilloscope with a bandwidth of at least 100MHz has to be used to carry out the shaping measurements (see Fig 37).

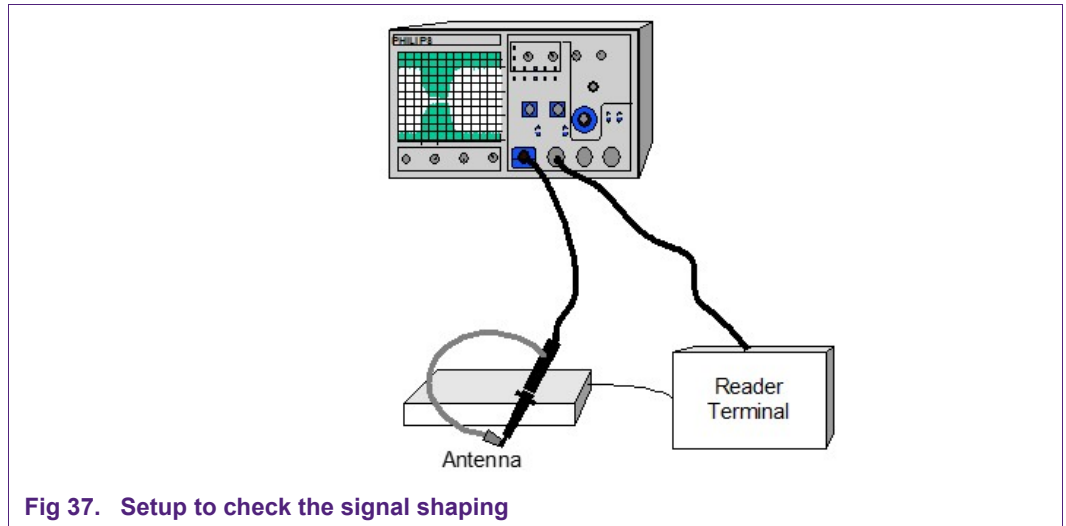


Fig 37. Setup to check the signal shaping

CH1: Use a loop with the ground line shortcut at the probe to enable inductive signal coupling. Hold the probe loop on top of the antenna. When the shaping compliance to a given standard is verified, the corresponding reference PICC must be connected to CH1.

CH2: (optional) used as trigger if possible

The absolute measured voltage in CH1 depends on the coupling (= distance) between the probe loop and the reader antenna.

The influence of the coupling on the shape can be neglected.

Once this quick verification has been done, the proper pick up coil must be used to check the compliancy to the different standards.

a. Waveform measurement using an “ISO” reference PICC

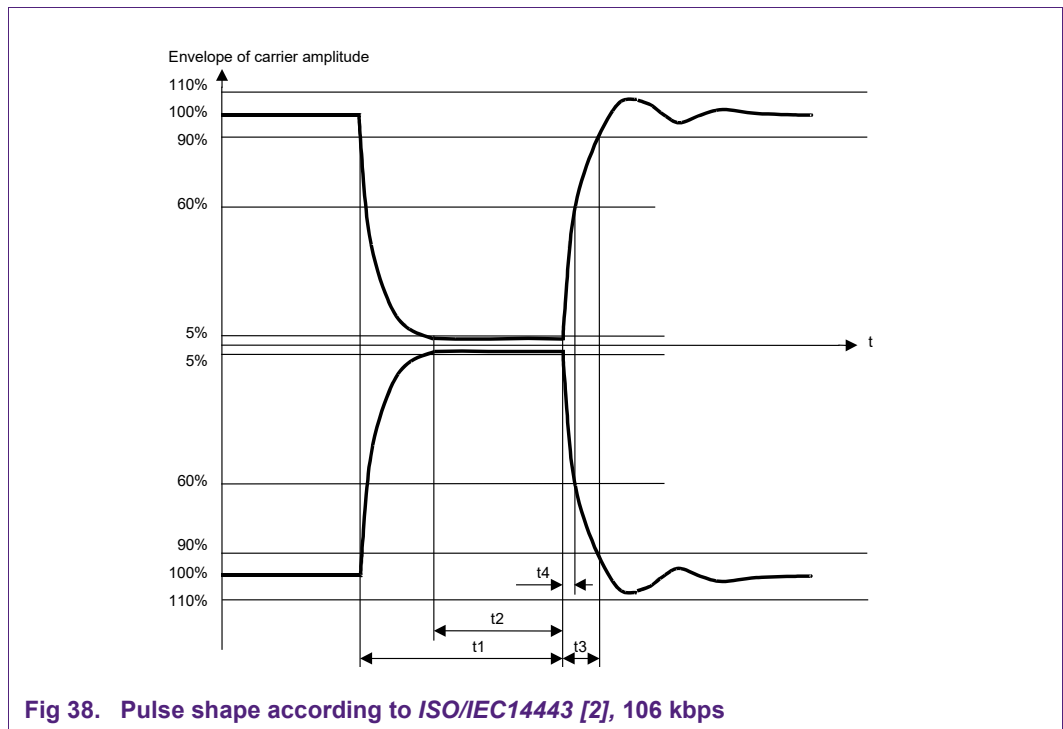
We will show here how to measure the waveform of your device using an “ISO” reference PICC. This procedure is not the official procedure, once some analysis tools described on this specification will not be used. However this procedure it is a good overview of the waveform measurement defined on “ISO”.

Procedure:

- 1) Tune the ISO Reference PICC to 16.5 MHz
- 2) Place the ISO Reference PICC in a test position on the device under test

- 3) Adjust the R2 load to obtain “Vload” (6V for class 1 ref PICC) measured on the connector CON3
- 4) Set your device to send a Type A or Type B command.
- 5) Using an oscilloscope trigger your acquisition to correct acquire a Type A or Type B pause.
- 6) Using the cursors of the oscilloscope measure the timings described on the figure below
- 7) The Timings measured must be inside minimum and maximum limits

It is recommended to check the pulse shape with the Reference PICC according to the values given in Fig 38 and Table 4.



The times t1-t2 describe the time span, in which the signal falls from 90% down to below 5% of the signal amplitude.

The rising time of the carrier envelope is t4. It must be checked that the carrier envelope at the end of the pause reaches 60% of the continuous wave amplitude within 0.4µs.

Table 4. Pulse shapes definition according to ISO/IEC14443[2], 106 kbps

Parameter	Condition	Min	Max
t1		28/fc	40.5/fc
t2	t1>34/fc	7/fc	t1
t3	t1<=34/fc	1.5 x t4	t1
t4		0	6/fc

*fc = carrier frequency

Please note that the standards can evolved. Final value must be directly retrieved from the latest official publication of the corresponding standard.

The type B modulation index m (see Fig 39) has also to be measured; the criteria are given in Table 5.

It must be noted that the PN7150 integrates an automatic adjustment of the modulation index to keep it constant whatever the antenna environment.

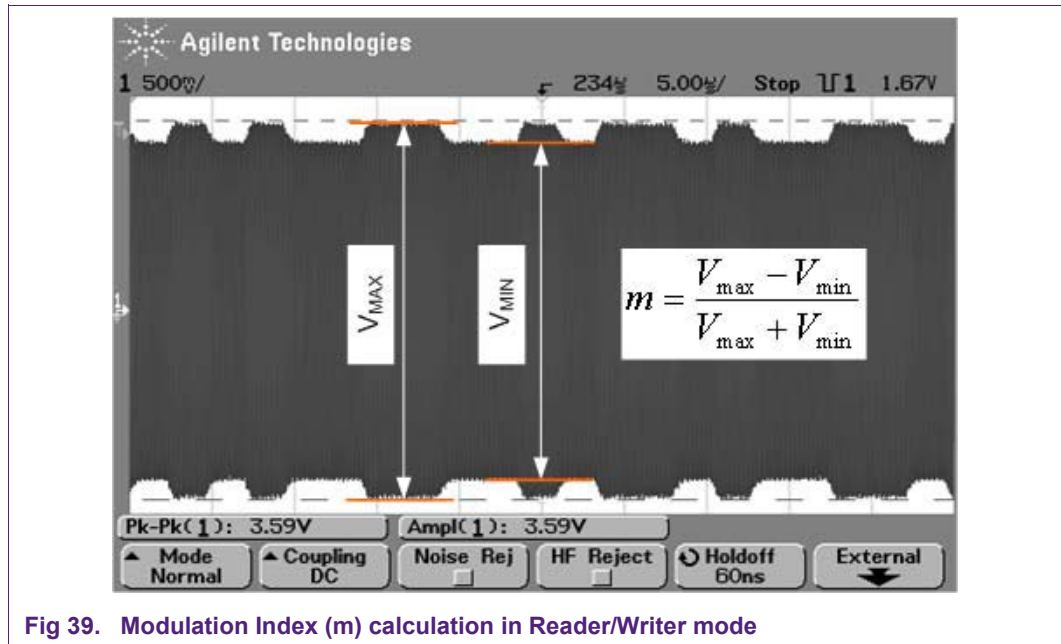


Fig 39. Modulation Index (m) calculation in Reader/Writer mode

Table 5. Type B 106kbps criteria according to ISO/IEC14443

Parameter	Min	Max	Unit
Modulation index	8	14	%
t _r	0	16/fc	
t _r	> 0 and t _f – 8/fc	< t _f +8/fc and 16/fc	

b. Waveform measurement using an EMV Test PICC

The procedure to check the Waveform on EMV Co specification is very similar to the “ISO”. The procedure below is not exactly the official procedure for the EMV Co testing, but it can gives you a good overview of the performance.

- 1) Connect the output J9 to an oscilloscope (50ohms). Additionally EMVCo uses a 20 MHz filter between the oscilloscope and the EMV Test PICC.
- 2) Set the jumper J8 in position 1-2, jumper on the “connector side”.

- 3) Place the EMV - Test PICC in one position of the operating volume (only the center positions will be checked from 0 cm to 4 cm).
- 4) Set your device to send a Type A or Type B command.
- 5) Using an oscilloscope trigger your acquisition to correct acquire a Type A or Type B pause.
- 6) Using the cursors of the oscilloscope measure the timings described in Fig 39.
- 7) The Timings measured must be inside minimum and maximum limits

c. Waveform measurement using a NFC Forum reference Listener

The procedure for the NFC Forum is very similar to the two other specifications. However the particularity is the use of different sizes of antennas and loads during the tests. The test procedure should be done using the reference Listener 1, 2 and 3, and the loads 330 ohms and 820 ohms.

This procedure is not exactly the official procedure for NFC Forum testing, but it can give you a good overview of the performance.

- 1) Connect the output J4 (sense coil) to an oscilloscope (50ohms).
- 2) Set the jumper for the desired load (330 ohms or 820 ohms)
- 3) Place the reference Listener in one position of the operating volume.
- 4) Set your device to send a NFC A or NFC B or NFC F command.
- 5) Using an oscilloscope trigger your acquisition to correct acquire NFC A or NFC B or NFC F command
- 6) Using the cursors of the oscilloscope measure the timings described in *Fig 39*.
- 7) The Timings measured must be inside minimum and maximum limits

5.2.1.3 Reception check

For simplification purposes we will test the reception of our device on reader mode using some functional checks. Even if the 3 different standards presented until now, have their own tests to check the reception of the reader mode. We suggest to check the reception, checking the communication distance in READER mode with some typical cards:

- MIFARE Ultralight
- MIFARE DESFire
- FeliCa card
- ISO/IEC14443-B card

Additionally, using an oscilloscope and a spy coil between the card and the reader it is possible to check if the communication did not occurred because of the reader reception or card reception.

How to check if the problem is from the card or from the reader:

- If you can see the command from the reader but there is no response from the card. This is probably a card reception problem.
- After a response from the card the reader does not send the next expected command. This is probably a reader reception problem.

If you identify one of these situations, the RX path must be measured on the FAIL situation. If the signal is correct, the problem can come from other layers, digital and so on. Additionally, you can use a RF spy from a test tool provider, to be able to check this point.

5.2.2 Card mode measurements

The card mode measurements will be divided in two parts: the transmission and the reception part.

For the transmission part, basically we will check load modulation amplitude for the 3 different standards.

On the reception part, we will check the communication distance with some readers, what we call the sensitivity of the receiver.

5.2.2.1 Load modulation amplitude measurement

When the PN7150 is configured in CARD mode, the data are transmitted by modulating the amplitude of the external RF field.

This is done simply by changing the load impedance presented to the antenna; it is called load modulation.

An illustration of the signal observed on an EMVCo test bench is shown in *Fig 40*.

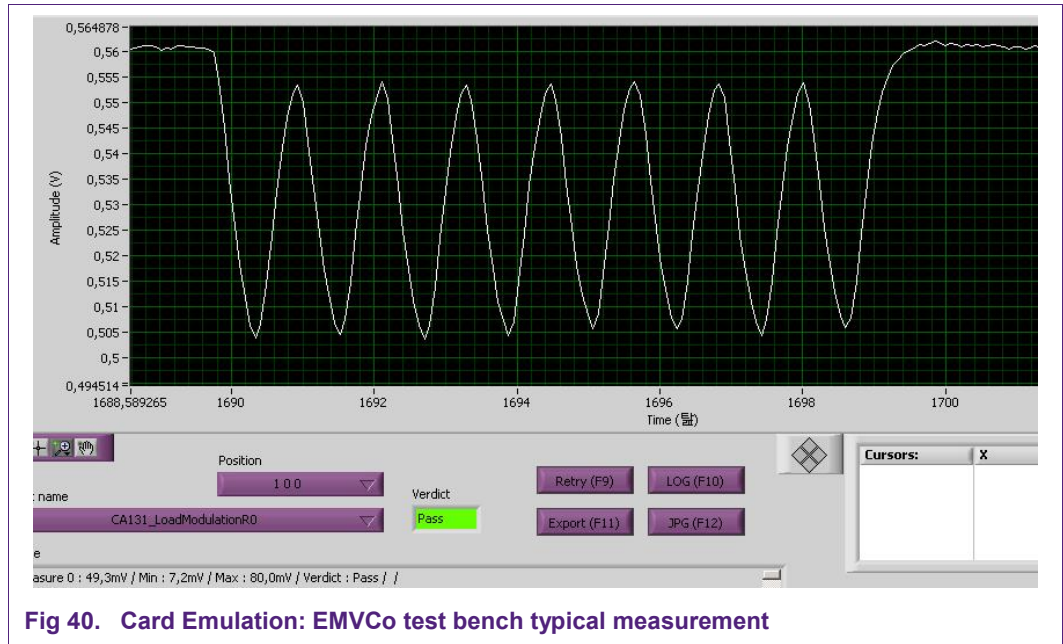


Fig 40. Card Emulation: EMVCo test bench typical measurement

The different standards define the amplitude of the load modulation in listen mode at different distances and positions on the antenna.

The load modulation amplitude or sideband level amplitudes have to be measured by using a specific test bench which is different for each standard (ISO, EMVCo, NFC Forum).

a. How to check the LMA on different test benches using an oscilloscope

If you do not have a certified test bench to test the load modulation, you can use an oscilloscope + the reference antennas for the standard connected to a NFC reader emulator.

The procedure will be the following:

- 1) Connect the output of the reference PCD to the oscilloscope.
- 2) Send a request using the requested power level.
- 3) Capture at least 7 cycles of the subcarrier load modulation response
- 4) Using cursors, measure the amplitude peak to peak of the response ("subcarrier")
- 5) The LMA measured must be inside minimum and maximum limits

Table 6. Load modulation HW for LMA test

Parameter	EMV Co	NFC Forum	„ISO“
Antenna	Test PCD	Poller 0,3,6	Test PCD assembly
Output	J2	J2	Bridge*

Parameter	EMV Co	NFC Forum	„ISO“
Input	J1	J1	RF IN

* Bridge corresponds to the output of the load modulation test circuit

5.2.2.2 Reception test

The performance verification of the PN7150 application can be finalized by some functional checks in CARD mode.

We suggest checking the communication distance with some reader, such as:

- Pegoda
- Omnikey 5321
- ACR122

Additionally, using an oscilloscope and a spy coil between the card and the reader it is possible to check if the communication did not occur because of the reader reception or card reception.

How to check if the problem is from the card or the reader:

- If you can see the command from the reader but there is no response from the card. This is probably a card reception problem.
- After a response from the card the reader does not send the next expected command. This is probably a reader reception problem.

If you identify one of these situations, the RX path must be measured on the FAIL situation. If the signal is correct, the problem can come from other layers, digital and so on.

Additionally, you can use a RF spy from a test tool provider, to be able to check this point.

5.3 Fine tuning through registers

In addition to the matching methodology, the RF performance can eventually be fine-tuned by the mean of registers which are accessible from the PN7150 host interface.

5.3.1 Register setting command

Please refer to the *PN7150 User Manual* [5] contactless configuration chapter to get more insight on the values and addresses of the registers, especially about the related NCI command TLV structure.

The RF_TRANSITION_CFG parameter which allows configuring the CLIF registers is different from the above structure since there must be transitions to take into account, as soon as a parameter is valid for different modes (e.g. reader and card) while its value can be different.

The extension of the TLV structure is given as below:

- The Tag Address is always 0xA0 0D
- The Length can be L=3, 4 or 6
- The Value is actually a secondary data area with a transition ID, the CLIF register offset (equivalent to an address), and the actual value.

Tag (2 Bytes)	Length (1 Byte)	Value (3, 4 or 5 Bytes, depending on the transition ID)		
0xA0 0D	0x03	Transition ID (1 Byte)	CLIF register offset (1 Byte)	1-Byte reg. value
	0x04			2-Byte reg. value
	0x06			4-Byte reg. value

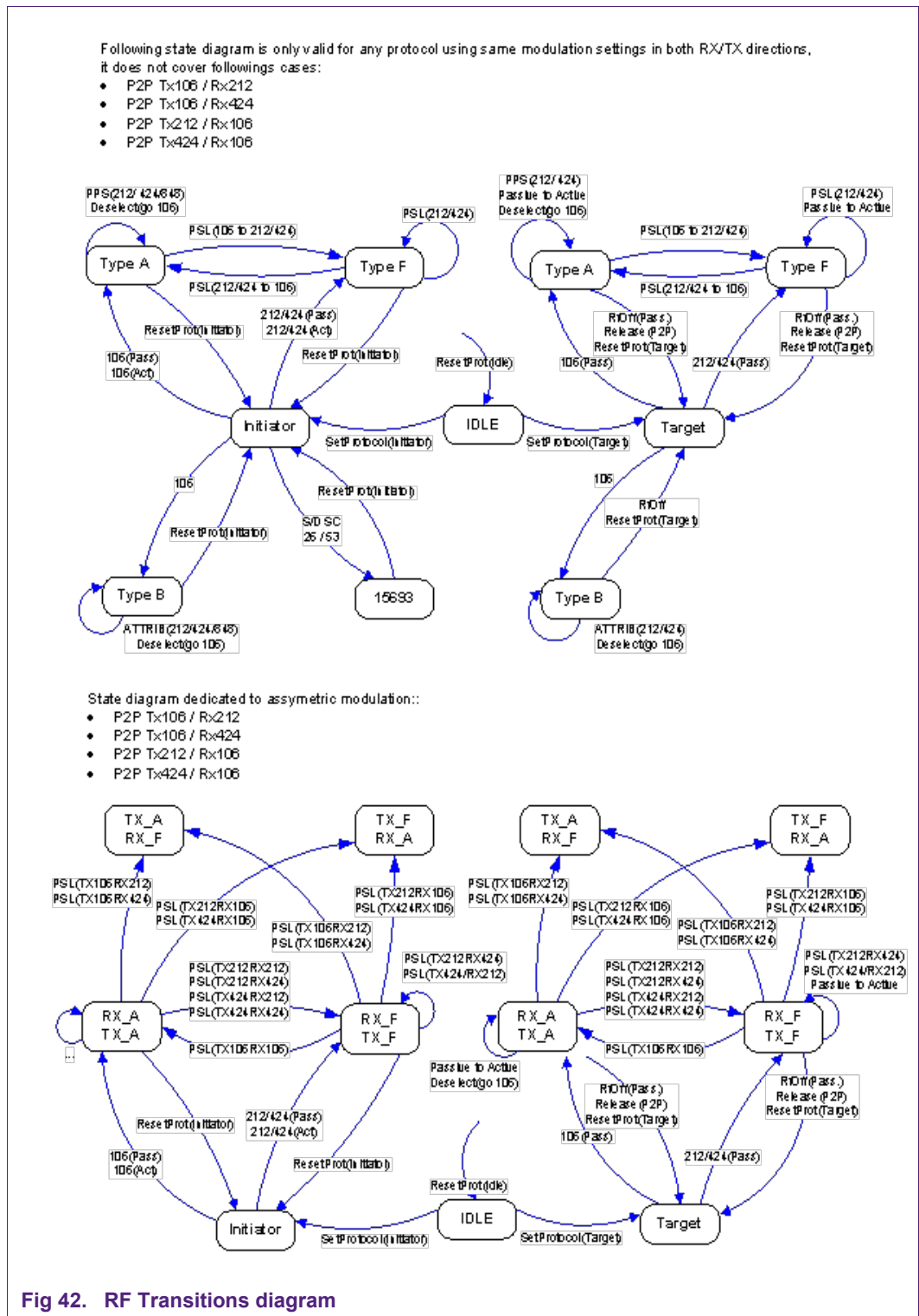
Fig 41. PN7150 CLIF NCI Structure

Basically, depending on the polling loop events, the transition ID corresponds to a set of transitions applied in the registers.

The transition ID depends on

- IN vs. OUT
 - o In each IN transition a set of CLIF registers is loaded out of the EEPROM
 - o In each OUT transition the settings are reverted
- Initiator vs. Target
- TX vs. RX
- Technology (A, B, F, etc.)
- Baud rate (106kb/s etc.)

A simplified view of the different transition IDs is depicted in the figure below. It does not include asymmetric data rates for instance.



Basically, PN7150 goes to one state or another, but cannot jump to a state where no link is defined, which makes the solution more robust. The transitions are defined as below:

- BOOT
 - o Called at boot time
 - o Basic initialization of CLIF (e.g. SMU_ANA_TX_STANDBY_REG)
- INITIATOR
 - o Called at the beginning of the reader phase
 - o Initialization common Reader/Initiator mode settings
- TARGET
 - o Called when external field is detected and CE/P2P Target is active
 - o Initialization of common CE/Target mode settings
- TECHNO_I_RX_X, TECHNO_I_TX_X, TECHNO_T_RX_X, TECHNO_T_TX_X
 - o Initialization of common technology dependent settings for transmitter and receiver
- BR_XXX
 - o Initialization of bit rate specific settings for transmitter and receiver for all different technologies / modes

The exhaustive list of transitions IDs is given as below.

Table 7. PN7150 Transition ID values

Name	ID
RF_CLIF_CFG_BOOT	00
RF_CLIF_CFG_INITIATOR	04
RF_CLIF_CFG_TARGET	06
RF_CLIF_CFG_I_ACTIVE	0A
RF_CLIF_CFG_T_PASSIVE	0C
RF_CLIF_CFG_TECHNO_I_TX15693	20
RF_CLIF_CFG_TECHNO_I_RX15693	22
RF_CLIF_CFG_TECHNO_T_TXA_P	24
RF_CLIF_CFG_BR_106_I_TXA	32
RF_CLIF_CFG_BR_106_I_RXA_P	34
RF_CLIF_CFG_BR_212_I_TXA	38
RF_CLIF_CFG_BR_212_I_RXA	3A
RF_CLIF_CFG_BR_424_I_TXA	3C
RF_CLIF_CFG_BR_424_I_RXA	3E
RF_CLIF_CFG_BR_848_I_TXA	40
RF_CLIF_CFG_BR_848_I_RXA	42
RF_CLIF_CFG_BR_106_I_TXB	44
RF_CLIF_CFG_BR_106_I_RXB	46

Name	ID
RF_CLIF_CFG_BR_212_I_TXB	48
RF_CLIF_CFG_BR_212_I_RXB	4A
RF_CLIF_CFG_BR_424_I_TXB	4C
RF_CLIF_CFG_BR_424_I_RXB	4E
RF_CLIF_CFG_BR_848_I_TXB	50
RF_CLIF_CFG_BR_848_I_RXB	52
RF_CLIF_CFG_BR_212_I_TXF	54
RF_CLIF_CFG_BR_212_I_RXF_P	56
RF_CLIF_CFG_BR_424_I_TXF	5A
RF_CLIF_CFG_BR_424_I_RXF_P	5C
RF_CLIF_CFG_GTM_B	98
RF_CLIF_CFG_GTM_FELICA	9A

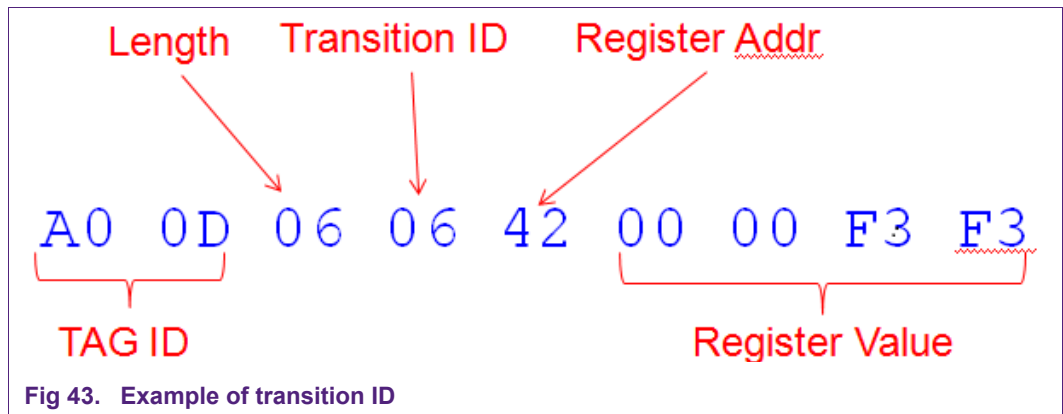
The registers can be one to 4 Bytes long.

As an example, the figure below shows the *CLIF_ANA_TX_AMPLITUDE_REG* register in transition *RF_CLIF_CFG_TARGET* to 0xF3F30000

Note that the byte order for the register value is defined as Little Endian, meaning LSByte written first (LSB to MSB).

The order of the different bytes is given as follows (32 bits):

[7:4] [3:0] [15:12] [11:8] [23:20] [19:16] [31:28] [27:24]



5.3.2 Main Registers for Card and Reader modes

All PN7150 registers are loaded with default values. As a first step some basic registers can be adjusted according to the specific application for CARD mode or READER mode.

Table 8. Card/Listener mode registers

Description	Register Name	Transition ID	Type	NCI command (default value)
RF Tx carrier amplitude	CLIF_ANA_TX_AMPLITUDE_REG	RF_CLIF_CFG_TARGET	ALL	A0 0D 06 06 42 00 02 FF FF
RF level	CLIF_ANA_NFCLD_REG	RF_CLIF_CFG_BOOT	ALL	A0 0D 03 00 40 01
FDT	CLIF_TRANSCEIVE_CONTROL_REG	RF_CLIF_CFG_TARGET	ALL	A0 0D 06 06 03 00 6D 00 20
ADC Config	CLIF_SIGPRO_ADCBCM_THRESHOLD_REG	RF_CLIF_CFG_TARGET	ALL	A0 0D 06 06 30 C8 00 64 00

Table 9. Reader/Poller mode registers

Description	Register Name	Transition ID	Type	NCI command
Rx resistor	CLIF_AGC_INPUT_REG	RF_CLIF_CFG_INITIATOR	ALL	A0 0D 06 04 35 F4 01 F4 01
AGC Config	CLIF_AGC_CONFIG0_REG	RF_CLIF_CFG_I_ACTIVE	ALL	A0 0D 06 0A 33 0F 01 00 70
		RF_CLIF_CFG_BR_106_I_RXA_P	Type A (106)	A0 0D 06 34 33 0F 01 01 70
RF Tx carrier amplitude	CLIF_ANA_TX_AMPLITUDE_REG	RF_CLIF_CFG_BR_106_I_TXA	Type A (106)	A0 0D 06 32 42 F8 10 FF FF
		RF_CLIF_CFG_BR_106_I_TXB	Type B (106)	A0 0D 06 44 42 88 10 FF FF
		RF_CLIF_CFG_BR_212_I_TXF	Type F (212)	A0 0D 06 54 42 88 10 FF FF
		RF_CLIF_CFG_BR_424_I_TXF	Type F (424)	A0 0D 06 5A 42 90 10 FF FF
		RF_CLIF_CFG_TECHNO_I_TX15693	Type 15693	A0 0D 06 20 42 88 10 FF FF
Rx Gain/filter	CLIF_ANA_RX_REG	RF_CLIF_CFG_BR_106_I_RXA_P	Type A (106)	A0 0D 04 34 44 21 00
		RF_CLIF_CFG_BR_106_I_RXB	Type B (106)	A0 0D 04 46 44 26 00
		RF_CLIF_CFG_BR_212_I_RXF_P	Type F (212)	A0 0D 04 56 44 22 00
		RF_CLIF_CFG_BR_424_I_RXF_P	Type F (424)	A0 0D 04 5C 44 26 00
		RF_CLIF_CFG_TECHNO_I_RX15693	Type 15693	A0 0D 04 22 44 22 00
Rx level Threshold (sensitivity)	CLIF_SIGPRO_RM_CONFIG1_REG	RF_CLIF_CFG_BR_106_I_RXA_P	Type A (106)	A0 0D 06 34 2D 24 47 0C 00
		RF_CLIF_CFG_BR_106_I_RXB	Type B (106)	A0 0D 06 46 2D 15 25 0D 00
		RF_CLIF_CFG_BR_212_I_RXF_P	Type F (212)	A0 0D 06 56 2D 05 9E 0C 00
		RF_CLIF_CFG_BR_424_I_RXF_P	Type F (424)	A0 0D 06 5C 2D 05 9E 0C 00
		RF_CLIF_CFG_BR_848_I_RXA	Type A (848)	A0 0D 06 42 2D 15 45 0D 00
RF_CLIF_CFG_TECHNO_I_RX15693	Type 15693	A0 0D 06 22 2D 50 44 0C 00		
Tx signal shape	CLIF_ANA_TX_SHAPE_CONTROL_REG	RF_CLIF_CFG_BR_106_I_TXA	Type A (106)	A0 0D 06 32 4A 33 07 00 08
		RF_CLIF_CFG_BR_212_I_TXA	Type A (212)	A0 0D 06 38 4A 33 07 00 08
		RF_CLIF_CFG_BR_424_I_TXA	Type A (424)	A0 0D 06 3C 4A 52 07 00 1B
		RF_CLIF_CFG_BR_848_I_TXA	Type A (848)	A0 0D 06 40 4A 12 07 00 00
		RF_CLIF_CFG_BR_106_I_TXB	Type B (106)	A0 0D 06 44 4A 21 07 00 07
		RF_CLIF_CFG_BR_212_I_TXB	Type B (212)	A0 0D 06 48 4A 21 07 00 07
		RF_CLIF_CFG_BR_424_I_TXB	Type B (424)	A0 0D 06 4C 4A 21 07 00 07
		RF_CLIF_CFG_BR_848_I_TXB	Type B (848)	A0 0D 06 50 4A 21 07 00 07
		RF_CLIF_CFG_BR_212_I_TXF	Type F (212)	A0 0D 06 54 4A 33 07 01 07
		RF_CLIF_CFG_BR_424_I_TXF	Type F (424)	A0 0D 06 5A 4A 31 07 01 07
RF_CLIF_CFG_TECHNO_I_TX15693	Type 15693	A0 0D 06 20 4A 00 00 00 00		

5.4 Card Mode

5.4.1 Configuring registers in Card Mode

The following registers improve the card emulation mode performance in type A B and F by influencing the load modulation amplitude (LMA) and the sidebands levels on the TX signal path.

This tuning by registers must ensure a correct operation and interoperability between PCD and PICC products. Performance for high distance communication (Low field strength) must be checked against readers like Pegoda and payment readers.

In addition to the readers the following test benches shall be used to get the best performance:

- 1- EMVCo test bench to define minimum functionality for PICC and PCD usage vs. RF powering frames timings Type A Type B commands.
- 2- ISO test bench to verify the operation of a PICC vs. ISO/IEC 14443-2 and ensures independency vs. coupling effect.

5.4.1.1 CLIF_ANA_CLK_MAN_REG

a. Register definition

CLIF_ANA_CLK_MAN_REG is the first parameter to configure in order to adjust the DLL clock phase offset between the RX and TX paths (See table and figure below).

Based on the clock offset the signal emitted at the antenna is in phase or out of phase with the emitted field from the reader. Its impact on the amplitude of the reader field is important and can drastically impact the corresponding load modulation.

CLIF_ANA_CLK_MAN_REG is not set via RF_TRANSITION_CFG parameter (Tag Address is not A0 0D) then it cannot be set using procedure defined in 5.3.1. Instead, usual NCI command CORE_SET_CONFIG_CMD and CORE_GET_CONFIG_CMD must be used. Default value is the following (NCI command form) "A0 1D 11 55 33 14 17 00 AA 85 00 80 55 2A 04 00 63 00 00 00".

Table 10. CLIF_ANA_CLK_MAN_REG register setting for CE

Bit	Symbol	Description
[135:8]	Internal use	Must not be modified
[7:0]	CLOCK_CONFIG_DLL_ALM	Select DLL clock phase

Table 11. Less significant byte values for each phase

Value (hex)	Phase shift
50	0°
51	45°
52	90°
53	135°

Value (hex)	Phase shift
54	180°
55	225°
56	270°
57	315°

b. Schematics providing principle

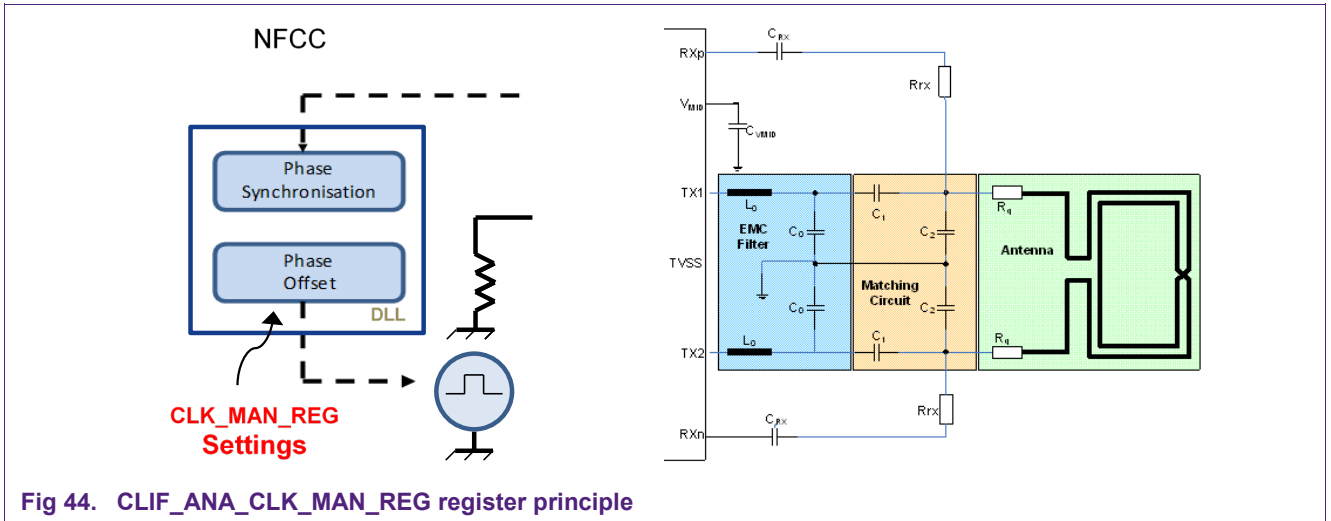


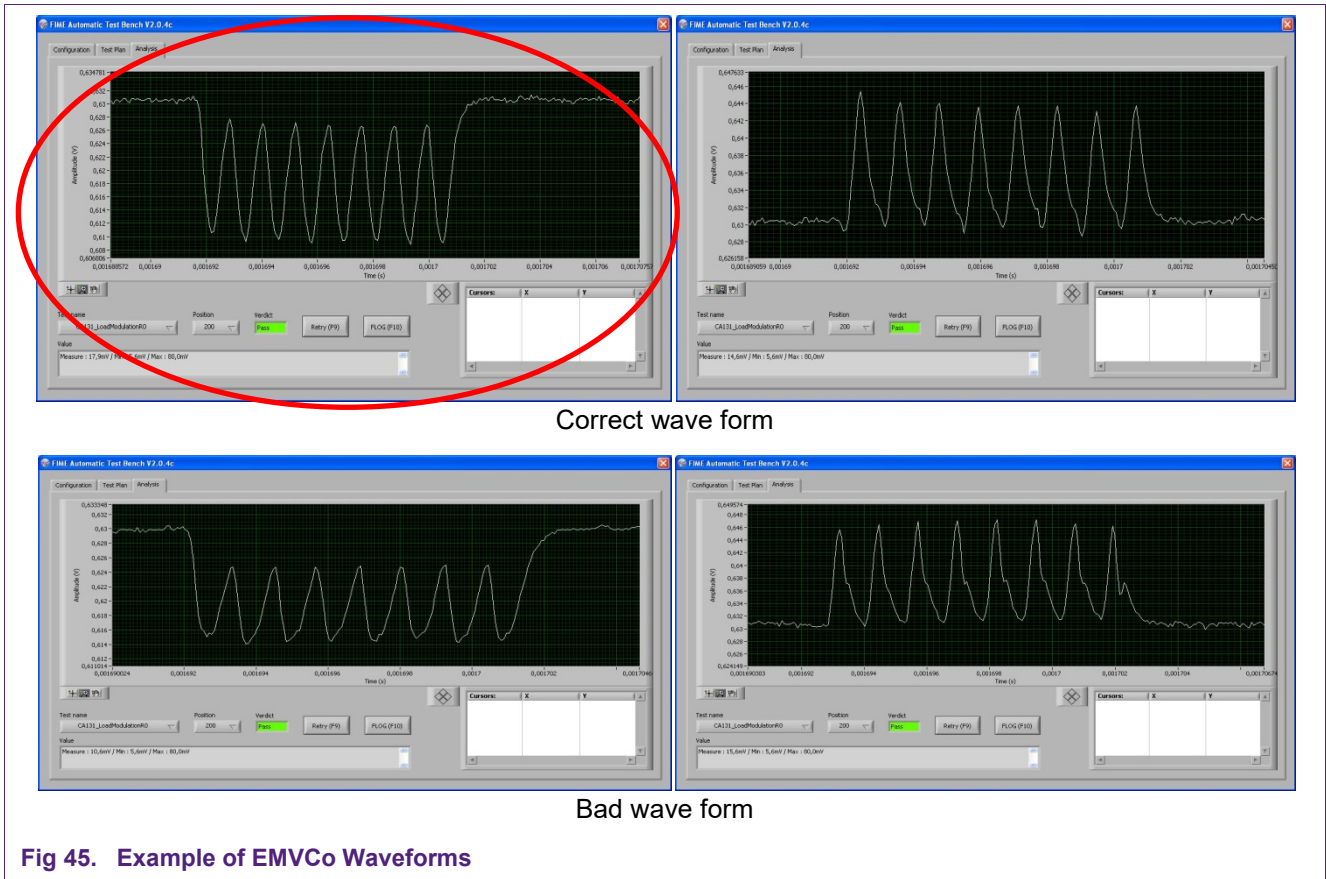
Fig 44. CLIF_ANA_CLK_MAN_REG register principle

c. Register setting procedure

- Parameter: CLOCK_CONFIG_DLL_ALM
- Value range: 50h to 57h
- Measurement process:
 - Run EMVCo CA131 (or NFC Forum 9.1.3.1 Load Modulation amplitude for NFC-A poller 0) test @ 2cm.
 - Get LMA values.
 - Get and check the waveform screenshot.
- Objective:
 - Select clock phase value for which the waveform is the best sine wave.
 - Confirm the optimal setting by using Pegoda (or payment) reader and getting best distance.

d. Measurement example

The graphs below show a selection of measurements done on a reference design. The best sine wave allows selecting the right clock phase.



5.4.1.2 CLIF_ANA_TX_AMPLITUDE_REG

a. Register definition

CLIF_ANA_TX_AMPLITUDE_REG is the second register to configure.

- **[9:8]** (usually called TVDD drop) adjust the load modulation amplitude by choosing the amplitude of the output signal generated at PN7150 TX pin. It is recommended to use the maximum value [00]. Based on these adjustments the load modulation shape can be improved to comply with the targeted standards including interoperability.
- **[27:24] & [19:16]** adjust the N-MOS transistor conductance value applied during non-modulated phases (CW- Continuous Wave) and modulated phase (MOD- Modulation phase) respectively. [0001] means minimum conductance (maximum impedance) and vice versa.

Note that value [0000] shall not be used.

Table 12. CLIF_ANA_TX_AMPLITUDE_REG register setting for CE

Bit	Symbol	Description
[31:28]	Internal use	Must not be modified
[27:24]	TX_GSN_CW_CM	gsn setting @ continuous wave in card mode
[23:20]	Internal use	Must not be modified
[19:16]	TX_GSN_MOD_CM	gsn setting @ modulation in card mode
[15:10]	Internal use	Must not be modified
[9:8]	TX_CW_AMPLITUDE_ALM_CM	Set amplitude of un-modulated carrier @ card mode [00] => Maximum amplitude [01] => Maximum amplitude – typically 150mV [10] => Maximum amplitude – typically 400mV [11] => Maximum amplitude – typically 900mV
[7:0]	Internal use	Must not be modified

b. Register setting procedure

- **Adjusting CW GSN to get optimal field strength from the reader (best sensitivity on RX)**
 - Parameter: TX_GSN_CW_CM
 - Value range: 1h to Fh
 - Measurement process:
 - Run EMVCo CA121 (or NFC Forum 9.1.2.1 Modulation Polling Device to Listening Device at Limit Condition - NFC-A poller 0) test @ 4cm (or 5cm if no proven results)
 - Read distance on Pegoda.
 - Objective:
 - Select the range of CW for which CA121 passes (OK).
 - Get the best CW value which provides the highest distance.

- **Adjusting MOD GSN to get optimal Pegoda distance (optimal LMA on TX).** Keep the best value found in the previous test for CW GSN
 - Parameter: TX_GSN_MOD_CM
 - Value range: 1h, 3h, 9h or Fh
 - Measurement process:
 - Read distance on Pegoda
 - Perform EMVCo test CA131 (or NFC Forum 9.1.3.1 Load Modulation amplitude for NFC-A poller 0) test @ 2 (LMA) and get value.
 - Objective:
 - Get MOD for highest distance and confirm

- Confirm LMA passes for selected MOD value and with 3cm and 4cm.

c. Measurement examples

The “3D” graphs below provide a mapping of reader communication distances and LMA amplitude according to [CWMOD] pairs.

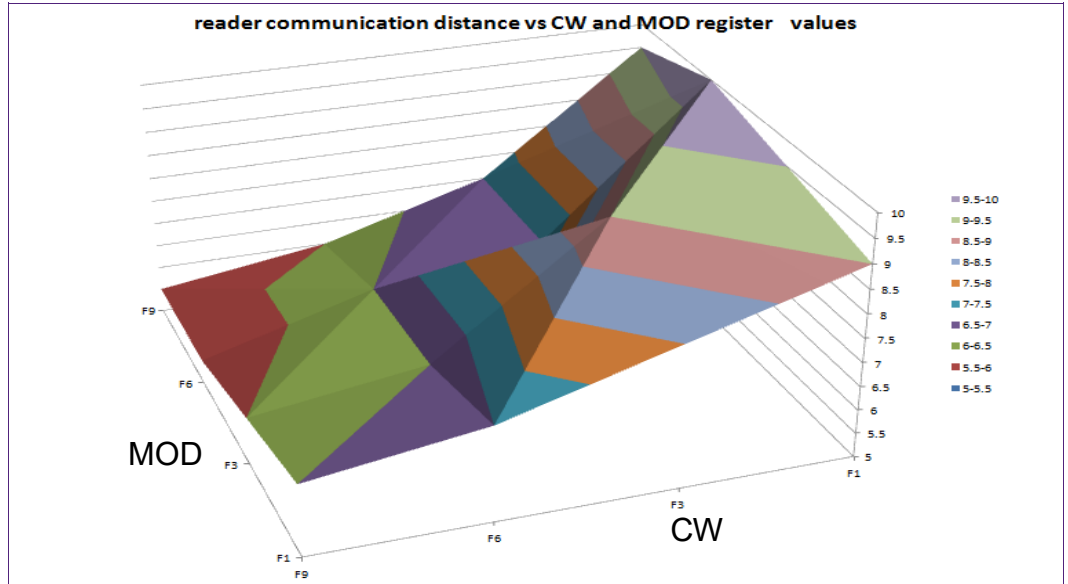


Fig 46. Example of Distance Results

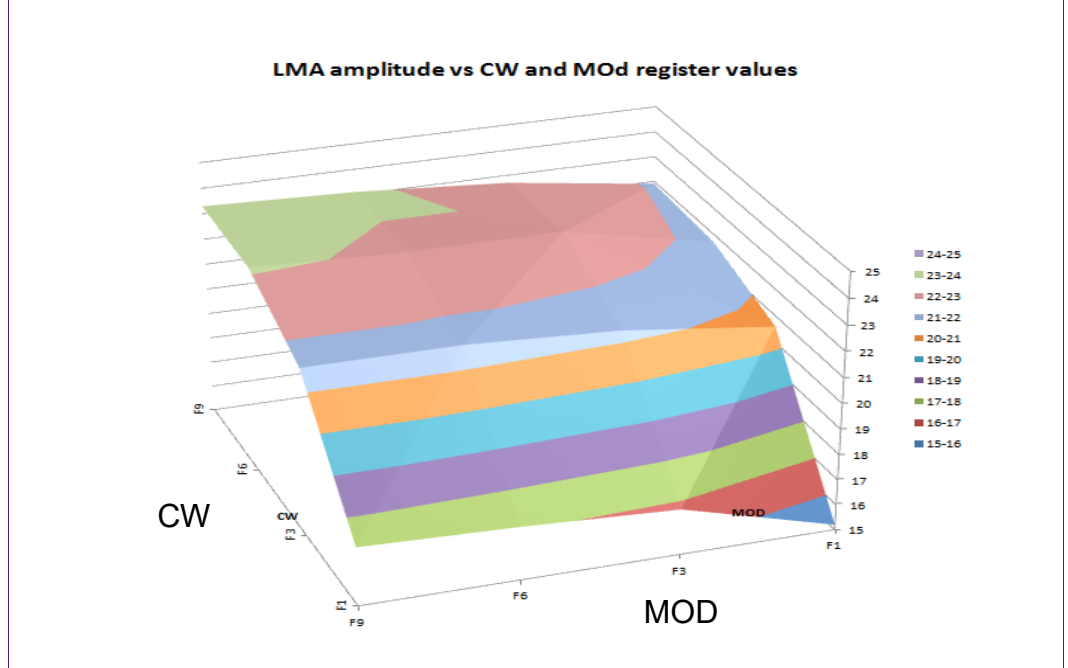


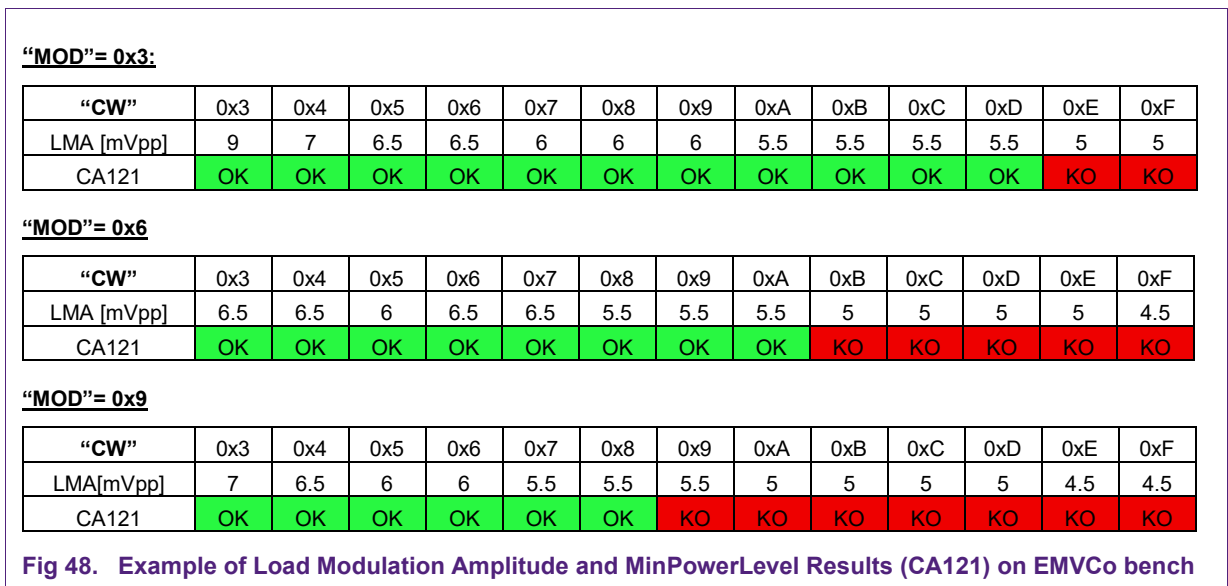
Fig 47. Example of LMA Results

According to these graphs we can notice that:

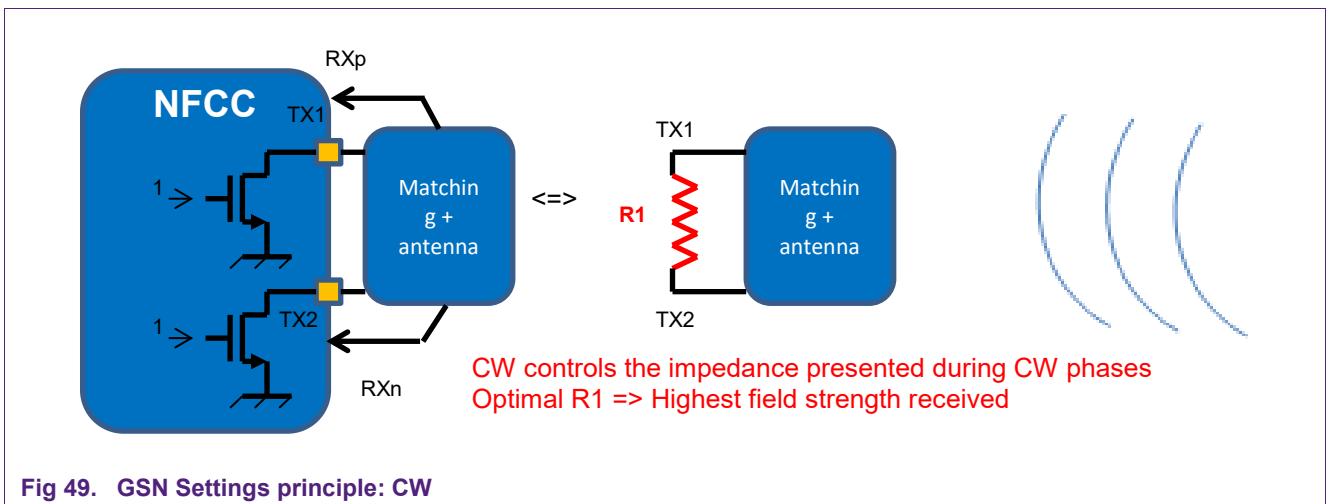
- Best Reader performances are reached for CW=1h to 5h and MOD=5h to 9h
- Best LMA for CW= 3h to 9h and MOD=1h to 9h
- CW=3h to 5h and MOD=5h to 9h seems to be the best range and compromise

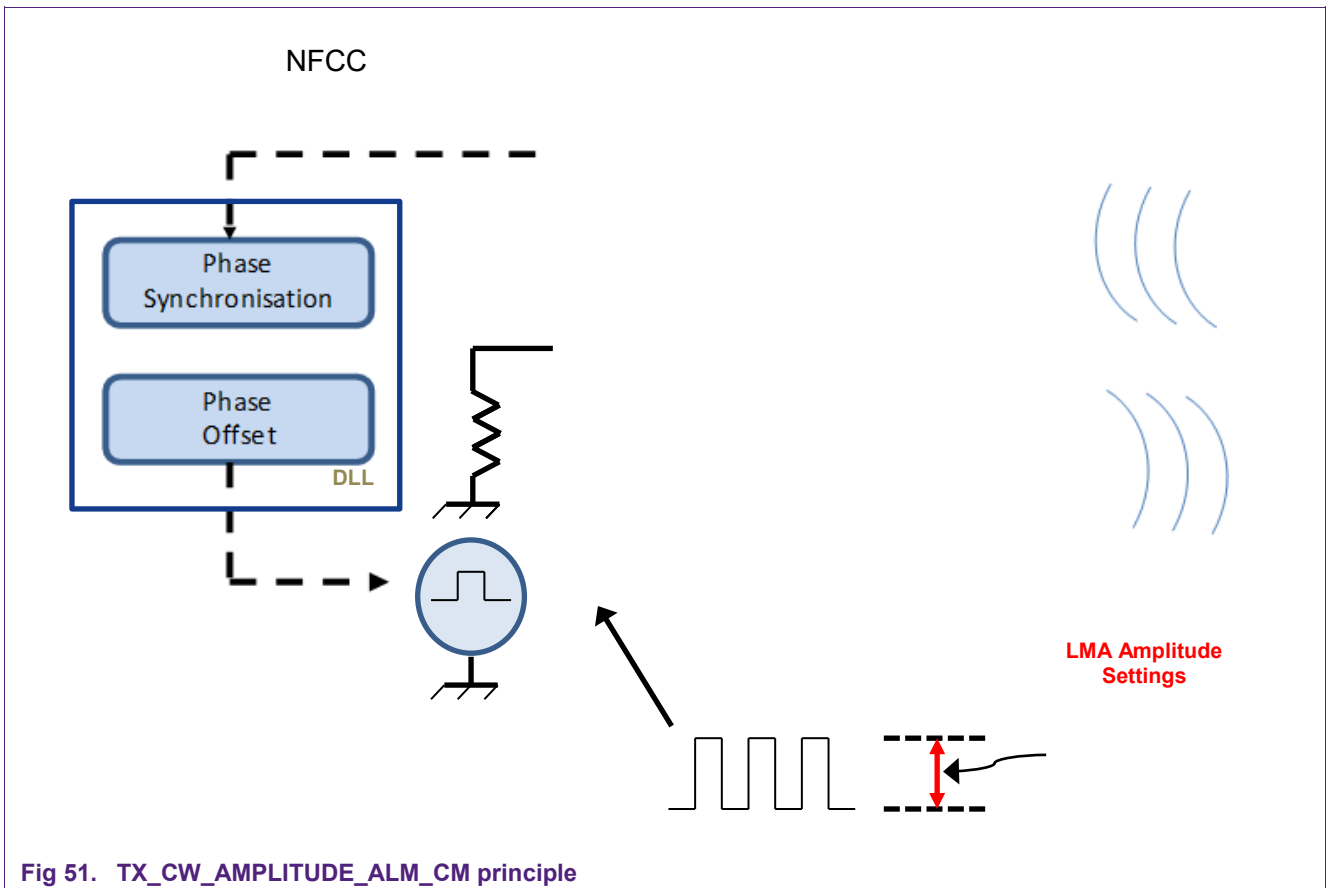
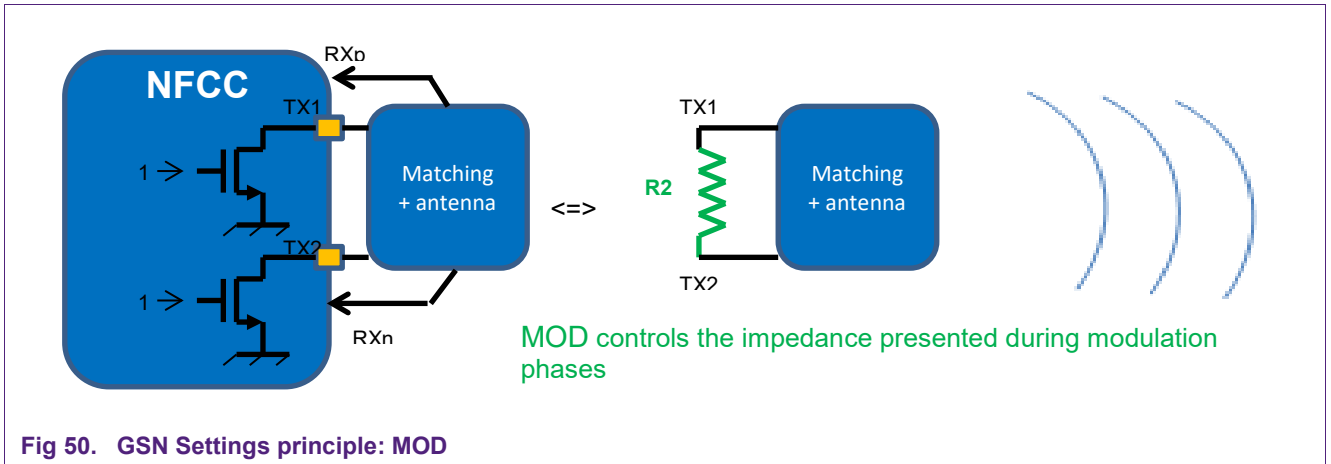
A selection of measurements regarding distance MinPowerLevel and LMA are given below for a certain setup. The best [CW MOD] can be selected accordingly:

[CW MOD] = (16) is a good pair but a range within (16) to (16) can be considered in case of interoperability issues.



d. Schematics illustrating the principle





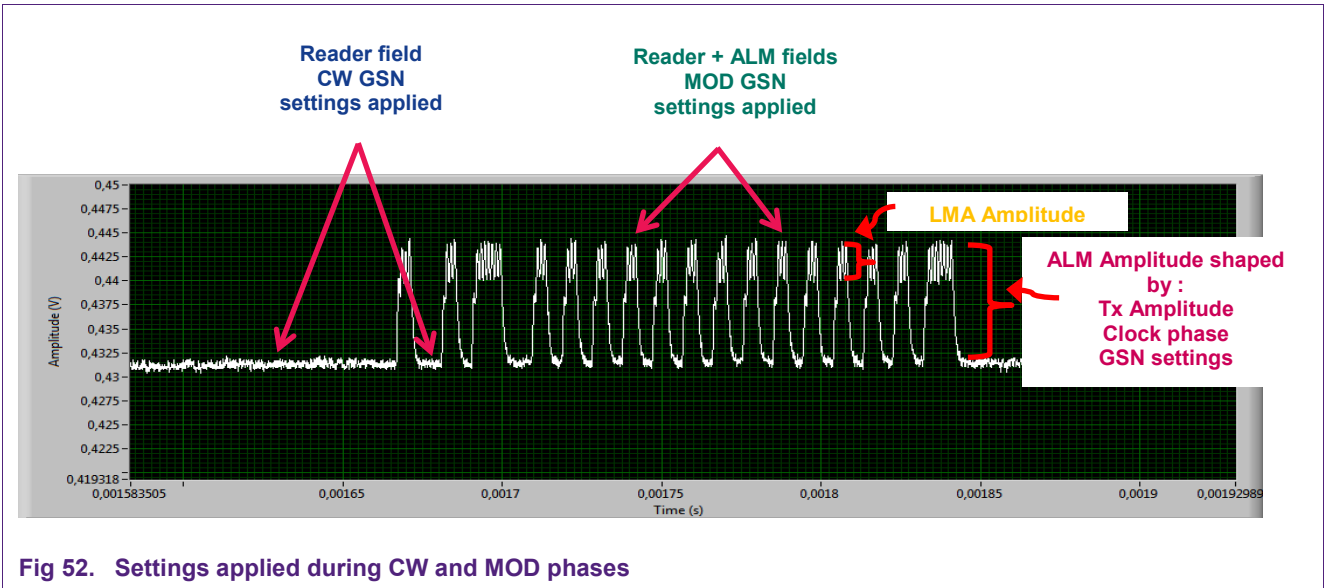


Fig 52. Settings applied during CW and MOD phases

5.4.1.3 CLIF_TRANSCEIVE_CONTROL_REG

a. Register definition

CLIF_TRANSCEIVE_CONTROL_REG can be adjusted to meet FDT requirement.

Table 13. CLIF_TRANSCEIVE_CONTROL_REG register setting for CE

Bit	Symbol	Description
[15:8]	TX_BITPHASE	Defines the number of 13.56 MHz cycles used for adjustment of tx_wait to meet the FDT.
[7:0]	Internal use	Must not be modified

b. Register setting procedure

- Parameter: TX_BITPHASE
- Value range:
 - 00h to FFh.
 - +1 step means a shift of +1/13.56Mhz s on the FDT time
- Measurement process:
Run EMVCo CA144.200 (No analogy with NFC forum test) (FDT value).
- Objective:
The result of the FDT PICC ANTICOLLISION must be between $9\text{etu} + 84/\text{Fc} + 150\text{ns}$ and $9\text{etu} + 84/\text{Fc} + 200\text{ns}$ to achieve the best performances in combination tests (etu = elementary time unit).

5.4.1.4 CLIF_ANA_NFCLD_REG

a. Register definition

CLIF_ANA_NFCLD_REG can be adjusted to define the RF level detector level i.e. the level of the external RF field seen by PN7150. Indeed, in some cases the external RF field might not be fully turned OFF and still detected to be present.

Table 14. CLIF_ANA_NFCLD_REG register setting for CE

Bit	Symbol	Description
[31:4]	Internal use	Must not be modified
[3:0]	CM_RFL_NFC	Programming of detection

b. Register setting procedure

- Parameter: CM_RFL_NFC
- Value range: 0h to Fh
- Measurement process:
 - Start with default value 1h. Make +1 => 0x02 (A0 0D 03 00 40 02) and select only devices which are reliable passing this test (i.e. 5 to 10 consecutive measurements) for the certification. If 0x02 is not sufficient, try 0x03.
 - Run EMVCo CA112.200 (or NFC Forum 9.1.1.12 Power On A poller 0) and CA113.200 (or NFC Forum 9.1.1.12 Power OFF A poller 0) tests.
- Objective:
 Select the value (default value +1 or +2 maximum) that enables to pass the test. If 0x04 or more the overall RF performance of the device might be impacted. For instance, combination results or communication range could be slightly.

5.4.1.5 CLIF_SIGPRO_ADCBCM_THRESHOLD_REG

ADC Based Card Mode thresholds CLIF_SIGPRO_ADCBCM_THRESHOLD_REG register.

Table 15. CLIF_SIGPRO_ADCBCM_THRESHOLD_REG register

Bit	Symbol	Description
[31:29]	Internal use	Must not be modified
[28:16]	EDGE_DETECT_TH	Threshold for the edge decision block of the ADCBCM
[15:13]	Internal use	Must not be modified
[12:0]	BIT_DETECT_TH	Threshold for the "bit" decision block of the ADCBCM

5.5 Reader Mode

5.5.1 Introduction

a. Type A definition

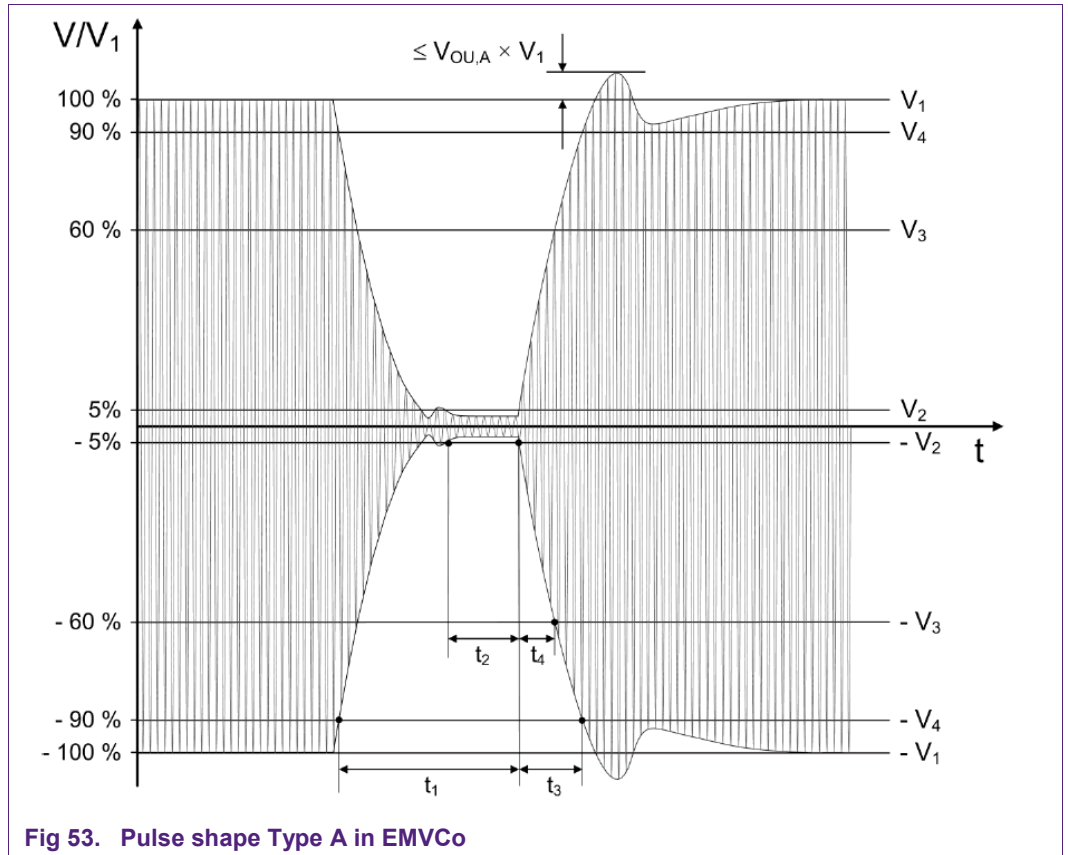


Fig 53. Pulse shape Type A in EMVCo

The time t_1 - t_2 describes the time span in which the signal falls from 90% down below 5% of the signal amplitude.

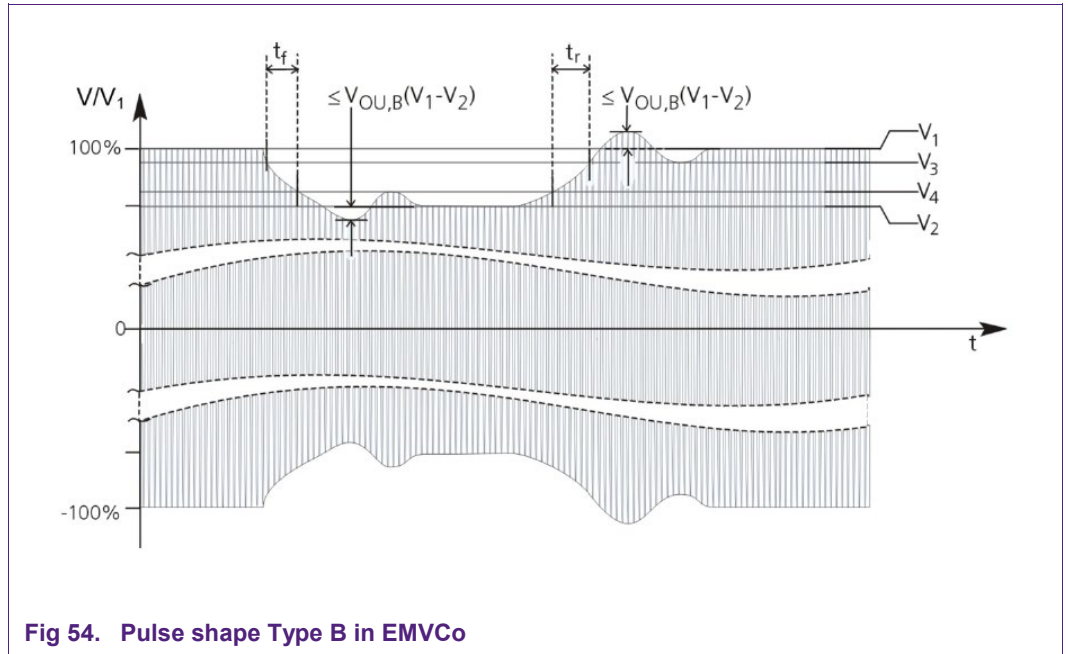
The most critical time concerning rising carrier envelope is t_4 . It must be checked that the carrier envelope at the end of the pause reaches 60% of the continuous wave amplitude within $0.4\mu s$.

Ringing following the falling edge shall remain below $V_{ouA} \times V_1$.

Overshoots immediately following the rising edge shall remain within $(1 \pm V_{ouA}) \times V_1$.

Please refer to [6] (Book D) to get t_1 t_2 t_3 t_4 and V_{ouA} values.

b. Type B definition



V1 is the initial value measured immediately before any modulation is applied by the reader.

V2 is the lower value.

The modulation index (mi) V3 and V4 are defined as follows:

$$mi = (V1-V2)/(V1+V2)$$

$$V3 = V1 - 0.1*(V1-V2)$$

$$V4 = V2 + 0.1*(V1-V2)$$

Please refer to [6] (Book D) to get the values of mi, t_f, t_r and VouB.

5.5.2 Configuring registers in Reader Mode for pulse shape

5.5.2.1 CLIF_ANA_TX_AMPLITUDE_REG

a. Register definition

CLIF_ANA_TX_AMPLITUDE_REG can be set to adjust pulse shape.

[31:28] & [23:20] adjust the N-MOS transistor conductance value applied during non-modulated phases (CW- Continuous Wave) and modulated phase (MOD- Modulation phase) respectively

- **[31:28]**: It is recommended to keep it at its maximum value (F) to get maximum envelop of the carrier amplitude

- **[23:20]**: It plays on the modulation index
- [13:12] & [7:3] adjust the load modulation amplitude by choosing the amplitude of the output signal generated at PN7150 TX pin
- **[13:12]**: It plays on modulation index by degrading CW amplitude
 - **[7:3]**: It plays on the modulation index, the higher the value the higher the modulation index

Table 16. CLIF_ANA_TX_AMPLITUDE_REG register for Reader mode

Bit	Symbol	Description
[31:28]	TX_GSN_CW_RM	gsn setting @ continuous wave in reader mode
[27:24]	Internal use	Must not be modified
[23:20]	TX_GSN_MOD_RM	gsn setting @ modulation in reader mode
[19:14]	Internal use	Must not be modified
[13:12]	TX_CW_AMPLITUDE_RM	Set amplitude of un-modulated carrier @ reader mode
[11:8]	Internal use	Must not be modified
[7:3]	TX_RESIDUAL_CARRIER	Set amplitude of un-modulated carrier
[2:0]	Internal use	Must not be modified

b. Register setting procedure

- Adjusting TX_RESIDUAL_CARRIER

- Parameter: TX_RESIDUAL_CARRIER
- Values: 0h to 1Fh
- Measurement process:
 - Utilize a PICC card and an oscilloscope to observe the LMA and modulation index @ 0cm then 1cm, both must meet the standard
 - Start with medium value (**12h**)
 - Adjust the modulation index by increasing or decreasing the value
- Target:
 - Select value for which modulation index is correct at both distances

If TX_RESIDUAL_CARRIER adjustment is not enough, try TX_CW_AMPLITUDE_RM tuning.

- Adjusting TX_CW_AMPLITUDE_RM

- Parameter: TX_CW_AMPLITUDE_RM
- Values: 0h to 3h
- Measurement process:
 - Use the best value for TX_RESIDUAL_CARRIER obtained previously.

- Use a PICC card and an oscilloscope to observe the LMA @ 0cm then 1cm
 - Start with value 0h then increase the value
 - Objective:
 - Select value for which modulation index is correct
- If TX_CW_AMPLITUDE_RM adjustment is not enough, try TX_GSN_CW_RM & TX_GSN_MOD_RM tuning.

- **Adjusting TX_GSN_CW_RM**
- Parameter: TX_GSN_CW_RM
- Values: 0h to Fh
- Measurement process:
 - Use the best value for TX_RESIDUAL_CARRIER and TX_CW_AMPLITUDE_RM obtained previously.
 - Use a PICC card and an oscilloscope to observe the LMA @ 0cm then 1cm.
 - Start with value Fh then decrease the value
- Target:
 - Select value for which modulation index is correct
- **Adjusting TX_GSN_MOD_RM**
- Parameter: TX_GSN_MOD_RM
- Values: 0h to Fh
- Measurement process:
 - Use the best value for TX_RESIDUAL_CARRIER and TX_CW_AMPLITUDE_RM obtained previously.
 - Use a PICC card and an oscilloscope to observe the LMA @ 0cm then 1cm.
 - Start with value Fh then decrease the value
- Target:
 - Select value for which modulation index is correct

5.5.3 Configuring registers in Reader Mode for Rx path optimization

5.5.3.1 CLIF_ANA_RX_REG

a. Register definition

CLIF_ANA_RX_REG can be fine-tuned to improve the analog down-sampling and baseband amplification of the card response before it is processed by the digital block.

○ **[3:2]: RX_HPCF**

Set the lower corner frequency of the BBA internal band-pass filter to reduce analog demodulation interferences.

- Care:

- If the corner frequency is set too close or above the actual baseband signal frequency the signal strength of the « useful » signal is dampened leading to a loss of reading range but at the same time it can also stabilize the reader performance => Tradeoff might be necessary.
- Furthermore, the RX_HPCF parameter influences the BBA amplification level (gain). The higher the HPCF the lower the gain (1-2dB / per setting).
- For a reliable setting of the HPCF the observation of the frequency spectrum of the BBA input should be available for the given design
=> Since not available each setting has to be evaluated by functional testing

- Value range:

- For 106kbps baseband signals: 00b ... 10b
- For other bitrates baseband signals: 00b ... 11b

○ **[1:0]: RX_GAIN**

Set the amplification level of the **BaseBandAmplifier**

- Care:

The gain must be set in combination with the HPCF parameter taking into account the optimization of the disturbances in the down-mixed RX signal.

- Value range:

- 10b ... 11b High performance & sensitivity for max reading rang:
Strongly depends on the SNR in the system
- 01b ... 10b Typical
- 00b High robustness & stability but low reading range

Table 17. CLIF_ANA_RX_REG register in reader mode

Bit	Symbol	Description
[15:4]	Internal use	Must not be modified
[3:2]	RX_HPCF	Lower Corner Frequency: 00->45kHz 01->85kHz 10->150kHz 11->250kHz
[1:0]	RX_GAIN	Gain Adjustment BBA: 00->33dB

Bit	Symbol	Description
		01->40dB
		10->50dB
		11->57dB

b. Register setting procedure

- Parameter: RX_HPCF
- Values: 0h to 3h
- Measurement process:
 - Use DESFire EV1, MIFARE Ultralight, TOPAZ and measure the reading distances (see annex 1).
- Target:
 - Select settings for which distance is improved.
- Parameter: RX_GAIN
- Values: 0h to 3h
- Measurement process:
 - Use DESFire EV1, MIFARE Ultralight, TOPAZ and measure the reading distances (see annex 1).
- Target:
 - Select settings for which distance is improved.

When the best parameter of CLIF_ANA_RX_REG is found the configuration of CLIF_SIGPRO_RM_CONFIG1_REG can start.

5.5.3.2 CLIF_SIGPRO_RM_CONFIG1_REG

a. Register definition

CLIF_SIGPRO_RM_CONFIG1_REG can be used to tune the digital signal processing regarding the bit and subcarrier detection for the down-sampled and amplified card mode response. The configuration of this register must be done when the best configuration of CLIF_ANA_RX_REG has been found.

- **[15:12]: MIN_LEVEL**
 Defines the threshold for the bit and subcarrier detection based on the amplitude of the correlated I & Q channel signal. It is used for all card mode response types.
- **[11:8]: MIN_LEVEL_P**

Defines the threshold for the phase shift detection based on the amplitude of the correlated I & Q channel. It is used for Type B (all baud rates) and Type A higher baud rates in addition to the Min_Level

For Min_Level and Min_Level_P:

- High value: receiver will be less sensitive but more robust against noise
- Low value: receiver will become sensitive to small card response but also to noise in the system
- Strong dependency on ANA_RX_REG

Care:

- Direct result of a register change is visible after a functional with Target activated
- Since the amplitude of the correlated I&Q channels is evaluated the whole receiver path configuration has a major impact on the final register value (from the RXN/ RXP-pins to the BBA output)

Value range:

- High performance & sensitivity for max. reading range: 2h ... 5h
- Typical: 5h ... 9h
- High robustness & stability but low reading range: 9h ... Fh

○ **[6:5]:**

Defines the required signal strength/threshold of an incorrect modulation for Type A-106kbps meaning the second half bit is also modulated. If the correlated I/Q signal for the un-modulated half bit is above this threshold a collision is detected.

Care:

- The higher the coil level the more robust the system will be but at the same time also less sensitive if it comes to detection of two cards

Value range:

- Typical: 00b ...01b

Table 18. CLIF_SIGPRO_RM_CONFIG1_REG register

Bit	Symbol	Description
[31:16]	Internal use	Must not be modified
[15:12]	MIN_LEVEL	Define the min level of the reception
[11:8]	MIN_LEVEL_P	Define the min level for the phase shift detector unit
[7]	Internal use	Must not be modified
[6:5]	COLL_LEVEL	Defines how strong a signal must be to be interpreted as a collision for Manchester subcarrier communication types

Bit	Symbol	Description
[4:0]	Internal use	Must not be modified

b. Register setting procedure

- Parameter: MIN_LEVEL
- Values: 0h to 3h
- Measurement process:
 - Use DESFire EV1, MIFARE Ultralight, TOPAZ and measure the reading distances (see annex 1).
- Target:
 - Select settings for which distance is improved.
- Parameter: MIN_LEVEL_P
- Values: 0h to 3h
- Measurement process:
 - Use type B and F cards and measure distance (see annex 1).
- Target:
 - Select settings for which distance is improved.

5.5.4 Configuring TX control registers

5.5.4.1 CLIF_ANA_TX_SHAPE_CONTROL_REG

a. Register definition

CLIF_ANA_TX_SHAPE_CONTROL_REG can be used to shape the TX transmission signal in type A by adjusting its rising/falling edge.

Table 19. CLIF_ANA_TX_SHAPE_CONTROL_REG register

Bit	Symbol	Description
[31:17]	Internal use	Must not be modified
[16]	TX_SET_SINGLE_CP_MODE	Enables single charge-pump mode; Allows RC-shaping of modulation waveform
[15:8]	Internal use	Must not be modified
[7:4]	TX_SET_TAU_MOD_FALLING	Transmitter TAU setting for falling edge of modulation shape. In AnalogControl module the output signal is switched with the tx_envelope. Only valid is TX_SET_SINGLE_CP_MODE is set
[3:0]	TX_SET_TAU_MOD_RISING	Transmitter TAU setting for rising edge of modulation shape. In AnalogControl module the

Bit	Symbol	Description
		output signal is switched with the tx_envelope. Only valid is TX_SET_SINGLE_CP_MODE is set

b. Register setting procedure

- Parameter: TX_SET_TAU_MOD_RISING, TX_SET_TAU_MOD_FALLING and TX_SET_SINGLE_CP_MODE
- Values: 0h to Fh
- Measurement process:
 - Use oscilloscope and zoom as depicted in the picture below.
- Objective:
 - Select settings for which the timing meets the specification.
 - 0h value means faster rising and falling edges (potential overshoot/undershoot issue).
 - Fh value means smoother rising and falling edges.

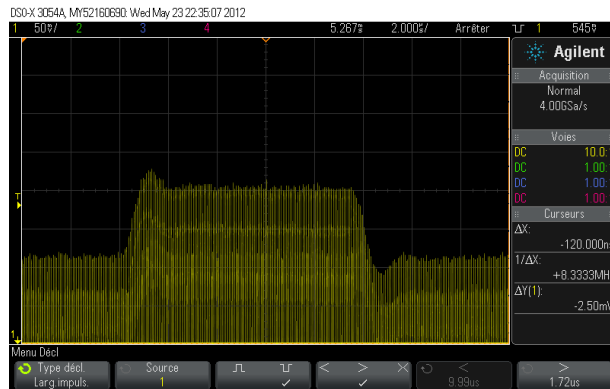


Fig 55. CLIF_ANA_TX_SHAPE_CONTROL_REG type B rising/falling edges illustration with [7:0]=0x00

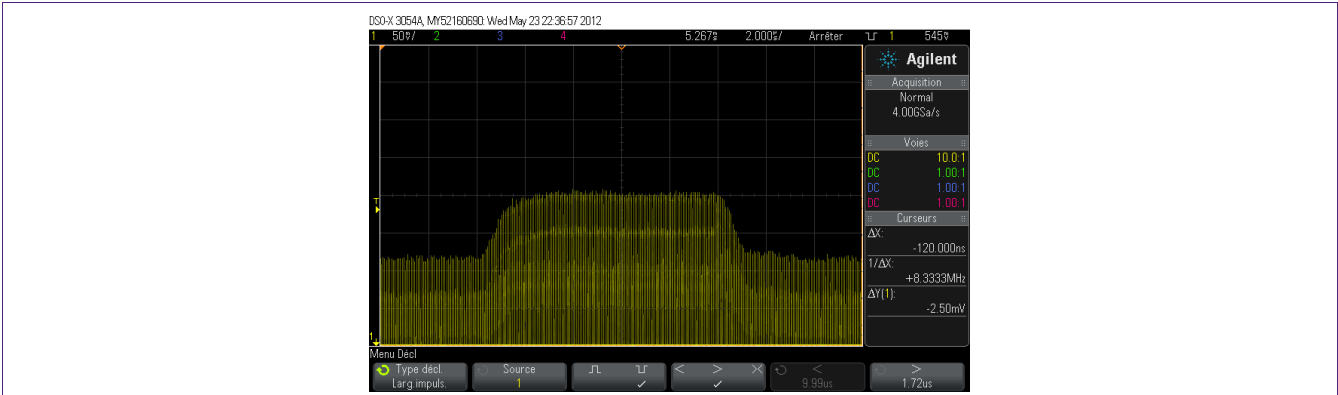


Fig 56. CLIF_ANA_TX_SHAPE_CONTROL_REG type B rising/falling edge illustration with [7:0]=0xFF

5.5.5 Configuring TX control

5.5.5.1 CLIF_TX_OVERSHOOT_CONFIG_REG

CLIF_TX_OVERSHOOT_CONFIG_REG can be adjusted to protect transmission against overshoot.

Table 20. CLIF_TX_OVERSHOOT_CONFIG_REG register

Bit	Symbol	Description
[31:16]	TX_OVERSHOOT_PATTERN	Overshoot pattern which is transmitted after each rising edge
[15:5]	Internal use	Must not be modified
[4:1]	TX_OVERSHOOT_PATTERN_LEN	Defines length of the overshoot prevention pattern (value +1). The pattern is applied starting from the MSB of the defined pattern, all other bits are ignored
[0]	TX_OVERSHOOT_PROT_ENABLE	If set to 1, the overshoot protection is enabled

5.5.5.2 CLIF_TX_UNDERSHOOT_CONFIG_REG

CLIF_TX_UNDERSHOOT_CONFIG_REG can be adjusted to protect transmission against undershoot.

Table 21. CLIF_TX_UNDERSHOOT_CONFIG_REG register

Bit	Symbol	Description
[31:16]	TX_UNDERSHOOT_PATTERN	Undershoot pattern which is transmitted after each rising edge
[15:5]	Internal use	Must not be modified
[4:1]	TX_UNDERSHOOT_PATTERN_LEN	Defines length of the undershoot prevention pattern (value +1). The pattern is applied

Bit	Symbol	Description
		starting from the MSB of the defined pattern, all other bits are ignored
[0]	TX_UNDERSHOOT_PROT_ENABLE	If set to 1, the undershoot protection is enabled

5.5.6 Configuring AGC

5.5.6.1 CLIF_AGC_INPUT_REG

Rx resistor can be adjusted via CLIF_AGC_INPUT_REG register.

Table 22. CLIF_AGC_INPUT_REG register

Bit	Symbol	Description
[31:26]	Internal use	Must not be modified
[25:16]	AGC_RM_VALUE	Static AGC value used for reader mode, value 0 defining the largest Rx resistor (Most sensitive)
[15:9]	Internal use	Must not be modified

5.5.6.2 CLIF_AGC_CONFIG0_REG

AGC is configured via CLIF_AGC_CONFIG0_REG register.

Table 23. CLIF_AGC_CONFIG0_REG register

Bit	Symbol	Description
[31:24]	Internal use	Must not be modified
[23:15]	AGC_THRESHOLD	Defines the threshold value for the AGC, must not be larger than $(AGC_TIME_CONSTANT \gg 1) - 1$
[14:5]	AGC_TIME_CONSTANT	Time constant for the AGC update, period is given by $(AGC_TIME_CONSTANT + 1) * 13.56MHz$
[4]	Internal use	Must not be modified
[3]	AGC_INPUT_SEL	Selects the AGC value to be loaded into the AGC and the source for manual mode, if set RM value is used, else CM value is used
[2]	AGC_LOAD	If set, one AGC control value is loaded from CLIF_AGC_INPUT_REG into the internal AGC register
[1]	AGC_MODE_SEL	Selects the operation mode of the AGC, if set Rx-Divider is controlled by the AGC, else it is controlled by CLIF_AGC_INPUT_REG value
[0]	AGC_MODE_ENABLE	If set, the AGC is enabled. If not set, the Rx-Divider is controlled by either the internal AGC register or a register value (dependent on AGC_MODE_SEL).

6. Reference design

The PN7150 have been widely tested and validated with below described single loop antenna.

6.1.1 Antenna reference

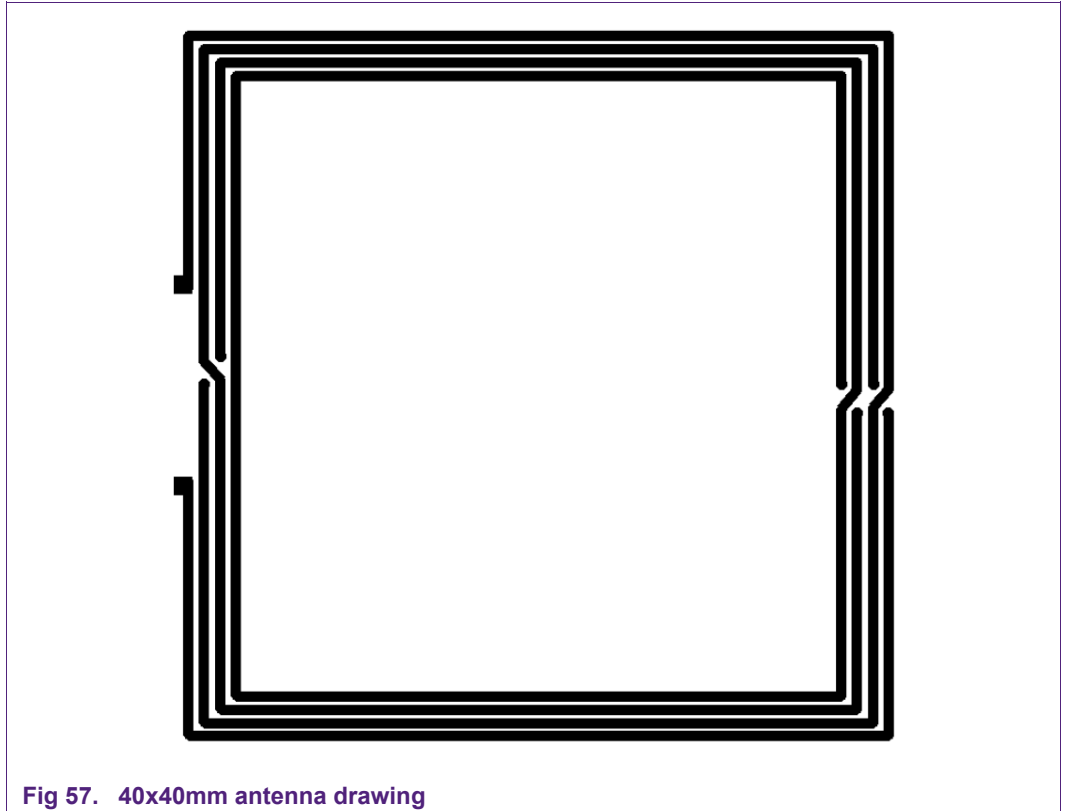


Fig 57. 40x40mm antenna drawing

Table 24. 40x40mm Antenna outlines

Physical outlines of the antenna board are shown here

Description	Value	Unit
size	40 x40	mm
# turns	4	
Copper width	0.4	mm
Spacing	0.3	mm
Copper height	35	µm

This antenna is tested in open air environment (no ferrite or metal sheet below).

The expected antenna performances are given in *Table 25*:

Table 25. 40x40mm Antenna expected performances

Tested Item	Expected performances
Detection distance with a MIFARE Ultralight ID1 PICC (antenna center aligned)	35 cm
NFC Forum reader compliance	Full compliance expected for PN7150
Sideband amplitude measured on an ISO10373-6 assembly PCD bench	Full compliance from 1.5A/m to 7.5A/m
Load modulation amplitude measured on an EMVCo 2.2 bench	Full compliance up to 4cm in the whole EMVCo operating volume
Detection distance with a Pegoda reader v1 (antenna center aligned)	75 cm

6.1.2 Recommended characteristics

In case you want to design your own single loop antenna for the PN7150 it is recommended to respect the below described characteristics:

Table 26. Recommended standard coil antenna physical characteristics

Description	Min	Max
Size	500 mm ²	5000 mm ²
# turns	2	8
Copper width	0.2mm	2mm
Spacing	0.2mm	2mm
Copper thickness	20µm	

7. References

- [1] ISO/IEC10373-6 standard – Identification cards – Test methods – Part 6: Proximity cards – 2011 release
- [2] ISO/IEC14443-2 standard – Identification cards - Contactless integrated circuit(s) cards – Proximity cards – 2010 release
- [3] Book D- EMV Contactless Communication Protocol Specification- Version 2.5 February 2013
- [4] NFC Forum – NFC Analog Specification - 2012 release
- [5] UM10936 - PN7150 User Manual

8. Abbreviations

Abbr.	Meaning
A/m	Amper per meter (magnetic field strength measurement unit)
AGC	Automated Gain Control
AN	Application Note
CH1 / CH2	Channel 1 / Channel 2
EMC	ElectroMagnetic Compatibility
Hmin / Hmax	Minimal and Maximum magnetic field strength
H-field	Magnetic field
IC	Integrated Circuit
ISO/IEC	International Standard Organization / International Electrotechnical Community
mA	milli Ampere
MHz	Mega Hertz
NFC	Near Field Communication
NFCC	NFC Controller (i.e. PN7150)
PC	Personal Computer
PCB	Printed Circuit Board
PCD	Proximity Coupling Device (Contactless reader)
PICC	Proximity Integrated Circuit Card (Contactless card)
Q / Q-factor	Quality Factor
RF	Radiofrequency
TBD	To Be Defined
V	Voltage
Vpp	Peak to peak voltage

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