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LPC32xx SDRAM and NOR FLASH boot issue

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Application note

Document information

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Keywords	LPC32x0, LPC32xx, LPC3220, LPC3230, LPC3240, LPC3250, SDRAM, NOR FLASH, boot
Abstract	This application note covers a recommended system design addition for systems that use SDRAM and boot from NOR FLASH.



Revision history

Rev	Date	Description
01	20100427	Initial version.

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1. Introduction

The NXP Semiconductor LPC32x0 32-bit microcontroller was designed for embedded applications requiring high performance and low power consumption. The LPC32x0 is based on the ARM926EJ-S CPU core and offers multiple boot options such as NAND and NOR FLASH devices, SPI FLASH devices, or boot over UART. It also offers multiple memory support options such as static memory devices, a 128 kB or 256 kB internal IRAM, or SDRAM. Static memory, NOR FLASH, and SDRAM devices are handled by the LCP32x0 External Memory Controller (EMC) and share the same external bus signals. NAND FLASH devices and SPI FLASH devices are handled by the NAND bus signals or the SPI bus signals.

In systems that use SDRAM and boot from NOR FLASH, an issue can occur on system reset that will prevent the SDRAM devices from releasing the data bus. This will prevent normal operation of NOR FLASH due to data bus contention and prevent the LPC32x0 from booting correctly. This issue does not impact NAND, SPI, or UART boot methods.

This application note will focus on a simple system design change to correctly restore SDRAM operation to a high impedance bus state on reset so NOR FLASH will boot correctly.

2. SDRAM and NOR boot issue description

This section provides an overview of EMC shared bus operation, SDRAM read and static memory operations, and an explanation of the issue. The overview focuses on the functionality specific to the issue and not the complete functionality of the associated interfaces.

2.1 External Memory Controller

The EMC provides an interface and signaling for various external memory types such as static volatile (RAM) and non-volatile (NOR FLASH) memories and SDRAM. The EMC provides dedicated control signals for the static memory and the SDRAM interfaces, but the address and data bus signals are shared between both memory types.

Because the address and data bus is shared for both memory types, only one memory device can be accessed by the EMC at any time. When a device on the EMC bus is not selected through its control signals, the data outputs for that device are required to be in a high impedance state to prevent multiple devices from driving the shared data bus. If the data bus is driven simultaneously by more than one device, it is in a state of bus contention. When a bus is in contention, the data on that bus is no longer valid. The EMC prevents bus contention issues by allowing only one device on the EMC to use the bus at any one time.

2.1.1 Static memory operation on the EMC

Accesses to static memory require setting the appropriate signals on the address and data busses (in the case of a write) and controlling the static memory control signals.

In a write operation (from the EMC), the data bus is driven along with the address bus and control signals and the write signal is used to latch the data in the external static memory device. The static memory device maintains its data bus in a high impedance input state during a write. The EMC will release the data bus into a high impedance state with the release of the control signals at the end of the write operation.

In a read operation (to the EMC), only the address bus and control signals are driven from the EMC. The EMC maintains a high impedance input state on the data bus and the static memory device drives the data bus. The EMC will then de-assert the control signals and the static memory device returns the data bus to a high impedance state.

Regardless of whether the operation is read or write, no other operations will occur on the data bus until the read or write cycle is complete and the data bus has returned to a high impedance state.

2.1.2 SDRAM data read operations on the EMC

SDRAM data operations are different than static memory data operations in that they occur on a clock edge instead of a control signal state. For a SDRAM read operation, the EMC controller provides a row and column address to the chip and then may read out one or more data values on successive clocks. SDRAM data bursts across the data bus with one data value being sent per clock cycle. If the clock is stopped or the clock enable is de-asserted during this burst read operation, the SDRAM will maintain its current state until the clocks are restored.

2.1.2.1 SDRAM state on system reset

If the SDRAM abruptly loses its clock during operation such as after a reset, it will maintain the state it was in when the clock was lost. In the case of a read operation where the SDRAM is driving the bus, the SDRAM device will continue to drive the bus regardless of the other SDRAM pin states.

To clear the drive condition, the SDRAM device needs a few clocks with the SDRAM clock enable signal active.

2.2 EMC SDRAM clock and clock enable states on reset

After LPC32x0 reset occurs, the LPC32x0 will generate a clock signal on the SDRAM clock pin, but doesn't assert the SDRAM clock enable. Without the clock enable, the SDRAM will maintain its current state.

2.3 SDRAM/NOR FLASH data bus contention on reset

If the LPC32x0 is reset during an SDRAM access, the SDRAM clock and clock enable will be immediately de-asserted. If the de-assertion occurs during the period of time the SDRAM is driving the data bus, the SDRAM will hold that state until the next clock occurs at the SDRAM clock input when the clock enable is active. However, the LPC32x0 won't deliver the clock and clock enables until software actually sets up the EMC state to do this, so the SDRAM will remain in the data assertion state on the data bus while the LPC32x0 tries to boot.

When the chip attempts to load boot code from NOR FLASH after reset, the correct signals are asserted to the NOR FLASH device and the NOR FLASH device places its data on the data bus. But if the SDRAM is still driving the bus, the NOR FLASH device and SDRAM device are in contention and the data will not be read correctly into the LPC32x0. In this situation, the LPC32x0 will fail to boot.

3. Simple hardware workaround

A simple hardware workaround can be used to correct this condition. The workaround circuit disables the LPC32x0 from driving the SDRAM clock enable signal and instead pulls up the SDRAM clock enable signal during the LPC32x0 reset period. The LPC32x0 will begin clocking the SDRAM before the reset period ends. The assertion of the SDRAM clock enable signal, along with normal SDRAM clocking provided by the EMC, will allow the SDRAM device to clear its current state and release the data bus.

This will allow NOR boot to work correctly after reset. This will not effect any other operation of the system using the LPC32x0.

3.1 Circuit workaround for SDRAM abrupt clock loss

The simple circuit shown below can be used to clear the SDRAM state at system reset. This will not change the normal functioning of the LPC32x0 EMC or SDRAM operations. If SDRAM devices are also present on the 2nd SDRAM chip select, a similar circuit will be needed for those devices using EMC_CKE1.

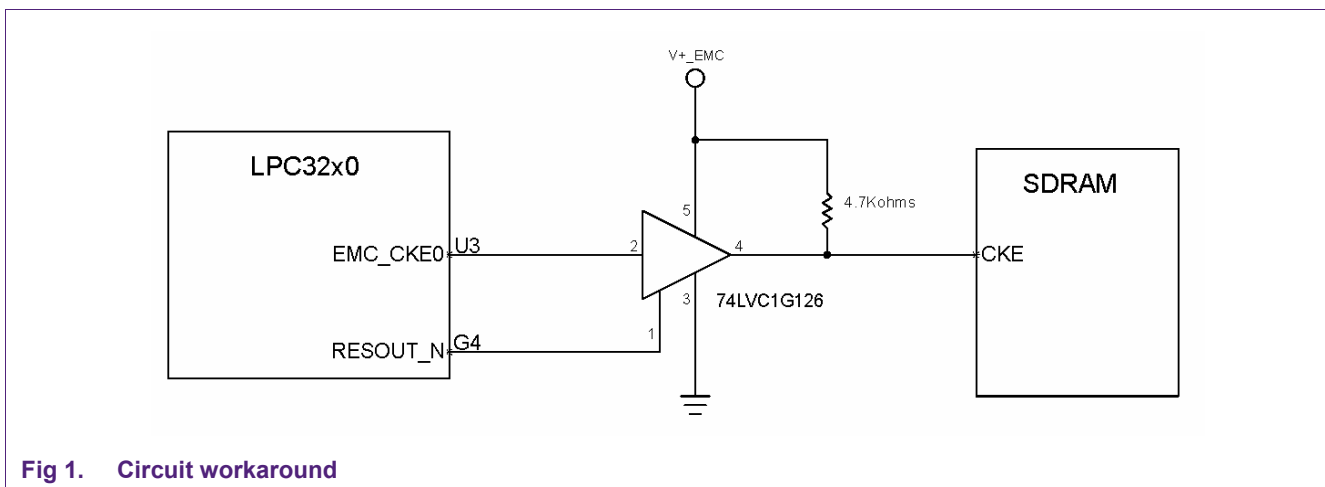


Fig 1. Circuit workaround

3.2 Use of alternate boot methods

Since this issue only occurs with NOR FLASH, using one of the other boot methods is a good workaround for the issue. If NOR FLASH is a requirement, one of the other boot methods can still be used to clear the SDRAM bus contention state in software and then transferring control to the code in NOR FLASH. This requires a small program in NAND or SPI FLASH to clear the SDRAM drive state by enabling the SDRAM clock and clock enable, wait for a few SDRAM clock cycles, and then jumping to the code in NOR FLASH.

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