Low-Voltage Translating 16-Bit I²C-Bus/SMBus I/O Expander

PCAL6416A

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The PCAL6416A is a 16-bit general purpose I/O expander that provides remote I/O expansion for many microcontroller families via the I²C-bus interface.

NXP® I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level to I/O devices operating at a different (usually higher) voltage level. The PCAL6416A has built-in level shifting feature that makes these devices extremely flexible in mixed signal environments where communication between incompatible I/O voltages is required. Its wide VDD range of 1.65 V to 5.5 V on the dual power rail allows seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL6416A: VDD(I²C-bus) and VDD(P). VDD(I²C-bus) provides the supply voltage for the interface at the controller side (for example, a microcontroller) and the VDD(P) provides the supply for core circuits and Port P. The bi-directional voltage level translation in the PCAL6416A is provided through VDD(I²C-bus). VDD(I²C-bus) should be connected to the VDD of the external SCL/SDA lines. This indicates the VDD level of the I²C-bus to the PCAL6416A, while the voltage level on Port P of the PCAL6416A is determined by the VDD(P).

The PCAL6416A contains the PCA6416A register set of four pairs of 8-bit Configuration, Input, Output, and Polarity Inversion registers and additionally, the PCAL6416A has Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs. The PCAL6416A is a pin-to-pin replacement to the PCA6416A, however, the PCAL6416A powers up with all I/O interrupts masked. This mask default allows for a board bring-up free of spurious interrupts at power-up.

At power-on, the I/Os are configured as inputs. However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or

output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.

The system controller can reset the PCAL6416A in the event of a time-out or other improper operation by asserting a LOW in the RESET input. The power-on reset puts the registers in their default state and initializes the I²C-bus/SMBus state machine. The RESET pin causes the same reset/initialization to occur without depowering the part.

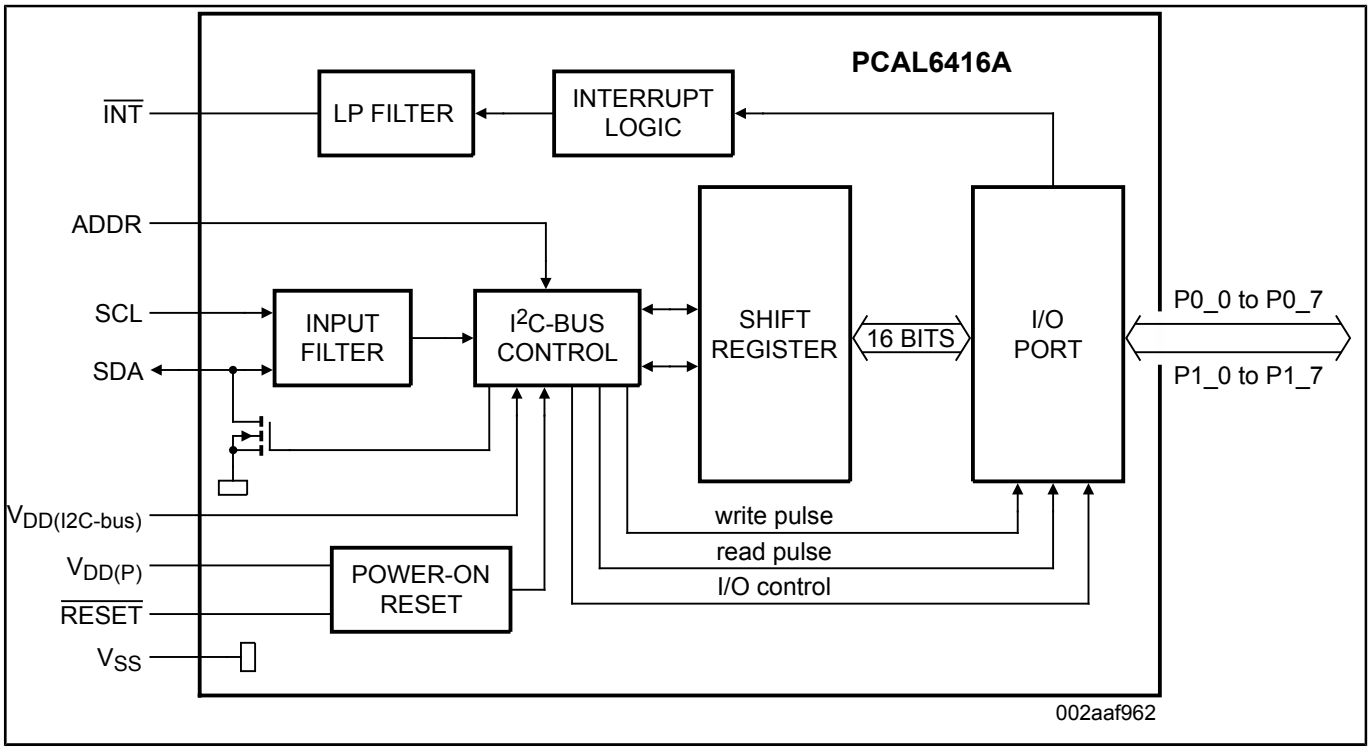
The PCAL6416A open-drain interrupt (INT) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed.

INT can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. Thus, the PCAL6416A can remain a simple target device. The input latch feature holds or latches the input pin state and keeps the logic values that created the interrupt until the controller can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I²C-bus address and allow up to two devices to share the same I²C-bus or SMBus.

PCAL6416A Block Diagram



View additional information for Low-Voltage Translating 16-Bit I²C-Bus/SMBus I/O Expander.

Note: The information on this document is subject to change without notice.
