Mask Set Errata for Mask 1N87M

This report applies to mask 1N87M for these products:

- MKL27Z32Vxx4, MKL27Z64Vxx4
- MKL17Z32Vxx4, MKL17Z64Vxx4

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
e3863	ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage
e8992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
e8010	LLWU: CMP flag in LLWU_Fx register cleared by multiple CMP out toggles when exiting LLSx or VLLSx modes.
e8594	ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM
e8595	ROM: ROM read memory command may read the incorrect data back from flash in some cases
e2580	UART: Start bit sampling not compliant with LIN 2.1 specification

Table 2. Revision History

Revision	Changes
23Jan2015	Errata added:e3863,e8992,e8010,e8594,e8595,e2580

e3863: ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage

Description: In 16-bit differential mode, the ADC may result in a conversion error when the input voltage on the plus-side of the differential pair (DPx) exceeds approximately (VREFH*31/32). Other modes are unaffected.

Workaround: To avoid a conversion error near positive full-scale in this mode, do not allow the input voltage on the plus-side of the differential pair (DPx) to exceed (VREFH*31/32).

e8992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Description: Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

Workaround: There are two workarounds:

1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.

2) Assert NMI signal for longer than 16 bus clock cycles.

e8010: LLWU: CMP flag in LLWU_Fx register cleared by multiple CMP out toggles when exiting LLSx or VLLSx modes.

Description: The comparator's corresponding wakeup flag in the LLWU_Fx register is cleared prematurely if:

1.The CMP output is toggled more than one time during the LLSx wakeup sequence and the comparator's corresponding flag in the LLWU_Fx register is cleared.

Or

2.The CMP output is toggled more than one time during the VLLSx wakeup sequence, PMC_REGSC[ACKISO] is cleared, and the comparator's corresponding flag in the LLWU_Fx register is cleared.

Workaround: When MCU is waking up from LLS, code can implement a software flag to retain the wakeup source, if required by software.

When MCU is waking up from VLLSx, code can implement a software flag prior to clearing PMC_REGSC[ACKISO] to retain the wakeup source, if required by software.

e8594: ROM: I2C0_A1 register does not contain the reset default value when MCU boots from ROM

Description: When the MCU boots from ROM, then the I2C0_A1 register will not hold the reset default value (i.e. 0x00) from the ROM boot.

Workaround: Re-initialize the I2C0_A1 register when booting from ROM and when I2C0 is used by applications.

e8595: ROM: ROM read memory command may read the incorrect data back from flash in some cases

Description: When using the ROM Read Memory command to read the same flash address twice, if in the middle of the two consecutive reads, the flash address space content is changed by either a flash erasing or programming command, the second Read Memory command does not return the correct value in flash, and instead returns the same value as the first read. The root cause is that the flash cache is not disabled and retains the previous content of the flash.

Workaround: Use one of two options:

1) Avoid continuous read of the same flash address space twice

2) Invalidate flash cache before second read of the same flash address

e2580: UART: Start bit sampling not compliant with LIN 2.1 specification

Description: The LIN 2.1 specification states that start bits should be checked at sample 7, 8, 9, and 10. The UART module checks the start bit at samples 3, 5, and 7 instead.

Workaround: Start bits longer than 5/16 of a bit time are guaranteed to be recognized. Start bits shorter than this should not be used with this version of the UART because they might not be recognized.

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