# Mask Set Errata for Mask 1N86B

## Introduction

This report applies to mask 1N86B for these products:

- KINETIS50MHZ

| Errata ID | Errata Title |
|---|---|
| 3863 | ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage |
| 4626 | DMA: DMA loads wrong value into Transfer Control Descriptor when configured for scatter/gather processing. |
| 4588 | DMAMUX: When using PIT with "always enabled" request, DMA request does not deassert correctly |
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| 6573 | JTAG: JTAG TDO function on the PTA2 disables the pull resistor |
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| 3928 | TSI: Delta voltage is 400 mV instead of 600 mV |

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| Errata ID | Errata Title |
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| 3926 | TSI: The TSI will run several scan cycles during reference clock instead of scanning each electrode once |
| 2638 | TSI: The counter registers are not immediately updated after the EOSF bit is set. |
| 4546 | TSI: The counter values reported from TSI increase when in low power modes (LLS, VLLS1, VLLS2, VLLS3) |
| 4181 | TSI: When the overrun flag is set, the TSI scanning sequence will exhibit undefined behavior. |
| 4935 | UART: CEA709.1 features not supported |
| 2582 | UART: Flow control timing issue can result in loss of characters |
| 4945 | UART: ISO-7816 T=1 mode receive data format with a single stop bit is not supported |
| 3892 | UART: ISO-7816 automatic initial character detect feature not working correctly |
| 5928 | USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases |

## e3863: ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage

**Errata type:** Errata

**Description:** In 16-bit differential mode, the ADC may result in a conversion error when the input voltage on the plus-side of the differential pair (DPx) exceeds approximately (VREFH*31/32). Other modes are unaffected.

**Workaround:** To avoid a conversion error near positive full-scale in this mode, do not allow the input voltage on the plus-side of the differential pair (DPx) to exceed (VREFH*31/32).

## e4626: DMA: DMA loads wrong value into Transfer Control Descriptor when configured for scatter/gather processing.

**Errata type:** Errata

**Description:** When DMA scatter/gather feature is enabled it loads a wrong value into Transfer Control Descriptor (TCD) after channel completes a major loop, which causes improper operation of this feature.

**Workaround:** Disable the scatter/gather feature by clearing DMA_TCDn_CSR[ESG] = 0. Scatter/gather feature can be emulated in one of the following ways.

1. Use DMA dynamic channel linking feature. The TCD can be loaded with a new value from memory with the linked DMA channel.

2. Enable DMA DONE interrupt. Configure the DMA Done interrupt to be asserted when a major loop is completed, DMA_TCDn_CSR[INTMAJOR], then in the interrupt service routine copy the 32-byte data structure of the TCD from memory to the current TCD local memory and then start current channel via software.

## e4588: DMAMUX: When using PIT with "always enabled" request, DMA request does not deassert correctly

**Errata type:** Errata

**Description:** The PIT module is not assigned as a stand-alone DMA request source in the DMA request mux. Instead, the PIT is used as the trigger for the DMAMUX periodic trigger mode. If you want to use one of the PIT channels for periodic DMA requests, you would use the periodic trigger mode in conjunction with one of the "always enabled" DMA requests. However, the DMA request does not assert correctly in this case.

Instead of sending a single DMA request every time the PIT expires, the first time the PIT triggers a DMA transfer the "always enabled" source will not negate its request. This results in the DMA request remaining asserted continuously after the first trigger.

**Workaround:** Use of the PIT to trigger DMA channels where the major loop count is greater than one is not recommended. For periodic triggering of DMA requests with major loop counts greater than one, we recommended using another timer module instead of the PIT.

If using the PIT to trigger a DMA channel where the major loop count is set to one, then in order to get the desired periodic triggering, the DMA must do the following in the interrupt service routine for the DMA_DONE interrupt:

1. Set the DMA_TCDn_CSR[DREQ] bit and configure DMAMUX_CHCFGn[ENBL] = 0

2. Then again DMAMUX_CHCFGn[ENBL] = 1, DMASREQ=channel in your DMA DONE interrupt service routine so that "always enabled" source could negate its request then DMA request could be negated.

This will allow the desired periodic triggering to function as expected.

## e2793: I2C: MCU does not wake as expected from STOP or VLPS mode on subsequent address matches if previous address is mismatched

**Errata type:** Errata

**Description:** The I2C module, acting as a slave on the I2C bus, does not wake as expected from normal STOP mode or VLPS mode on a valid address match if the previous address was not a match.

When the external I2C master sends a non-matching address, the I2C slave state machine does not look for a start bit past the first start bit on the bus. Consequently, subsequent transmissions by the I2C master with a matching address do not, on the first matching address, wake the MCU from stop mode or VLPS via the I2C interrupt.

**Workaround:** There are multiple workarounds:

(1) The master must continually re-transmit the MCU's slave address upon not receiving a NACK from the slave device during the slave addressing phase of the transmission. For clarification, the master must perform the following:

a) Send slave device address

b) Check for ACK bit

c) If ACK was received, continue with data transmission. Else, send repeated start signal and repeat steps a-c.

NOTE: Due to the nature of the errata, the maximum number of retransmissions needed to wake the part is nine times.

(2) When the MCU, operating as an I2C slave, is in STOP or VLPS mode: Ensure that the external I2C master sends a matching address to wake the slave MCU before it sends any transaction to other I2C slaves. The user must also ensure that MCU does not return to STOP or VLPS until after all packets to non-matching addresses have been sent.

(3) Use a pin interrupt (any pin, whether that pin is or is not being used by the active I2C module) to wake up the part before receiving I2C packets. NOTE: If using the SDA or SCL pin that the active I2C module is using, the part will wake-up on every I2C transaction on the bus.

(4) Use Wait mode instead of STOP or VLPS mode.

## e6573: JTAG: JTAG TDO function on the PTA2 disables the pull resistor

**Errata type:** Errata

**Description:** The JTAG TDO function on the PTA2 pin disables the pull resistor, but keeps the input buffer enabled. Because the JTAG will tri-state this pin during JTAG reset (or other conditions), this pin will float with the input buffer enabled. If the pin is unconnected in the circuit, there can be increased power consumption in low power modes for some devices.

**Workaround:** Disable JTAG TDO functionality when the JTAG interface is not needed and left floating in a circuit. Modify the PORTA_PCR2 mux before entering low power modes. Set the mux to a pin function other than ALT7. If set up as a digital input and left unconnected in the circuit, then a pull-up or pull-down should be enabled. Alternatively, an external pull device or external source can be added to the pin.

Note: Enabling the pull resistor on the JTAG TDO function violates the JTAG specification.

## e3964: JTAGC: When debug is active a wakeup from STOP or VLPS with interrupt causes a hard fault interrupt.

**Errata type:** Errata

**Description:** When exiting STOP or VLPS back into RUN mode with an interrupt a hard fault interrupt is caused when the JTAG debuger is enabled.

The MCU enters a pseudo STOP mode when the debugger is enabled.

The user cannot use the debugger to test code that wakes up from STOP with an interrupt.

**Workaround:** a. Disable the debugger with a Power off and on cycle before testing code that exits STOP or VLPS with an interrupt.

or

b. From the debugger, while in STOP or VLPS, halt the MCU with the debugger tools before triggering an interrupt.

## e4590: MCG: Transitioning from VLPS to VLPR low power modes while in BLPI clock mode is not supported.

**Errata type:** Errata

**Description:** Transitioning from VLPS mode back to VLPR (LPWUI control bit = 0) while using BLPI clock mode only, is not supported. During Fast IRC startup, the output clock frequency may exceed the maximum VLPR operating frequency. This does not apply to the BLPE clock mode.

**Workaround:** There are two options for workarounds

a) Exit to Run instead of VLPR. Before entering VLPR set the LPWUI bit so that when exiting VLPS mode the MCU exits to RUN mode instead of VLPR mode. With LPWUI set any interrupt will exit VLPR or VLPS back into RUN mode. To minimize the impact of the higher RUN current re-enter VLPR quickly.

or

b) Utilize MCG clock mode BLPE when transitioning from VLPS to VLPR modes.

## e4176: NMI: NMI interrupt service routine (ISR) might not be called when MCU wakes up from VLLSx modes.

**Errata type:** Errata

**Description:** When MCU wakes up from VLLSx modes via NMI pin the NMI ISR might not be called if the NMI pulse width is lower than 120us..

**Workaround:** NMI pulse width must be asserted for at least 120usec to ensure NMI ISR is called and entered. Note that a short NMI pulse will still wakeup the part, and the LLWU ISR will still be entered.

## e6665: Operating requirements: Limitation of the device operating range

**Errata type:** Errata

**Description:** Some devices, when power is applied, may not consistently begin to execute code under certain voltage and temperature conditions. Applications that power up with either VDD >= 2.0 V or temperature >= -20C are not impacted. Entry and exit of low-power modes is not impacted.

**Workaround:** To avoid this unwanted behavior, one or both of these conditions must be met:

a) Perform power on reset of the device with a supply voltage (VDD) equal-to or greater-than 2.0 V , or

b) Perform power on reset of the device at a temperature at or above -20 C.

## e4473: PMC: 1MHz Flash operation in VLPR mode not supported on date code 1202 and earlier.

**Errata type:** Errata

**Description:** Configuring the flash clock for an operating frequency of 1MHz can cause the MCU to generate core lockup resets.

**Workaround:** The flash clock can be configured for a max operating frequency of 500KHz. Note that this does not affect the core clock which can still be configured to operate up to 4MHz.

Note: Device code date markings indicate the week and year of manufacture. The date is coded as four numerical digits, the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “CTZZ1202A" indicates the 2nd week of the year 2012.

## e5666: PMC: Maximum current consumption in VLPR, VLPW, VLPS, LLS and VLLSx modes may be higher than data sheet specification.

**Errata type:** Errata

**Description:** Maximum current consumption in Very Low Power Run (VLPR), Very Low Power Wait (VLPW), Very Low Power Stop (VLPS), Low Leakage Stop (LLS) ,Very Low Leakage Stop3 (VLLS3) ,Very Low Leakage Stop2 (VLLS2) ,Very Low Leakage Stop1 (VLLS1) , and Very Low Leakage Stop0 (VLLS0) modes may exceed data sheet specification.

**Workaround:** This errata has two workarounds:

1. Limit VDD operating voltage to below 2.5 V, or

2. Obtain 3N86B mask set revision, which has fixed this errata.

## e4481: PMC: STOP mode recovery unstable

**Errata type:** Errata

**Description:** Recovery from STOP mode is not guaranteed if STOP mode is used for a period of time longer than 50ms.

**Workaround:** There are two methods that can be used:

1. Set the BGEN bit in the PMC_REGSC register prior to entering STOP mode, and when existing STOP mode clear the BGEN bit.

2. Use a different low power mode such as VLPS.

## e5667: PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes

**Errata type:** Errata

**Description:** The Power Management Controller (PMC) bandgap 1-V reference is not available as an input to the Analog-to-Digital Converter (ADC) module (using ADC input channel AD27) or the Comparator (CMP) module (using CMP input IN6) in Very Low Power Run (VLPR), Very Low Power Wait (VLPW), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), Very Low Leakage Stop3 (VLLS3), Very Low Leakage Stop2 (VLLS2), Very Low Leakage Stop1 (VLLS1), or Very Low Leakage Stop0 (VLLS0) modes.

This erratum does not apply to the VREF module 1.2 V reference voltage.

**Workaround:** Use of the PMC bandgap 1-V reference voltage as an input to the ADC and CMP modules requires the MCU to be in Run, Wait, or Stop modes.

## e4949: Reset and Boot: Device may not exit the power on reset (POR) event correctly with fast ramp-up slew rates.

**Errata type:** Errata

**Description:** Device may not exit the power on reset (POR) event correctly when the Vdd ramp-up slew rate is greater than 17 kV/sec as VDD is raised from 0V to 1.7V.

**Workaround:** Keep instantaneous slew rate of VDD below 17 kV/sec.

Status: This errata will be fixed on future mask sets.

## e5130: SAI: Under certain conditions, the CPU cannot reenter STOP mode via an asynchronous interrupt wakeup event

**Errata type:** Errata

**Description:** If the SAI generates an asynchronous interrupt to wake the core and it attempts to reenter STOP mode, then under certain conditions the STOP mode entry is blocked and the asynchronous interrupt will remain set.

This issue applies to interrupt wakeups due to the FIFO request flags or FIFO warning flags and then only if the time between the STOP mode exit and subsequent STOP mode reentry is less than 3 asynchronous bit clock cycles.

**Workaround:** Ensure that at least 3 bit clock cycles elapse following an asynchronous interrupt wakeup event, before STOP mode is reentered.

## e5472: SMC: Mode transition VLPR->VLLS0(POR disabled)->RUN, will cause POR & LVD.

**Errata type:** Errata

**Description:** The Mode transition of VLPR into VLLS0 (POR disabled) then Exit, with LLWU event, back to to RUN mode will cause a POR and LVD reset instead of the expected WAKEUP exit.

**Workaround:** The recommendation is to transition from VLPR to RUN before entering VLLS0 with POR disabled mode.

## e3928: TSI: Delta voltage is 400 mV instead of 600 mV

**Errata type:** Errata

**Description:** Currently the delta voltage for the TSI channels is nominally 400mV. On future revisions the delta voltage will be changed to 600mV.

**Workaround:** Customers should account for this change in specification during their evaluations.

## e3926: TSI: The TSI will run several scan cycles during reference clock instead of scanning each electrode once

**Errata type:** Errata

**Description:** The TSI will run several scan cycles during reference clock instead of scanning each electrode once. For each automatic scanning period determined by AMCLKS (clock source), AMPSC (prescaler) and SMOD (period modulo), TSI will scan during one reference clock cycle divided by the AMPSC prescaler.

This does not affect the count result from TSI because TSI counters keep the last scan result.

**Workaround:** 1. Because counter results are not affected, a simple workaround is to use the smallest prescaler possible and use a bigger SMOD value, this will minimize the number of extra scans, thus also minimizing the amount of average extra current used by the module.

2. If strict control of number of scan cycles is needed, trigger scans with software control (using the SWTS bit) and control time between scans with a separate timer. This solution is only recommended if strict control of scan cycles is needed, if not, recommendation is to use workaround 1.

## e2638: TSI: The counter registers are not immediately updated after the EOSF bit is set.

**Errata type:** Errata

**Description:** The counter registers are not immediately updated after the end of scan event (EOSF is set). The counter registers will become available 0.25 ms after the EOSF flag is set. This also applies for the end-of-scan interrupt, as it is triggered with the EOSF flag. This behavior will occur both in continuous scan and in software triggered scan modes.

**Workaround:** Insert a delay of 0.25 ms or greater prior to accessing the counter registers after an end of scan event or an end of scan interrupt that is triggered by the EOSF flag. This delay does not need to be a blocking delay, so it can be executing other actions before reading the counter registers. Notice that the out-of-range flag (OUTRGF) and interrupt occur after the counters have been updated, so if the OUTRGF flag is polled or the out-of-range interrupt is used, the workaround is not necessary.

## e4546: TSI: The counter values reported from TSI increase when in low power modes (LLS, VLLS1, VLLS2, VLLS3)

**Errata type:** Errata

**Description:** When the MCU goes into LLS or VLLSx modes, with the TSI enabled for wakeup, the counter value reported by the TSI increases with respect to what was reported in active mode. Because the wakeup threshold is calculated in active mode, it is highly likely that MCU will wakeup immediately after going to low power.

**Workaround:** 1. Use Wait, Stop, or VLPS. These modes do not require any wakeup threshold calibration as TSI remains in active mode and wakes up each end of scan so that normal baseline tracking algorithm can be used.

2. To use LLS or VLLSx modes with the TSI as a wakeup source, calibrate the wakeup threshold using the desired low power mode. During application initialization, configure the TSI to exit low power via the LLWUI (low-leakage wake-up interrupt) with an End of Scan using the desired wakeup electrode. For example enter LLS mode with automatic scanning enabled so that after the first scan the TSI module causes an exit from low power at the end of scan. After the wakeup event, read the TSIx_WUCNTR Register, this register will have the value for the count during low power mode. Use this value to calculate THRSHLD register value.

## e4181: TSI: When the overrun flag is set, the TSI scanning sequence will exhibit undefined behavior.

**Errata type:** Errata

**Description:** When the overrun flag is set, the TSI scanning sequence will exhibit undefined behavior, so the results of measurements are invalid at this point. In order to continue reading valid measurements, disable the TSI module and reconfigure it.

**Workaround:** During development make sure to measure the required scanning time for all the electrodes in your system and configure the scanning time with AMCLKS, AMPSC and SMOD so that an overrun will not happen. Consider adding about 30 to 70% more time as headroom to make sure overrun is not triggered. If scanning time is critical and added scan time is not acceptable, detect the overrun condition either by polling the overrun flag in a loop or through the TSI interrupt. Once overrun is detected, disable the TSI module, clear all flags and reconfigure. During reconfiguration, SMOD can be increased by 10% or more of the current value to reduce the number of overrun occurrences.

## e4935: UART: CEA709.1 features not supported

**Errata type:** Errata
**Description:** Due to some issues that affect compliance with the specification, the CEA709.1 features of the UART module are not supported. Normal UART mode, IrDA, and ISO-7816 are unaffected.

**Workaround:** Do not use the UART in CEA709.1 mode.

## e2582: UART: Flow control timing issue can result in loss of characters

**Errata type:** Errata
**Description:** When /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

**Workaround:** For UARTs that implement an eight entry FIFO: When the FIFO is enabled, the receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

For UARTs without a FIFO (or if the FIFO is disabled): Delay might need to be added between characters on the transmit side in order to allow time for the negation of /RTS to be recognized before the next character is sent.

## e4945: UART: ISO-7816 T=1 mode receive data format with a single stop bit is not supported

**Errata type:** Errata
**Description:** Transmission of ISO-7816 data frames with single stop bit is supported in T=1 mode. Currently in order to receive a frame, two or more stop bits are required. This means that 11 ETU reception based on T=1 protocol is not supported. T=0 protocol is unaffected.

**Workaround:** Do not send T=1, 11 ETU frames to the UART in ISO-7816 mode. Use 12 ETU transmissions for T=1 protocol instead.

## e3892: UART: ISO-7816 automatic initial character detect feature not working correctly

**Errata type:** Errata

**Description:** The ISO-7816 automatic initial character detection feature does not work. The direct convention initial character can be detected correctly, but the inverse convention initial character will only be detected if the S2[MSBF] and S2[RXINV] bits are set. This defeats the purpose of the initial character detection and automatic configuration of the S2[MSBF], S2[RXINV], and C3[TXINV] bits.

**Workaround:** Use software to manually detect initial characters. Configure the UART with S2[MSBF] and S2[RXINV] cleared. Then check UART receive characters looking for 0x3B or 0x03. If 0x3B is received, then the connected card is direct convention. If 0x03 is received, then the connected card is inverse convention. If an inverse convention card is detected, then software should set S2[MSBF], S2[RXINV], and C3[TXINV].

## e5928: USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases

**Errata type:** Errata

**Description:** The USBx_USBTCR0[USBRESET] bit is not properly synchronized. In some cases using the bit can cause the USB module to enter an undefined state.

**Workaround:** Do not use the USBx_USBTCR0[USBRESET] bit. If USB registers need to be written to their reset states, then write those registers manually instead of using the module reset bit.

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