# PCA9460

## 13-channel power management integrated circuit (PMIC) for ultra-low power applications

Rev. 3.4 — 10 January 2024 Product data sheet

## 1 General description

The PCA9460 is a single chip Power Management IC (PMIC) designed to support ultra-low-power applications where standby power and overall power consumption of power management IC is critical. The PCA9460 is designed to be paired with i.MX 8ULP processor which enables such key applications. It provides power supply solutions for low power wearable application where size and efficiency are critical.

The PCA9460 comes equipped with four buck regulators, five LDOs and additional load switches. This design offers the most flexible configuration for i.MX 8ULP or other processors to enable the ultra-low-power system design. Each buck regulator has been designed with ultra-low Iq current to reduce standby current. Two buck regulators support smart Dynamic Voltage Scaling (DVS), which allows the system designed to set the right voltage on the processors the PCA9460 is powering. This process minimize power consumption that is controlled through the PMIC_STBY_REQ pin or MODE[2:0] pins. Five LDOs have 300 nA low quiescent current. One LDO is available for SNVS core power supply, one 250 mA LDO is to regulate to low output voltage from buck regulator output. Three 250 mA LDOs supply power to the processor and peripheral devices. Four 150 mΩ load switches switch power for peripheral devices. These switches can be configured as an LED driver with two different blink modes.

The PCA9460 is offered in a 42-bump wafer-level CSP package, 2.86 mm x 2.46 mm, 0.4 mm pitch.

## 2 Features and benefits

Ultra-low-power system design for long battery life or green offline performance using:

- Four buck regulators
  - Two 1 A buck regulators
  - Two 1 A buck regulator with DVS
  - Low Iq (1.5 µA at low power mode, 5.5 µA at normal mode)
- Five linear regulators
  - One 250 mA NMOS LDO
  - Three 250 mA PMOS LDO
  - 10 mA SNVS LDO
  - Built-in active discharge resistor
- Four Load Switches with active discharge resistor to allow easy connect/disconnect of multiple system rails
  - 150 mΩ Rdson
  - ON/OFF control in different modes
  - Configurable to LED driver with two blink patterns
- Power control IO for intelligent system design
  - Power ON/OFF control
  - Standby/Run mode control
  - Smart DVS control
- Flexible power ON/OFF sequence

- Fm+ 1 MHz $I^2C$ Interface allows continuous communication with the host
- ESD protection
  - Human Body Model (HBM) : ± 2000 V
  - Charged Device Model (CDM) : ± 500 V
- 7 x 6 bump array, 0.4 mm pitch, WL-CSP, 2.86 mm x 2.46 mm enables a small solution size

# 3 Applications

- Ultra-low-power portable devices
  - eReader
  - Tablet
  - Watch
  - Portable headset
  - Handheld printer/scanner
  - Bike computer

# 4 Ordering information

| Part number | Orderable part number | Topside marking | Temperature range (TA) | Processor and DDR Memory Platform | Package | | |
|---|---|---|---|---|---|---|---|
| | | | | | Name | Description | Version |
| PCA9460AUK | PCA9460AUKZ | N9460A | –40 °C to +85 °C | Ideal for i.MX 8ULP + LPDDR4 | WLCSP42 | Wafer Level Chip-Scale package; 42 bumps; 2.86 mm x 2.46 mm x 0.525 mm body (backside coating included), 0.4 mm pitch | SOT1459-7 |
| PCA9460BUK | PCA9460BUKZ | N9460B | | Ideal for i.MX 8ULP + LPDDR4X | | | |
| PCA9460CUK | PCA9460CUKZ | N9460C | | Ideal for i.MX 8ULP + LPDDR3 | | | |

# 5 Internal block diagram

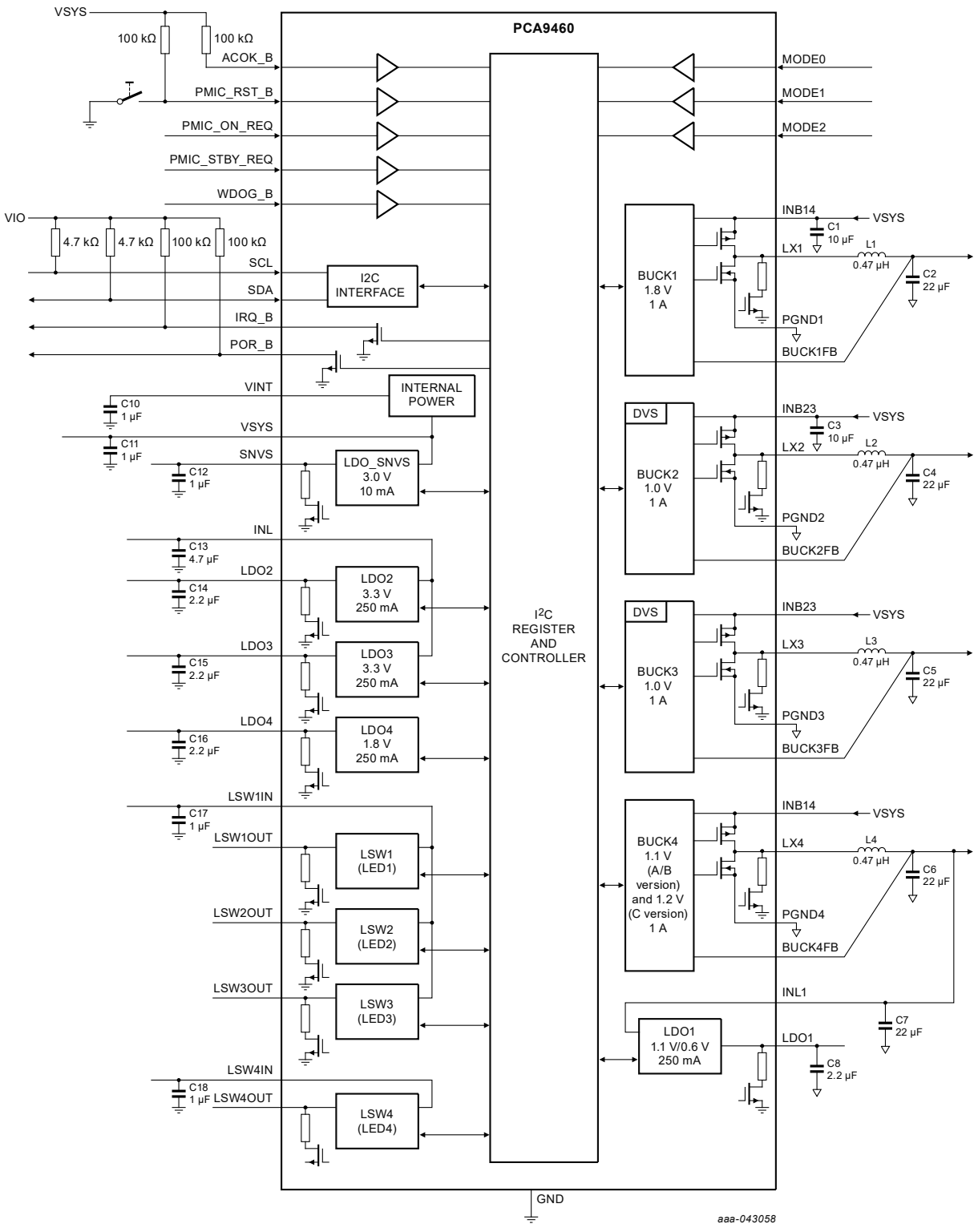



**Figure 1. Block diagram**

# 6 Pinning information

## 6.1 Pinning

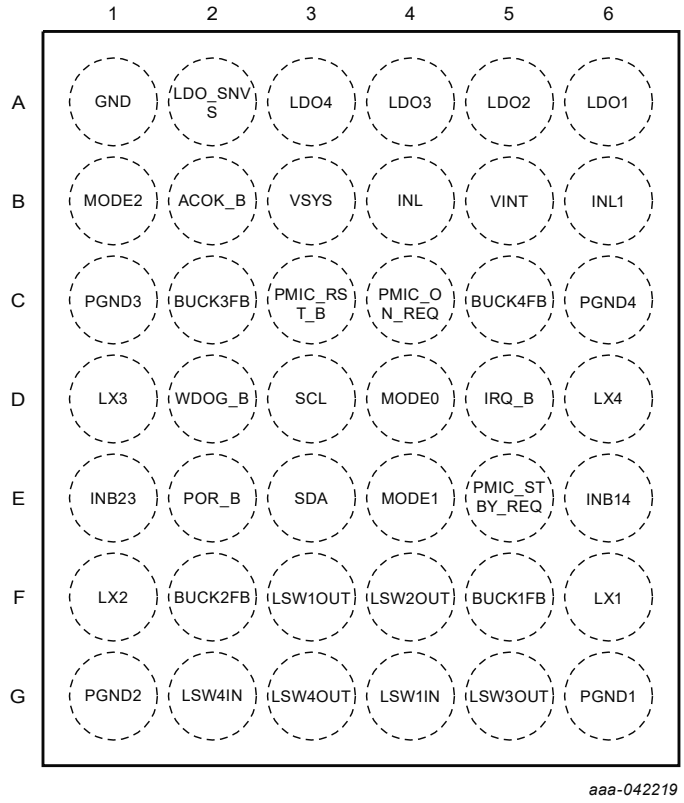



**Figure 2. PCA9460 pin map – Top View ( Bump-side down )**

## 6.2 Pin description

**Table 1. Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| MODE0 | D4 | DI | Digital MODE0 input pin |
| MODE1 | E4 | DI | Digital MODE1 input pin |
| MODE2 | B1 | DI | Digital MODE2 input pin |
| ACOK_B | B2 | DI | PMIC ON signal |
| PMIC_RST_B | C3 | DI | PMIC reset input pin. Once it is asserted low, PMIC performs cold reset. |
| POR_B | E2 | DO | Power On reset output pin. Open drain output requiring external pull up resistor. |
| PMIC_ON_REQ | C4 | DI | PMIC ON input from Application processor. When it is asserted high, the device starts power on sequence. |
| PMIC_STBY_REQ | E5 | DI | Standby mode input from Application processor. When it is asserted high, device enters STANDBY mode. |
| SCL | D3 | DI | $I^2C$ serial clock pin |
| SDA | E3 | DIO | $I^2C$ serial data pin |
| WDOG_B | D2 | DI | Watchdog reset input from application processor |

**Table 1. Pin description***...continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| IRQ_B | D5 | DO | PMIC interrupt pin, Open drain output requiring external pull up resistor |
| INB14 | E6 | P | Buck 1 / Buck 4 input pin, bypass with 10 µF |
| LX1 | F6 | P | Buck 1 switching node |
| PGND1 | G6 | P | Buck 1 Power ground |
| BUCK1FB | F5 | AI | Buck 1 feedback pin |
| INB23 | E1 | P | Buck 2 / Buck 3 input pin, bypass with 10 µF |
| LX2 | F1 | P | Buck 2 switching node |
| PGND2 | G1 | P | Buck 2 Power ground |
| BUCK2FB | F2 | AI | Buck 2 feedback pin |
| LX3 | D1 | P | Buck 3 switching node |
| PGND3 | C1 | P | Buck 3 Power ground |
| BUCK3FB | C2 | AI | Buck 3 feedback pin |
| LX4 | D6 | P | Buck 4 switching node |
| PGND4 | C6 | P | Buck 4 Power ground |
| BUCK4FB | C5 | AI | Buck 4 feedback pin |
| VSYS | B3 | P | Internal power input. Bypass with a 1 µF to Ground |
| LDO_SNVS | A2 | P | LDO_SNVS output pin, bypass with 1 µF to Ground |
| INL | B4 | P | LDO2/LDO3/LDO4 power input pins, bypass with a 4.7 µF to Ground |
| LDO2 | A5 | P | LDO2 output. Bypass with a 2.2 µF to Ground |
| LDO3 | A4 | P | LDO3 output. Bypass with a 2.2 µF to Ground |
| LDO4 | A3 | P | LDO4 output. Bypass with a 2.2 µF to Ground |
| INL1 | B6 | P | LDO1 input pins, bypass with a .2.2 µF to Ground |
| LDO1 | A6 | P | LDO1 output. Bypass with a 2.2 µF to Ground |
| LSW1IN | G4 | P | Load Switch input pin. Bypass with 1 µF to Ground |
| LSW1OUT | F3 | P | Load Switch output pin, if LSW1 is configured to LED driver, LSW1OUT is current source for LED |
| LSW2OUT | F4 | P | Load Switch output pin. if LSW2 is configured to LED driver, LSW2OUT is current source for LED |
| LSW3OUT | G5 | P | Load Switch output pin. if LSW3 is configured to LED driver, LSW3OUT is current source for LED driver |
| LSW4IN | G2 | P | Load Switch input pin. Bypass with 1 µF to Ground |
| LSW4OUT | G3 | P | Load Switch output pin. if LSW4 is configured to LED driver, LSW4OUT is current source for LED |
| VINT | B5 | P | Internal power supply output, bypass with 1 µF to GND |
| GND | A1 | P | Analog ground pin |

# 7 Functional description

## 7.1 Features

The PCA9460 is a power management integrated circuit (PMIC) designed to be the primary power management for NXP processors, 8ULP.

- Four buck regulators
  - Two 1A buck regulators
  - Two 1A buck regulator with DVS
  - Built-in active discharge resistor
  - Low Iq ( 1.5 µA at low power mode, 5.5 µA at normal mode )
- Five linear regulators
  - One 250 mA NMOS LDO
  - Three 250 mA PMOS LDO
  - Built-in active discharge resistor
  - 10 mA SNVS LDO
- Four load switches with active discharge resistor
  - 150 mΩ Rdson
  - ON/OFF control in different modes
  - Configurable to LED driver with two blink patterns
- Power control IO
  - Power ON/OFF control
  - Standby/Run mode control
  - Smart DVS control
- Flexible power ON/OFF sequence
- Fm+ 1 MHz $I^2C$ Interface
- ESD protection
  - Human Body Model (HBM) : +/- 2000 V
  - Charged Device Model (CDM) : +/-500 V
- 6 x 7 bump array, 0.4 mm pitch, WL-CSP, 2.86 mm x 2.46 mm

## 7.2 Functional diagram

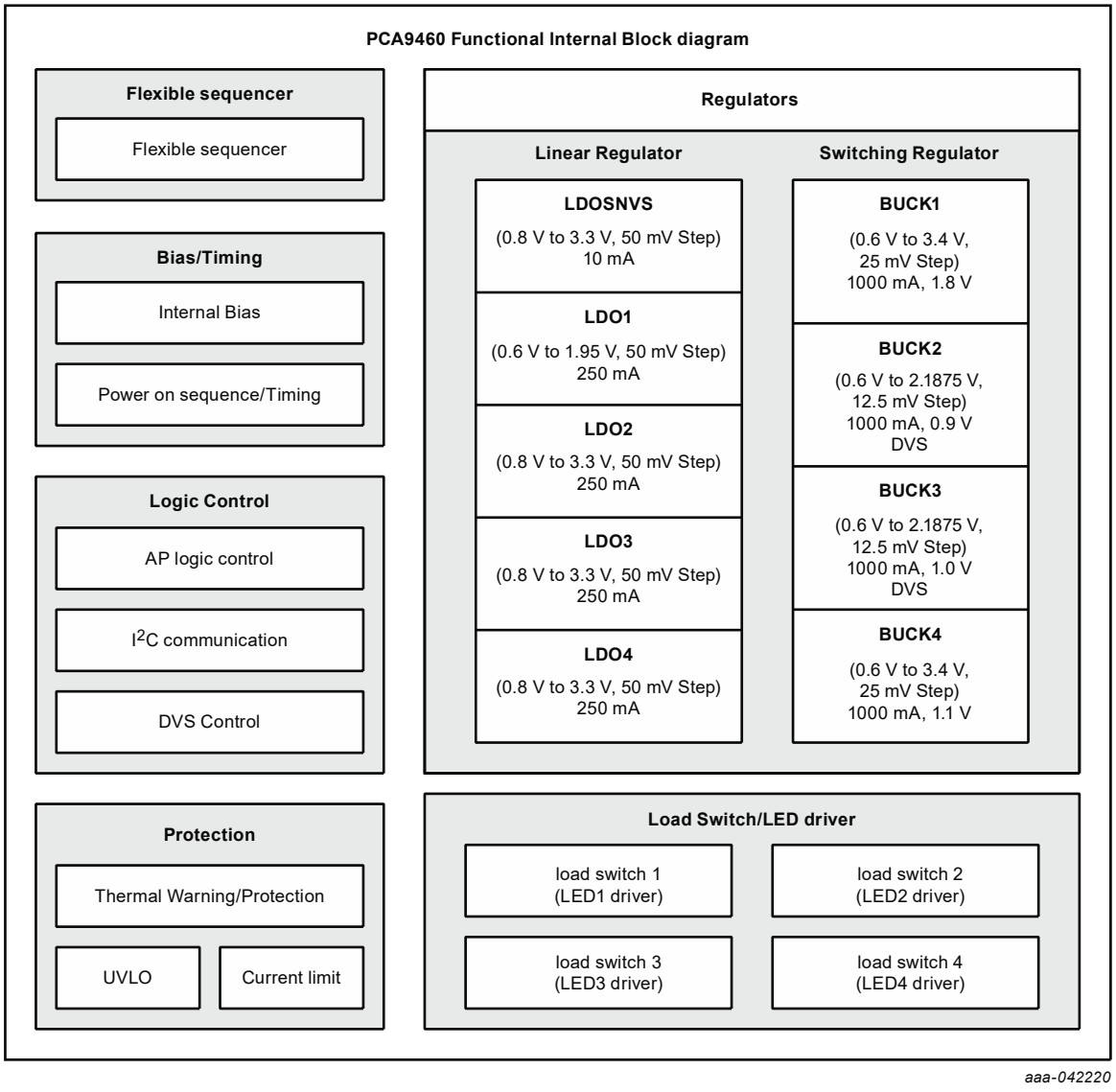



**Figure 3. PCA9460 functional block diagram**

## 7.3 PCA9460 version

The PCA9460 can be configured to each regulator default voltage and start-up sequence from the internal OTP configuration. Table 2 shows each OTP configuration for all devices.

**Table 2. OTP configuration**

*PCA9460A = i.MX 8ULP + LPDDR4; PCA9460B = i.MX 8ULP + LPDDR4X; PCA9460C = i.MX 8ULP + LPDDR3*

| Address | Register | PCA9460A | PCA9460B | PCA9460C | Description |
|---|---|---|---|---|---|
| 0x01 | OTP_VER | 0x02 | 0x11 | 0x21 | PCA9460A - Rev. 2 ; PCA9460B - Rev. 1 ; PCA9460C - Rev. 1 |
| 0x0A | PWR_SEQ_CTRL | 0x06 | | | 2 ms TON_STEP & 8 ms TOFF_STEP |
| 0x0C | SYS_CFG2 | 0x71 | | | 2 sec ONKEY timer; Normal Power Mode; 2.85 V VSYS UVLO |
| 0x10 | BUCK1CTRL | 0x39 | | | Normal mode; Enable Active Discharge Resistor ; Buck 1 ON at RUN state |
| 0x11 | BUCK1OUT | 0x30 | | | 1.8 V |
| 0x14 | BUCK2CTRL | 0x79 | | | 25 mV/2 µs DVS speed; Normal mode; Enable Active Discharge Resistor; Buck 2 ON at RUN state |
| 0x15 | BUCK2OUT_DVS0 | 0x20 | | | 1.0 V |
| 0x1F | BUCK2OUT_MAX_LIMIT | 0x38 | | | 1.3 V |
| 0x21 | BUCK3CTRL | 0x79 | | | 25 mV/2 µs DVS speed; Normal mode; Enable Active Discharge Resistor; Buck 3 ON at RUN state |
| 0x22 | BUCK3OUT_DVS0 | 0x20 | | | 1.0 V |
| 0x2C | BUCK3OUT_MAX_LIMIT | 0x38 | | | 1.3 V |
| 0x2E | BUCK4CTRL | 0x39 | | | Normal mode; Enable Active Discharge Resistor ; Buck 4 ON at RUN state |
| 0x2F | BUCK4OUT | 0x14 | | 0x18 | PCA9460A & PCA9460B = 1.1 V ; PCA9460C = 1.2 V |
| 0x30 | LDO1_CFG | 0x9D | | | LDO1 Auto Cout; 15 mΩ out trace compensation; Normal mode; LDO1 ON at RUN state |
| 0x31 | LDO1_OUT | 0x8A | 0x80 | 0x8C | PCA9460A = 1.1 V ; PCA9460B = 0.6 V ; PCA9460C = 1.2 V |
| 0x32 | LDO2_CFG | 0x11 | | | Enable Active Discharge Resistor ; LDO2 ON at RUN state |
| 0x33 | LDO2_OUT_L | 0x32 | | | 3.3 V on LDO2 when LDO2_VSEL = Low |
| 0x34 | LDO2_OUT_H | 0x14 | | | 1.8 V on LDO2 when LDO2_VSEL = High |
| 0x35 | LDO3_CFG | 0x11 | | | Enable Active Discharge Resistor ; LDO3 ON at RUN state |
| 0x36 | LDO3_OUT | 0x32 | | | 3.3 V |
| 0x37 | LDO4_CFG | 0x11 | | | Enable Active Discharge Resistor ; LDO4 ON at RUN state |
| 0x38 | LDO4_OUT | 0x14 | | | 1.8 V |
| 0x39 | LDOSNVS_CGF | 0xEC | | | Enable Active Discharge Resistor ; Always ON mode ; 3.0 V output |
| 0x40 | LSW1_CTRL | 0x11 | | | Load Switch mode; Enable Active Discharge; Load SW1 ON at RUN State |
| 0x41 | LSW2_CTRL | 0x11 | | | Load Switch mode; Enable Active Discharge; Load SW2 ON at RUN State |
| 0x42 | LSW3_CTRL | 0x11 | | | Load Switch mode; Enable Active Discharge; Load SW3 ON at RUN State |
| 0x43 | LSW4_CTRL | 0x11 | | | Load Switch mode; Enable Active Discharge; Load SW4 ON at RUN State |

## 7.4 Power states

PCA9460 has six power states: OFF, SNVS, RUN, PWRDN, PWRUP and FAULT_SD. Figure 4 shows the state transition diagram showing the conditions to enter and exit each state.

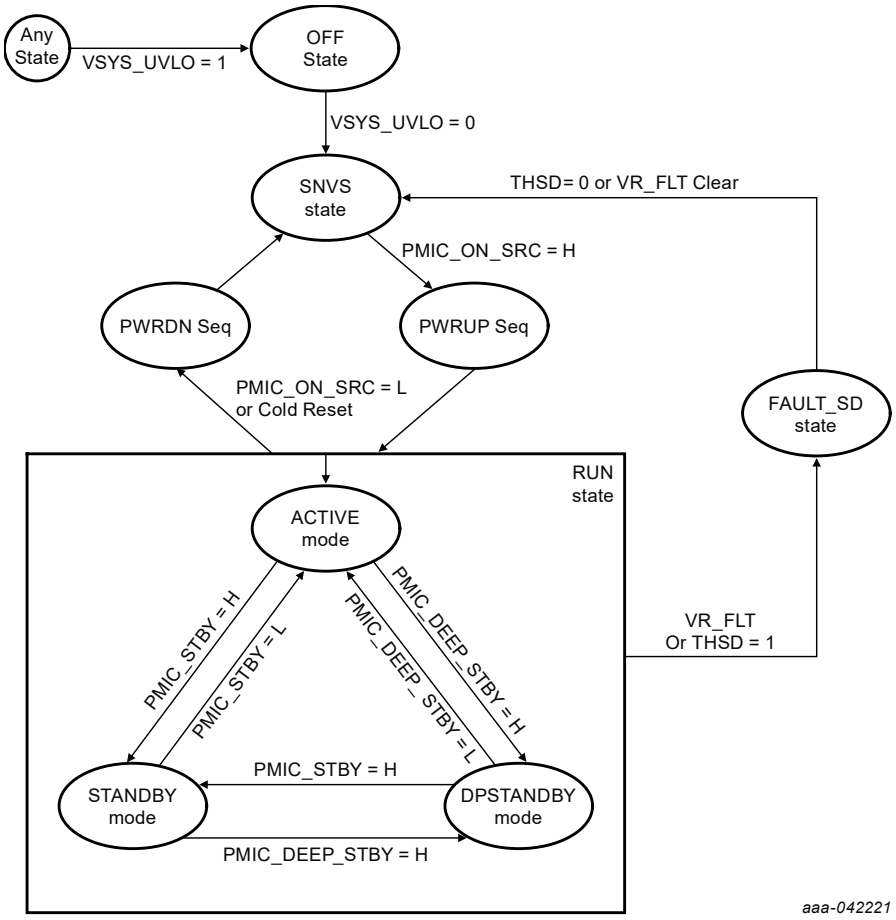



**Figure 4. Power states diagram**

### 7.4.1 Off state

PCA9460 enters OFF state from any state when VSYS falls below $V_{SYS\_UVLO}$ threshold. All regulators including LDO_SNVS are off, and all registers get reset in the state.

### 7.4.2 SNVS state

PCA9460 enters SNVS ( Secure Non-Volatile Storage mode ) when VSYS exceeds VSYS_UVLO rising threshold. LDO_SNVS is turned on within $t_{SNVS}$. After turning LDO_SNVS on, it monitors power on source signals to move to PWRUP state.

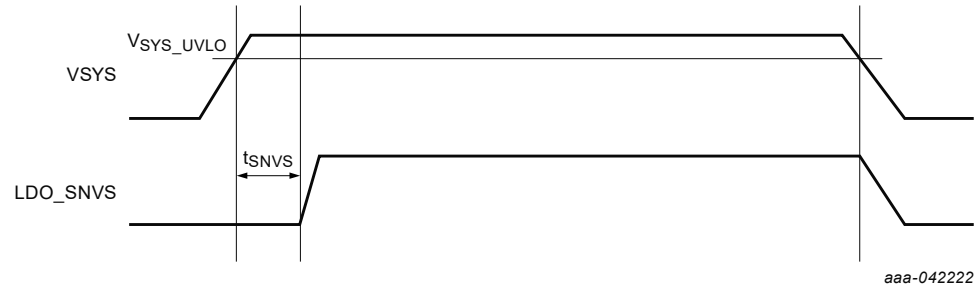



**Figure 5. SNVS state ON/OFF sequence**

| Time | Description | Value | Comment |
|---|---|---|---|
| $t_{SNVS}$ | Maximum time to enable LDO_SNVS from VSYS UVLO detected | 20 ms | |

### 7.4.3 PWRUP state

#### 7.4.3.1 Power ON sources

When internal signal, PMIC_ON_SRC, is asserted high in SNVS state, it starts powering up regulators with pre-defined power ON sequence. PMIC_ON_SRC signal is generated by below three signals.

- PMIC_ON_REQ after its debounce time
- PMIC_RST_B after its ONKEY debounce time. (It can be masked in PWR_SEQ_CTRL register)
- ACOK_B after its debounce time → OTP option to be disabled. (It can be masked in PWR_SEQ_CTRL register)

Figure 6 show the block diagram how PMIC_ON_SRC is generated.

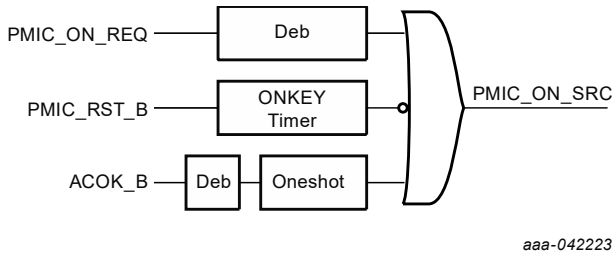



**Figure 6. PCA9460 power on source**

When ACOK_B signal is configured as Power on source in PWR_SEQ_CTRL register, One shot signal is generated from the falling edge of ACOK_B and the signal is maintained high for $t_{ACOK\_B\_Oneshot}$. If PMIC_ON_REQ pin is asserted high before one shot timer is expired, PMIC is kept powered on. If not, PCA9460 takes power-off sequence after one shot timer.

ACOKB_S status bit in INT1_STATUS register is updated after its debounce timer, $t_{ACOK\_B\_DEB}$.

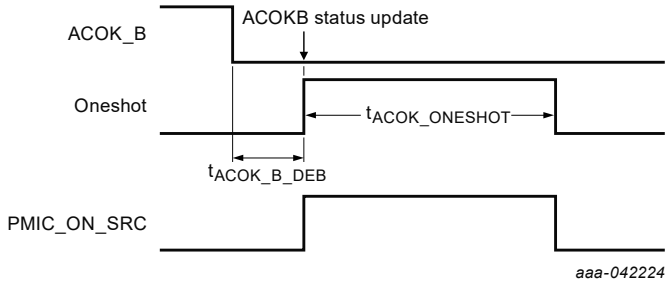



**Figure 7. ACOK_B timing**

PMIC_RST_B pin is used to turn on PCA9460 at SNVS state or to make PMIC reset at RUN state after detecting PMIC_RST_B falling edge. PMIC_RSTB_S status bit in INT1 STATUS register is updated in debounce time, $t_{DEB\_PMIC\_RST\_B}$, after falling edge detection.

When PMIC_RST_B falls low at SNVS state, then it starts counting timer. After ONKEY timer expired, ONKEY_S status bit is updated and PMIC_ON_SRC signal is generated if PMIC_RST_B pin is configured to power on source in PWR_SEQ_CTRL register. PMIC_ON_SRC is generated by PMIC_RST_B pin only when PCA9460 is in SNVS state. If ONKEY timer is expired at RUN state, only ONKEY_S bit is updated.

When PMIC_RST_B pin falls low at RUN state and RESETKEY timer is expired, RESETKEY_S status bit is updated and perform reset function configured in RESET_CTRL register after $t_{RESET\_WAIT}$, which is for AP to determine to proceed reset or not. For detail reset behavior, refer to Section 7.5.

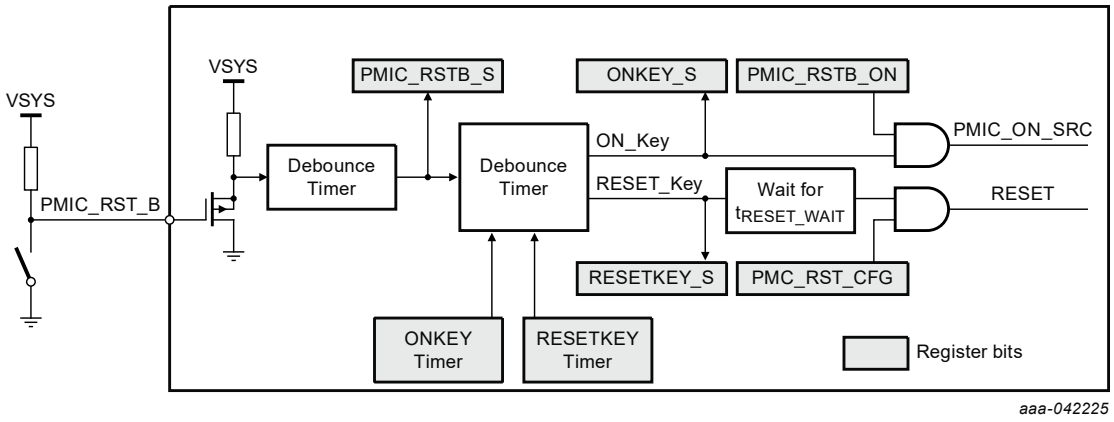



**Figure 8. PMIC_RST_B block diagram**

### 7.4.3.2 Power ON sequence

PCA9460 supports flexible power sequencer which power-on sequence can be pre-programmed in OTP.

When PMIC_ON_SRC is asserted high, PUD_T1 group is turned on at first in $t_{ON\_STEP}$ after PMIC_ON_SRC is high. The next group, PUD_T2 is turned on in $t_{ON\_STEP}$ after POK of PUD_T1 group regulator(s) is high. If the POK doesn't come up within $t_{POK\_EXP}$, then the POK is ignored and the next group is turned ON in $t_{ON\_STEP}$. This power on sequence ended up releasing POR_B pin high impedance in $t_{RSTB}$ after the last group, PUD_T16 regulator is turned ON. PUD group which any regulator is not assigned, the next PUD group is turned on in $t_{ON\_STEP}$.

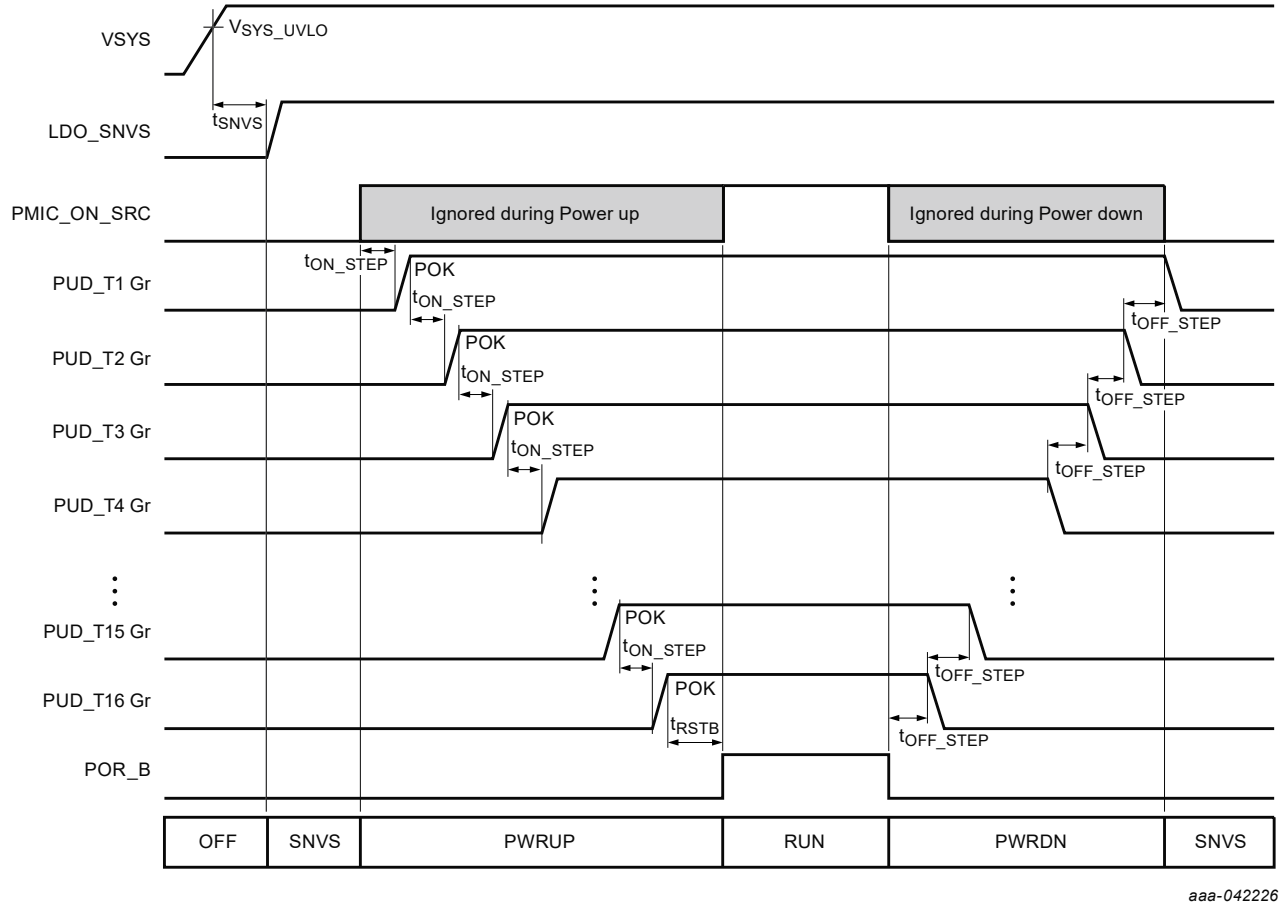



**Figure 9. PCA9460 power ON/OFF sequence**

**Table 3. Power up sequence**

| Regulator | PCA9460A | PCA9460B | PCA9460C |
|---|---|---|---|
| BUCK1 | T8, 1.8 V | T8, 1.8 V | T8, 1.8 V |
| BUCK2 | T10, 1.0 V | T10, 1.0 V | T10, 1.0 V |
| BUCK3 | T11, 1.0 V | T11, 1.0 V | T11, 1.0 V |
| BUCK4 | T11, 1.1V | T11, 1.1V | T11, 1.2V |
| LDO1 | T14, 1.1V | T14, 0.6V | T14, 1.2V |
| LDO2 | T9, 3.3 V | T9, 3.3 V | T9, 3.3 V |
| LDO3 | T12, 3.3 V | T12, 3.3 V | T12, 3.3 V |
| LDO4 | T12, 1.8 V | T12, 1.8 V | T12, 1.8 V |
| LSW1 | T13 | T13 | T13 |
| LSW2 | T10 | T10 | T10 |
| LSW3 | T15 | T15 | T15 |
| LSW4 | T9 | T9 | T9 |

### 7.4.4 PWRDN state

When PMIC_ON_SRC is asserted low in RUN state, PCA9460 enters PWRDN state, where it starts with pulling down POR_B, and then turning off each power rail in $t_{OFF\_STEP}$ and is transitioned to SNVS state.

### 7.4.5 RUN state

PCA9460 enters RUN state after PWRUP state. If PMIC_ON_SRC is asserted low, PCA9460 is transitioned to PWRDN state. When Cold reset event is triggered in RUN state, it is transitioned to PWRDN state. Regulator fault or Thermal shutdown happens in this state, it is transitioned to FAULT_SD state.

There are three kinds of modes in RUN state, ACTIVE, STANDBY and DPSTANDBY modes, depending on PMIC_STBY_REQ pin and STANDBY_CFG bit in SYS_CFG1 register.

Internal signals to change modes are generated as below.

1. PMIC_STBY = PMIC_STBY_REQ pin when STANDBY_CFG = 0b
   PMIC_STBY is set high only when PMIC_STBY_REQ pin is high and STANDBY_CFG bit is 0b.
2. PMIC_DEEP_STBY = PMIC_STBY_REQ pin when STANDBY_CFG = 1b
   PMIC_DEEP_STBY is set high only when PMIC_STBY_REQ pin is high and STANDBY_CFG bit is 1b.

Each regulator and load switch have enable configuration bits to turn on each mode.

00b = OFF

01b = ON at RUN State

10b = ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY

11b = ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY

#### 7.4.5.1 ACTIVE mode

When PCA9460 enters RUN state from PWRUP state, it enter ACTIVE mode at first. And then it transitions to STANDBY mode or DPSTANDBY mode depending on PMIC_STBY or PMIC_DEEP_STBY signal.

#### 7.4.5.2 STANDBY mode

PCA9460 is transitioned to STANDBY mode when PMIC_STBY is high. PMIC_STBY is determined by PMIC_STBY_REQ pin when STANDBY_CFG bit in SYS_CFG1 register is set to 0b. PCA9460 move to ACTIVE mode when PMIC_STBY_REQ pin is low. It transitioned to DPSTANDBY mode when STANDBY_CFG bit is changed to 1b.

#### 7.4.5.3 DPSTANDBY mode

PCA9460 is transitioned to DPSTANDBY ( Deep Standby) mode when PMIC_DEEP_STBY is high. PMIC_DEEP_STBY is determined by PMIC_STBY_REQ pin when STANDBY_CFG bit in SYS_CFG2 register is set to 1b. PCA9460 move to ACTIVE mode when PMIC_STBY_REQ pin is low. It transitioned to STANDBY mode when STANDBY_CFG bit is changed to 0b.

**Table 4. States Summary**

| State | Mode | VSYS | PMIC_ON_SRC | STANDBY_CFG bit | PMIC_STBY_REQ |
|---|---|---|---|---|---|
| OFF | — | VSYS < $V_{SYS\_UVLO}$ | X | X | X |
| SNVS | — | VSYS > $V_{SYS\_UVLO}$ | Low | X | X |
| RUN | ACTIVE | VSYS > $V_{SYS\_UVLO}$ | High | X | Low |

**Table 4. States Summary***...continued*

| State | Mode | VSYS | PMIC_ON_SRC | STANDBY_CFG bit | PMIC_STBY_REQ |
|---|---|---|---|---|---|
| RUN | STANDBY | VSYS > $V_{SYS\_UVLO}$ | High | 0b | High |
| RUN | DPSTANDBY | VSYS > $V_{SYS\_UVLO}$ | High | 1b | High |

*X : Don't care*

### 7.4.6 FAULT_SD state

PCA9460 has two Fault shutdown sources.

1. **Thermal shutdown**: Transition to SNVS state after FAULT_SD state
   When junction temperature reaches $T_{JSHDN}$, it enters FAULT_SD state after $t_{FLT\_THSD}$, where all regulators are turned off immediately after pulling down POR_B. It stays at FAULT_SD until junction temperature falls below $T_{JSHDN}$. When the temperature drops below $T_{JSHDN}$, then it transitions to SNVS state.

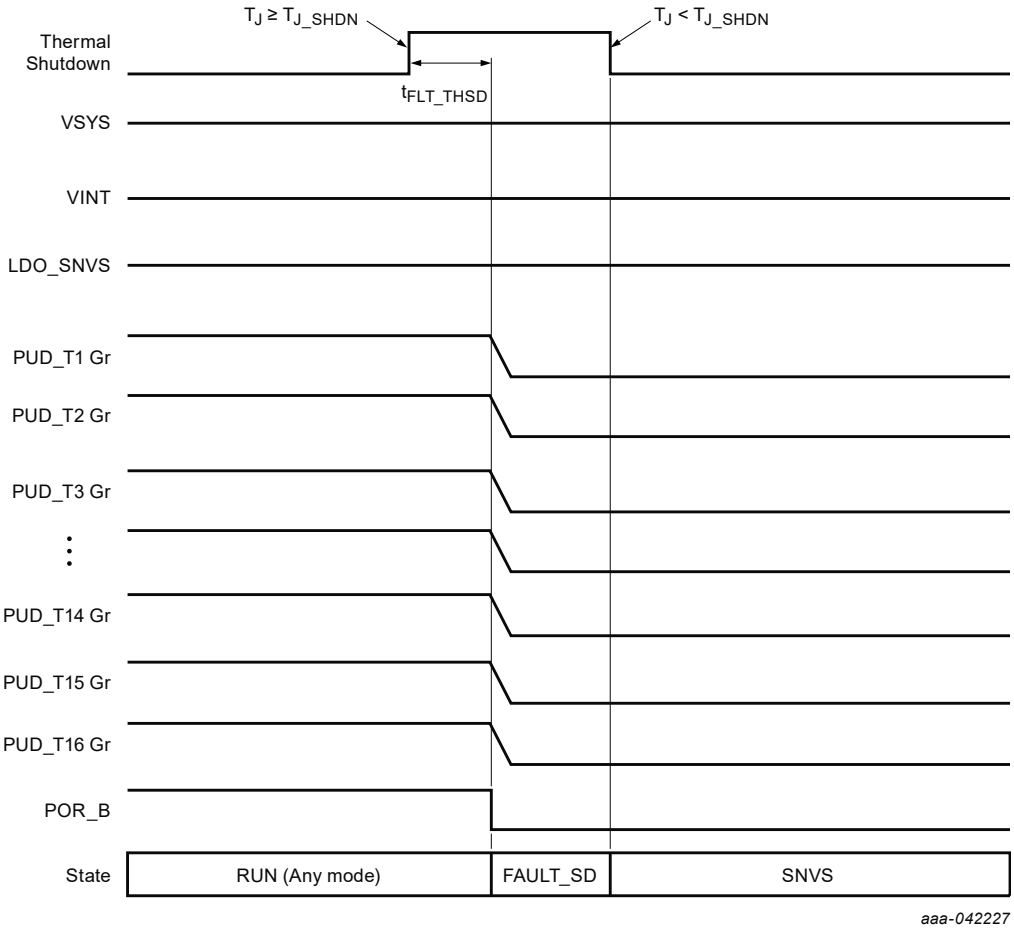



**Figure 10. PCA9460 FAULT_SD from Thermal shutdown**

**Table 5.**

| Time | Description | Value | Comment |
|---|---|---|---|
| $t_{FLT\_THSD}$ | Time to reset released from Fault event | 20 µs | |

2. **Voltage regulator fault in RUN state**: Transition to FAULT_SD state in $t_{FLT\_SD\_WAIT}$ after Fault is detected and then transition to SNVS state in $t_{FLT\_SD\_STAY}$

VR Fault status bit in INT1_STATUS register is latched to "1" when corresponding regulator voltage falls below POK threshold for $t_{DEB\_POKB}$.

If the fault status bit is masked in VRFLT1_MASK register, PCA9460 doesn't enter FAULT_SD state, instead, PCA9460 stays at RUN state. If the fault register bit is unmasked, it starts $t_{FLT\_SD\_WAIT}$ timer. Application processor can determine to enter FAULT_SD state by masking the VR Fault status bit in VRFLT1_MASK registers before the timer expires. PCA9460 enter FAULT_SD state when the timer is expired. PCA9460 stays at FAULT_SD state for $t_{FLT\_SD\_STAY}$ and moves to SNVS state from FAULT_SD mode after $t_{FLT\_SD\_STAY}$.

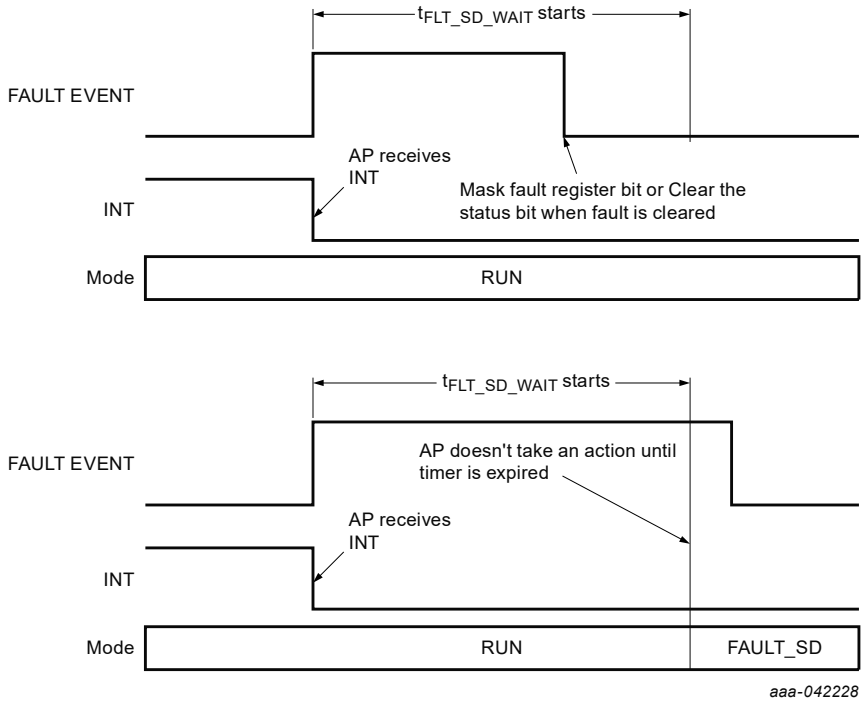



**Figure 11. FAULT_SD from VR Fault in RUN state**

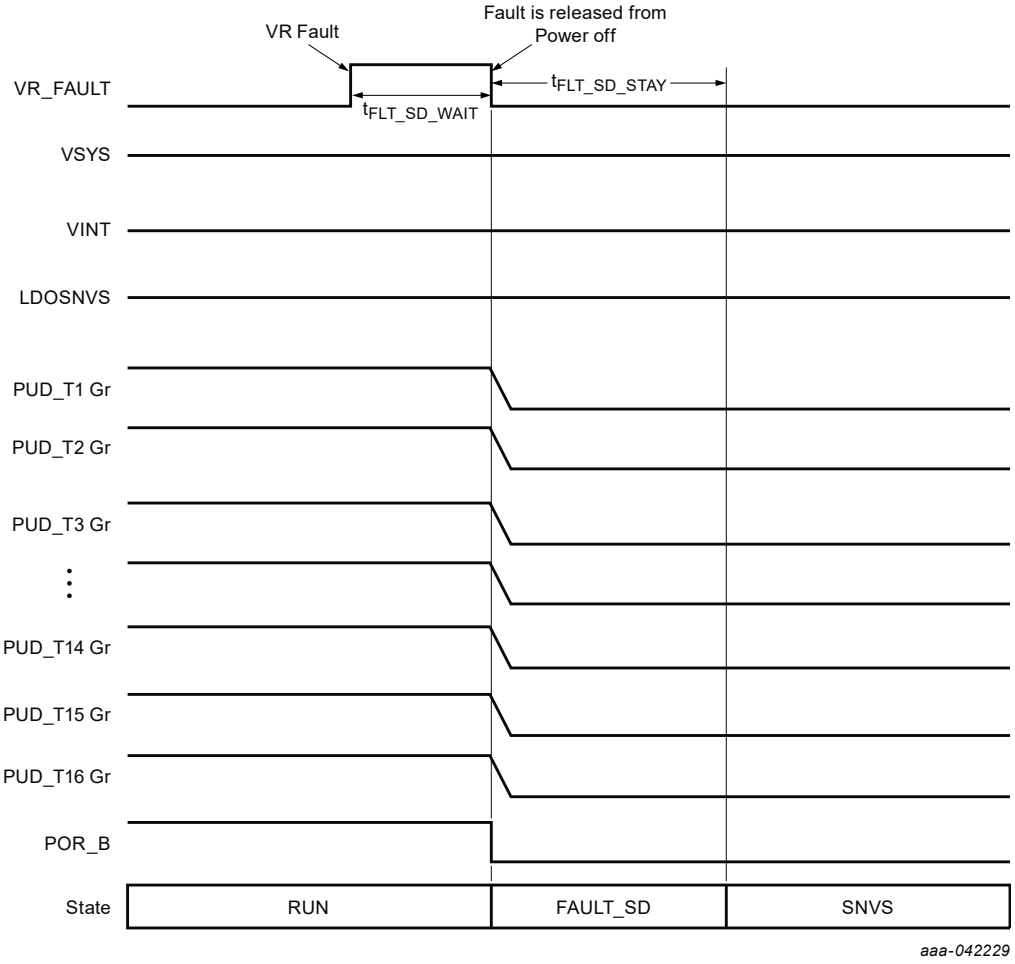



**Figure 12. PCA9460 FAULT_SD from VR Fault in RUN/STANDBY**

**Table 6. FAULT_SD description**

| Time | Description | Value | Comment |
|---|---|---|---|
| $t_{FLT\_SD\_WAIT}$ | VR Fault wait time to enter fault shutdown | 100 ms | 20 µs, 100 ms option |
| $t_{FLT\_SD\_STAY}$ | Time to stay at Fault_SD state | 100 ms | |

## 7.5 PMIC reset

The PCA9460 PMIC has three reset inputs, WDOG_B pin, PMIC_RST_B pin and $I^2C$ reset bit, The reset is executed only at RUN state.

The reset behavior is configured in 0x08 RESET_CTRL register for WDOG_B pin and PMIC_RST_B pin. $I^2C$ reset behavior is configured in 0x09 SW_RST register.

**Table 7. PMIC Reset description**

| 0x08 – RESET_CTRL | | | | Reset Type | S |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Type** | **Reset** | **Description** | |
| 7 to 6 | WDOG_B_CFG | R/W | 00 | When WDOG_B is asserted to L, PMIC behavior<br>**00b = WDOG_B reset is disabled**<br>01b = Warm Reset, POR_B pin is asserted low for $t_{RSTB}$<br>10b,11b = Cold Reset, All voltage regulators are recycled | |
| 5 to 4 | PMIC_RST_CFG | R/W | 10 | When PMIC_RST_B is asserted to L, PMIC behavior<br>00b = PMIC_RST_B reset is disabled<br>01b = Warm Reset, POR_B pin is asserted low for $t_{RSTB}$<br>**10b**, 11b **= Cold Reset, All voltage regulators are recycled** | |
| **0x09 – SW_RST** | | | | **Reset Type** | **O** |
| **Bit** | **Name** | **Type** | **Reset** | **Description** | |
| 7 to 0 | SW_RST_KEY | R/W | 0x00 | Software reset register. This register is read back to "0x00" right after writing the value.<br>**0x00 = No action**<br>0x05 = Reset O-type registers to default value<br>0x09 = Reset O-type registers and S-type registers<br>0x14 = Cold reset (Power recycle all regulators )<br>0x35 = Warm Reset (Toggle POR_B for $t_{RSTB}$)<br>0xEE = PMIC digital reset ( Debug purpose only )<br>Others = Forbidden | |

WDOG_B is asserted low, PCA9460 gets reset depending on WDOG_B_CFG bit configuration. When the bits are set to 2b00, the reset by WDOG_B pin is disabled. If the bits are set to 2b01, warm reset is preformed, where pulling POR_B low for $t_{RESET}$ and reset $I^2C$ O type registers to default value keeping power rails remaining ON. After reset, WDOG_B pin must be released high to get another reset from WDOG_B falling edge.

When PMIC_RST_B is asserted low and it stays low for RESETKEY timer configured in SYS_CFG1 register, PCA9460 waits for $t_{RESET\_WAIT}$ after issuing RESETKEY interrupt. If application processor doesn't disable reset by writing 00b in PMIC_RST_CFG bits, then PCA9460 gets reset depending on PMIC_RST_CFG bits configuration. When the bits are set to 2b00, any reset by PMIC_RST_B pin is disabled. If the bits are set to 2b01, warm reset is preformed, in which pulling POR_B low for $t_{RESET}$ and reset $I^2C$ O type registers to default value keeping power rails remaining ON. After reset, PMIC_RST_B pin must be released high to get another reset from PMIC_RST_B falling edge.

Cold reset event is generated by either of $I^2C$ reset, WDOG_B falling edge or PMIC_RST_B falling edge after debounce time. Once it is detected, POR_B is pulled low and takes power down sequence. PCA9460 stays at RESET for $t_{RESTART}$ and then start power on sequence even though WDOG_B pin is still low.

Figure 13 shows cold reset behavior. From any cold reset signal from either of PMIC_RST_B, WDOG_B or $I^2C$, it starts with power down sequence and stays off for $t_{RESETART}$. It automatically proceed power ON sequence and then enters RUN state. PMIC_ON_SRC is ignored for $t_{PWR\_HOLD\_RST}$ after entering RUN state. If PMIC_ON_SRC doesn't come up until $t_{PWR\_HOLD\_RST}$ is expired, then PCA9460 is turned off.

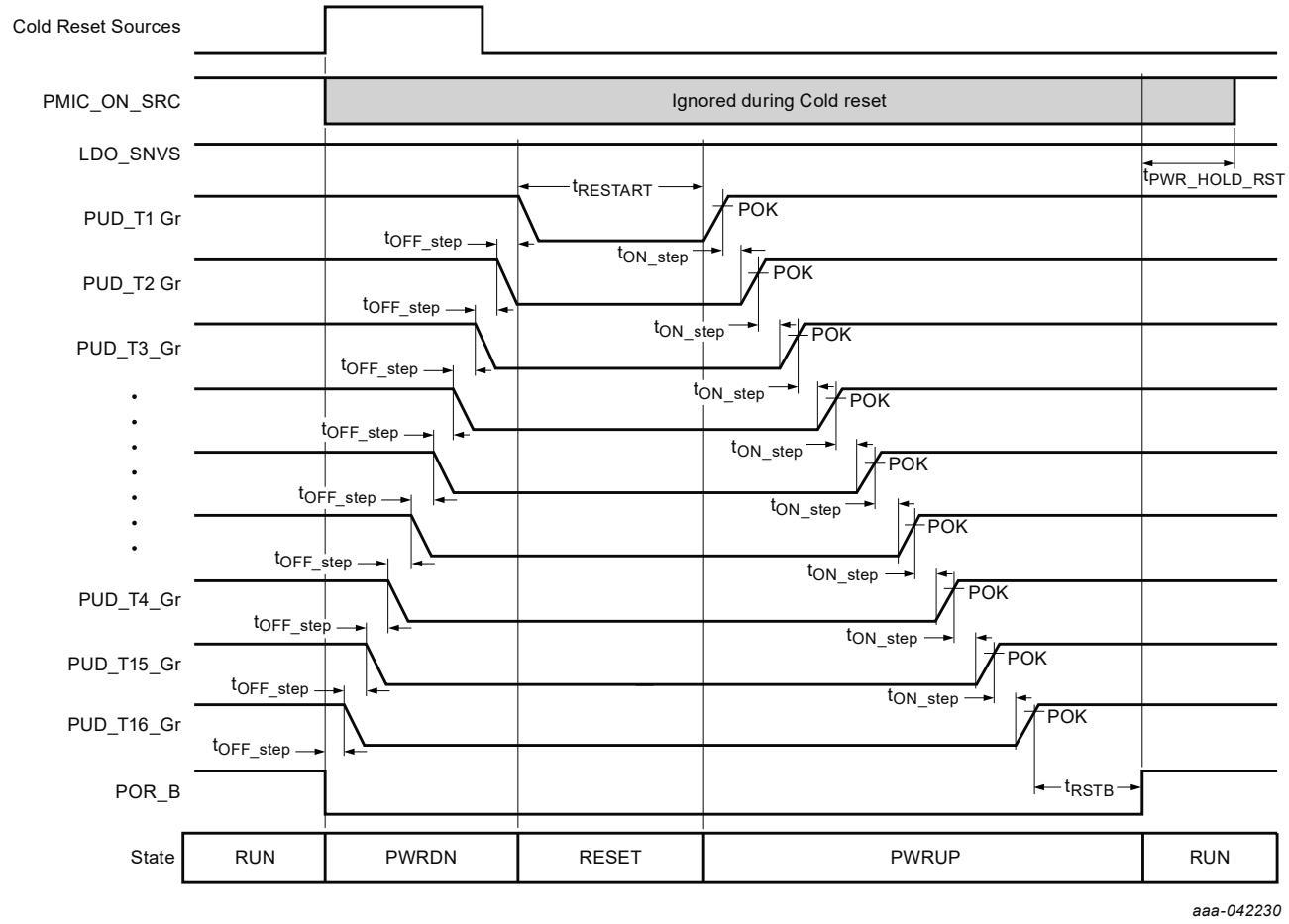



**Figure 13. PCA9460 Cold reset**

**Table 8. PCA9460 Cold reset description**

| Time | Description | Value | Comment |
|---|---|---|---|
| $t_{RESTART}$ | Time to power ON seq from end of power OFF seq during cold reset | 250 ms | |
| $t_{PWR\_HOLD\_RST}$ | Time to hold power-on after reset | 100 ms | |

Figure 14 shows warm reset behavior. From any warm reset signal from either of PMIC_RST_B, WDOG_B or $I^2C$, it makes POR_B toggled for $t_{RESET}$ and all O type registers get reset. PMIC_ON_SRC is ignored for $t_{PWR\_HOLD\_RST}$ after entering RUN state as like cold reset behavior.

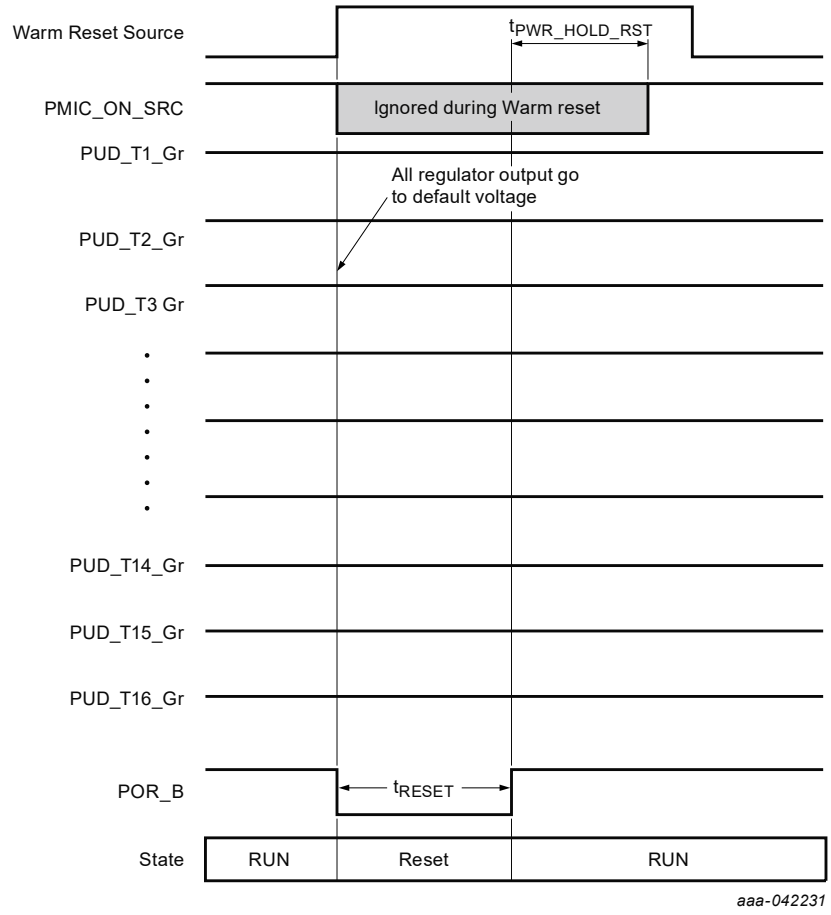



**Figure 14. Warm reset**

**Table 9. Warm reset description**

| Time | Description | Value | Comment |
|---|---|---|---|
| $t_{RESET}$ | POR_B low time at Warm reset | 20 ms | |

## 7.6 Regulator summary

The PCA9460 PMIC features four high efficiency low quiescent current buck regulators, four LDO regulators and low iq SNVS LDO to supply voltages for the application processor and peripheral devices.

### 7.6.1 BUCK regulator

The PCA9460 has four high-efficiency low Iq buck regulators. Each buck regulator features soft start and over-current protection. Buck regulator operates in two modes, PFM and PWM mode. Each buck regulator operates in PFM(Pulse Frequency Modulation) mode at light load that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

In PFM Mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (Pulse Width Modulation) mode and operates in continuous conduction

mode with a nominal switch frequency fsw of typically 2 MHz. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

When the Bx_FPWM bits (Bit 2) on the BUCKxCTRL registers are set to 1, the buck regulator operates in only PWM mode, regardless of load current.

Internal active discharge resistor is installed in each buck regulator output to discharge voltage on output capacitors when regulator is off. It is configurable through the $I^2C$ register using Bx_AD bit (Bit 3) on BUCKxCTRL registers.

Table 10 shows buck regulator summary.

**Table 10. PCA9460 Buck Summary**

| Buck# | Input pin | Default VOUT [V] | VOUT range [V] | Step size [mV] | Default ON/ OFF | Current rating [mA] |
|---|---|---|---|---|---|---|
| BUCK1 | INB14 | 1.8 | 0.6 to 3.4 | 25 | ON | 1000 |
| BUCK2 | INB23 | 1.0 | 0.6 to 2.1875 | 12.5 | ON | 1000 |
| BUCK3 | INB23 | 1.0 | 0.6 to 2.1875 | 12.5 | ON | 1000 |
| BUCK4 | INB14 | [1] | 0.6 to 3.4 | 25 | ON | 1000 |

[1] PCA9460A and PCA9450B: 1.1 V, PCA9460C: 1.2 V

BUCK1 and BUCK4 output voltages are programmable from 0.60 V to 3.40 V in 25 mV steps. This is done by setting the B1_OUT[6:0], and B4_OUT[6:0] bits on registers BUCK1OUT and BUCK4OUT respectively. Table 108 shows the output voltage coding for these regulators.

BUCK2 and BUCK3 output voltages are programmable from 0.60 V to 2.1875 V in 12.5 mV steps. Setting Bx_DVS_CTRL bits to 00b, DVS is controlled by Bx_DVS0[6:0] bits on BUCKxOUT_DVS0 register through $I^2C$. Table 107 shows the output voltage coding for these regulators.

### 7.6.1.1 ON/OFF control

Each buck regulator can be turned ON/OFF through $I^2C$ or PMIC_STBY_REQ pin, which can be configured in each Bx_ENMODE bits in BUCKxCTRL register.

- BxENMODE = 00b : the buck regulator is forcedly OFF
- BxENMODE = 01b : the buck regulator is ON in RUN state ( ACTIVE / STANDBY / DPSTANDBY mode )
- BxENMODE = 10b : the buck regulator is ON in ACTIVE or STANDBY mode and it is OFF in DPSTANDBY mode
- BxENMODE = 11b : the buck regulator is ON in ACTIVE mode and it is OFF in STANDBY or DPSTANDBY mode

### 7.6.1.2 Dynamic voltage scaling

BUCK2 and BUCK3 support dynamic voltage scaling (DVS) through MODE[2:0] pins or PMIC_STBY_REQ pin depending on Bx_DVS_CTRL bits in BUCK23_DVS_CFG2 register.

**Table 11. 0x13 – BUCK23_DVS_CFG2**

*Reset Type: 0*

| Bit | Name | Type | Reset | Description |
|---|---|---|---|---|
| 7 to 6 | B2_DVS_CTRL | R/W | 00 | BUCK2 DVS Control<br>**00b = DVS control BUCK2OUT_DVS0 Reg through $I^2C$**<br>01b = DVS control through PMIC_STBY_REQ pin |

**Table 11. 0x13 – BUCK23_DVS_CFG2***...continued*

*Reset Type: 0*

| Bit | Name | Type | Reset | Description |
|---|---|---|---|---|
| | | | | 10b = DVS control through MODE[2:0] pins in ACTIVE mode and the voltage set to BUCK2OUT_STBY when PMIC_STBY_REQ = H<br>11b = DVS control through MODE[2:0] pins in RUN state |
| 5 to 4 | B3_DVS_CTRL | R/W | 00 | BUCK3 DVS Control<br>**00b = DVS control BUCK3OUT_DVS0 Reg through $I^2C$**<br>01b = DVS control through PMIC_STBY_REQ pin<br>10b = DVS control through MODE[2:0] pins in ACTIVE mode and the voltage set to BUCK3OUT_STBY when PMIC_STBY_REQ = H<br>11b = DVS control through MODE[2:0] pins in RUN state |
| 3 to 0 | RSVD | R/W | 0000 | Reserved |

When Bx_DVS_CTRL bits are set to 00b, DVS is controlled by Bx_DVS0 bits on the BUCKxOUT_DVS0 register through $I^2C$. If BUCKxOUT_DVS0 register is overwritten with different voltage through $I^2C$, the output voltage is changed accordingly without ramping up/down.

When the Bx_DVS_CTRL bits are set to 01b, the buck regulator output voltage is determined by BUCKxOUT_DVS0 and BUCKxOUT_STBY registers through PMIC_STBY_REQ pin.

When the bits are set to 10b, the output voltage is controlled by MODE[2:0] pins in ACTIVE mode ( PMIC_STBY_REQ pin = L) and the voltage is set to BUCKxOUT_STBY register in STANDBY mode or DPSTANDBY mode ( PMIC_STBY_REQ pin = H), where MODE[2:0] pins should not be changed.

When the bits are set to 11b, the buck voltage is always controlled by MODE[2:0] pins.

Figure 15 shows DVS function block diagram and Table 12 show how buck voltage is determined by MODE[2:0] pins.

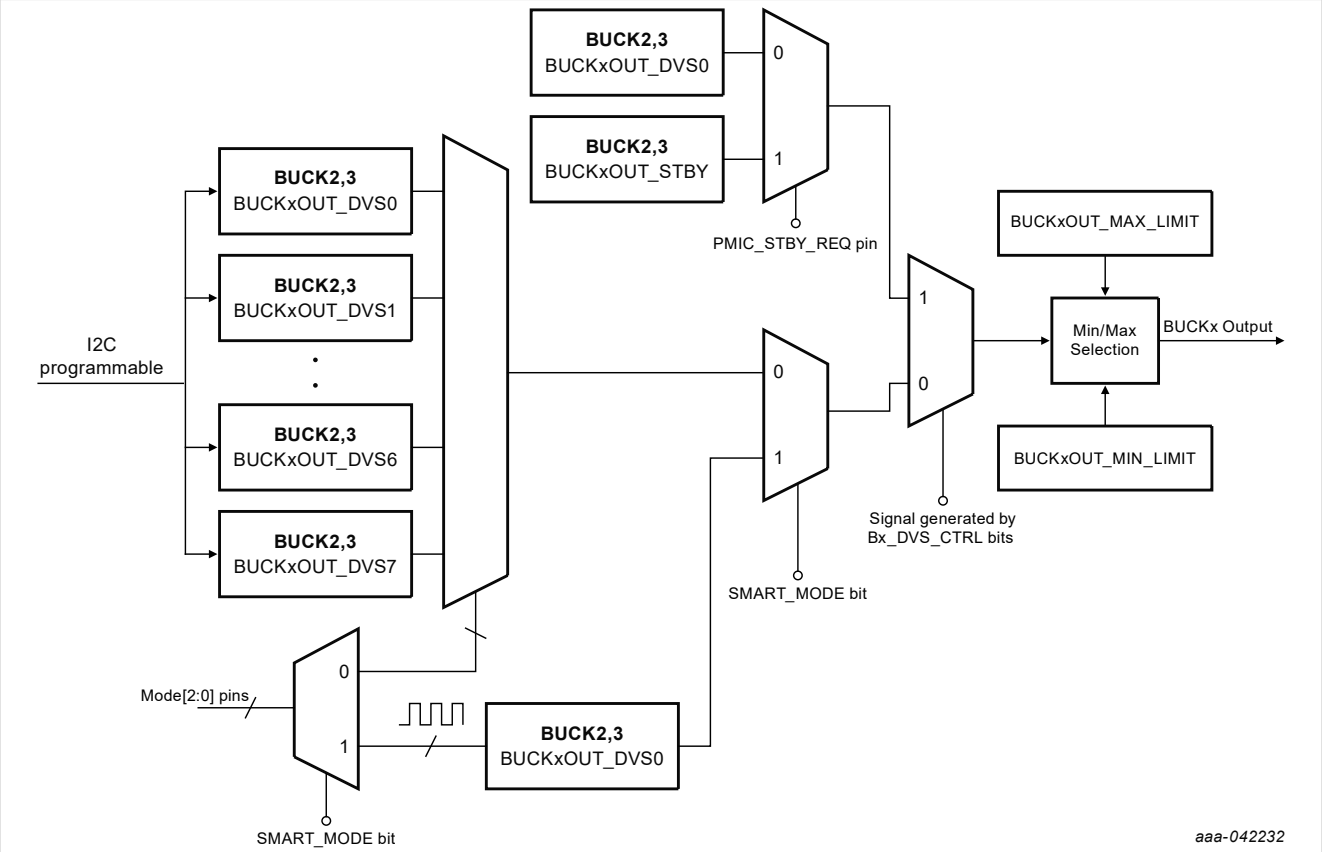



**Figure 15. DVS functional diagram**

**Table 12. MODE[2:0] pins configuration**

| $I^2C$ bits | | PMIC MODE pins | | | Buck output voltage |
|---|---|---|---|---|---|
| SMART_MODE | MODE2_EN | MODE2 | MODE1 | MODE0 | |
| 0 | X | 0 | 0 | 0 | BUCKxOUT_DVS0 |
| 0 | X | 0 | 0 | 1 | BUCKxOUT_DVS1 |
| 0 | X | 0 | 1 | 0 | BUCKxOUT_DVS2 |
| 0 | X | 0 | 1 | 1 | BUCKxOUT_DVS3 |
| 0 | X | 1 | 0 | 0 | BUCKxOUT_DVS4 |
| 0 | X | 1 | 0 | 1 | BUCKxOUT_DVS5 |
| 0 | X | 1 | 1 | 0 | BUCKxOUT_DVS6 |
| 0 | X | 1 | 1 | 1 | BUCKxOUT_DVS7 |
| 1 | 0 | X | 0 | 0 | No voltage Change |
| 1 | 0 | X | 0 | 1 | Decrement by Bx_DVS_DN mV, select BUCK through BUCK_SEL bit |
| 1 | 0 | X | 1 | 0 | Increment by Bx_DVS_UP mV, select BUCK through BUCK_SEL bit |
| 1 | 0 | X | 1 | 1 | No voltage Change |
| 1 | 1 | 0 | 0 | 0 | No voltage Change |

**Table 12. MODE[2:0] pins configuration***...continued*

| $I^2C$ bits | | PMIC MODE pins | | | Buck output voltage |
|---|---|---|---|---|---|
| SMART_MODE | MODE2_EN | MODE2 | MODE1 | MODE0 | |
| 1 | 1 | 0 | 0 | 1 | Decrement BUCK2 by Bx_DVS_DN mV |
| 1 | 1 | 0 | 1 | 0 | Increment BUCK2 by Bx_DVS_UP mV |
| 1 | 1 | 0 | 1 | 1 | No voltage Change |
| 1 | 1 | 1 | 0 | 0 | No voltage Change |
| 1 | 1 | 1 | 0 | 1 | Decrement BUCK3 by Bx_DVS_DN mV |
| 1 | 1 | 1 | 1 | 0 | Increment BUCK3 by Bx_DVS_UP mV |
| 1 | 1 | 1 | 1 | 1 | No voltage Change |

When SMART_MODE bit in BUCK23_DVS_CFG1 register is set to 0b, MODE[2:0] pins are used to select buck DVS output voltage configuration, BUCKxOUT_DVSx registers, which should be pre-configured by application processor. PCA9460 detects the first level change among MODE[2:0] pins, 3 internal clock later, the output voltage is updated. The maximum latency of these MODE pins is specified to $t_{MAX\_DIFF}$.

Figure 16 shows DVS operation through MODE[2:0] pins when SMART_MODE bit is set to 0b.

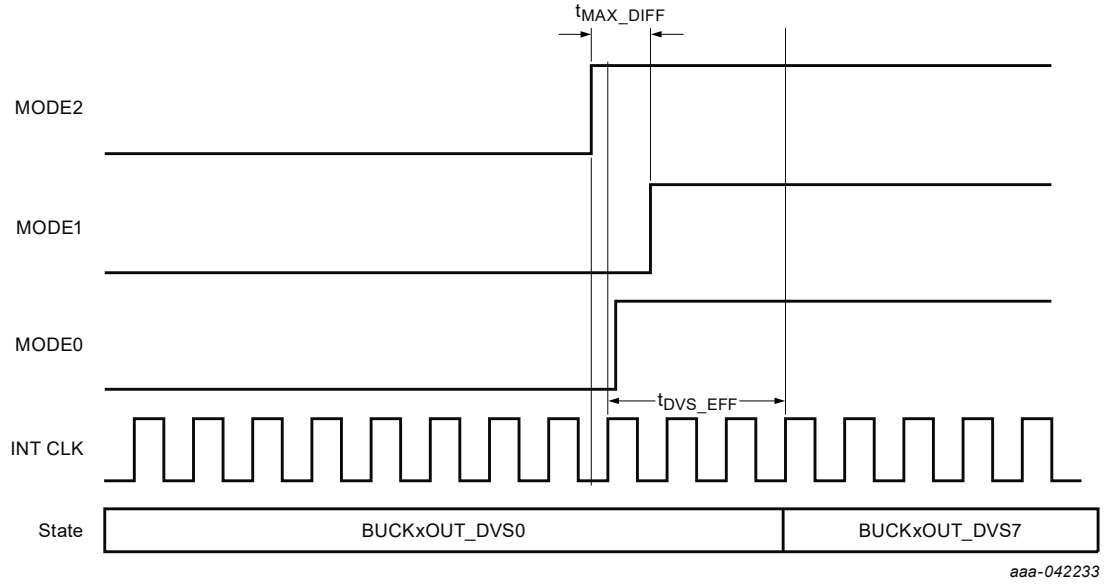



**Figure 16. MODE[2:0] pins operation at SMART_MODE = 0**

When SMART_MODE is set to 1b and MODE2_EN bit is set to "0", MODE2 pin is ignored in DVS function, MODE1 pin is used to increase buck regulator as much as Bx_DVS_UP bit by issuing one pulse. And MODE0 pin is used to decrease buck regulator as much as Bx_DVS_DN bit by issuing one pulse. The pulse width is controlled trough MODE_PULSE bit (bit 3) of the BUCK23_DVS_CFG1 register. Buck regulator should be selected through BUCK_SEL bit in this mode. Whenever the voltage is updated through MODE pin, the voltage is updated in BUCKxOUT_DVS0 register so as application processor can check the current output voltage setting. When both pin has same logic level, then the buck voltage is not changed.

When SMART_MODE is set to 1b and MODE2_EN bit is set to 1b, MODE2 pin is used to select BUCK regulator to be increased or decreased through MODE1 and MODE0 pins.

Figure 17 shows DVS operation through MODE[2:0] pins when SMART_MODE bit is set to 1b.

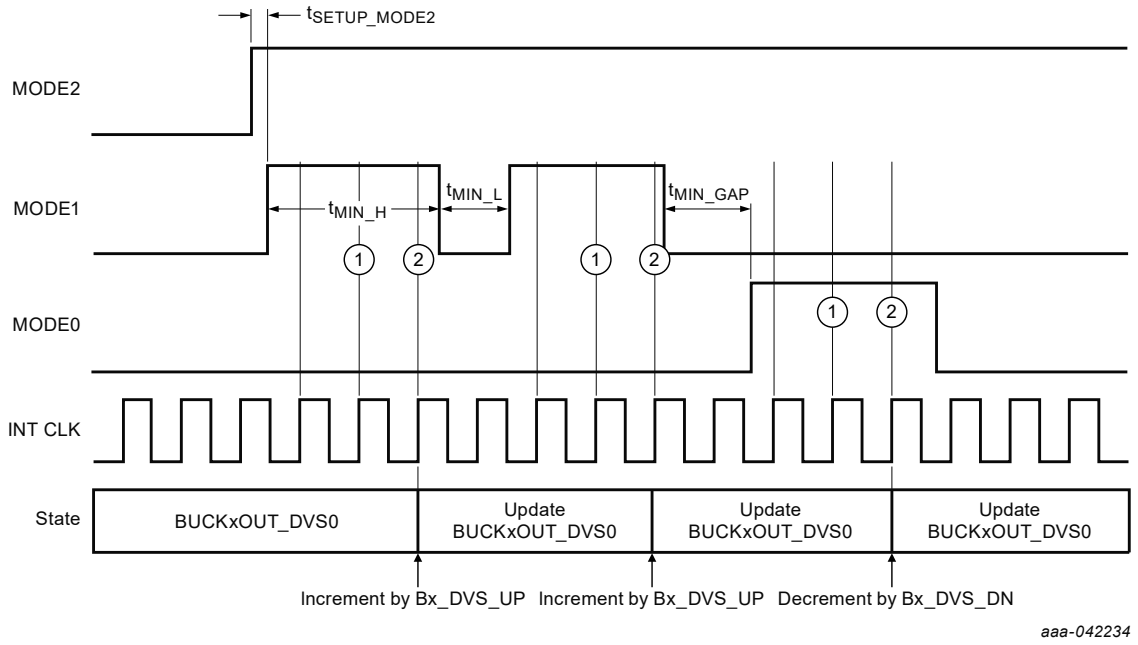



**Figure 17. MODE[2:0] pins operation at SMART_MODE = 1b, MODE2_EN = 1b**

MODE pins control requirements in SMART_MODE = 1b are:

1. MODE2 pin should be set within $t_{SETUP\_MODE2}$ before MODE1 or MODE0 pin is toggled
2. High Pulse hold time should be longer than $t_{MIN\_H}$
3. Low pulse hold time should be longer than $t_{MIN\_L}$
4. When MODE1 pin is toggled after MODE0 pin toggled and vice versa, it should be longer than $t_{MIN\_GAP}$.
5. Once detecting high pulse, the voltage is updated in BUCKxOUT_DVS0 register after two internal clocks.
6. Either MODE1 or MODE0 pin stay high, the buck regulator voltage is updated only once after two clocks.

The programmable voltage ramp-up and ramp-down are applied during the DVS voltage transition. The ramp rate is configured by Bx_RAMP[7:6] bits in each BUCKxCTRL registers.

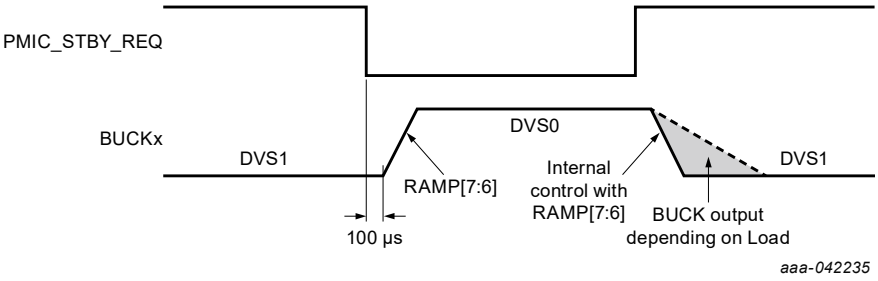



**Figure 18. DVS timing**

### 7.6.1.3 Overshoot improvement from PWM to PFM mode transient

The load transient response in PWM mode is improved compared to PFM mode, since the converter reacts faster on the load step and actively sinks energy on the load release. PCA9460 Buck regulator automatically enters PWM mode for 16 cycles after a heavy load release in order to bring the output voltage back to the regulation level faster. After 16 cycles of PWM mode, it automatically returns to PFM mode.

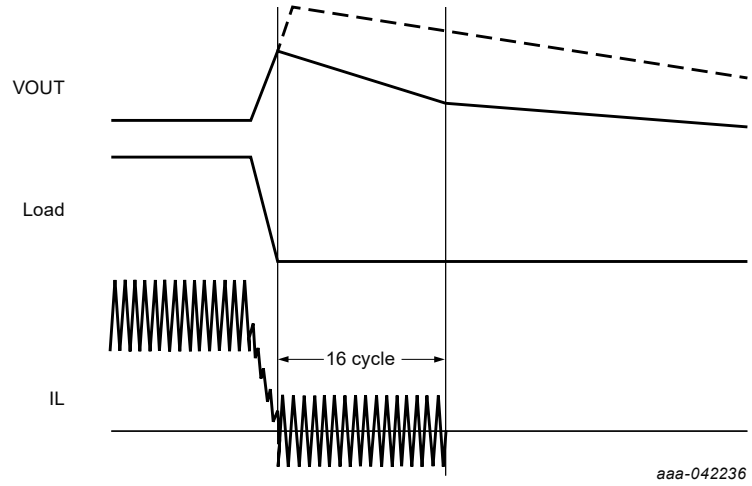



**Figure 19. Transition from PWM to PFM**

### 7.6.1.4 Low power mode

If BUCK is configured in low power mode, it turns internal circuity off to minimize quiescent current. The current is limited to IOUT_Max in Low Power Mode. BUCK2 and BUCK3 DVS feature also disabled in this mode. Therefore, low power mode should be used carefully not to exceed IOUT_Max current.

Each buck regulator has low power mode configuration bits in BUCKx_CTRL register.

**Table 13. Low power mode**

| BUCK_CTRL | | | | Reset Type | O |
|---|---|---|---|---|---|
| **Bit** | **Name** | **Type** | **Reset** | **Description** | |
| 5 to 4 | Bx_LPMODE | R/W | 11 | BUCK power mode<br>00b = Automatic transition mode<br>01b = Low power mode at STANDBY mode and DPSTANDBY mode<br>10b = Low power mode at DPSTANDBY mode<br>**11b = Normal mode** | |

If Bx_LPMODE bits are set to 00b, the buck regulator runs automatic transition mode between low power mode and normal mode depending on load current. When it is set to 01b, buck operates in normal mode at ACTIVE mode and in low power mode at STANDBY mode and DPSTANDBY mode. If it is set to 10b, the buck is in low power mode only at DPSTANDBY mode.

### 7.6.1.5 BUCK output limiting

Application processor may accidentally write higher voltage than absolute maximum voltage rating of its power input, it may cause significant damage on application processor. PCA9460 has registers to limit the maximum voltage to prevent such an incident.

BUCK2 and BUCK3 maximum / minimum output are limited by BUCKxOUT_MAX_LIMIT and BUCKxOUT_MIN_LIMIT registers, respectively. Even if Buck output is configured to higher than the limit voltage configured in BUCKxOUT_MAX_LIMIT registers or lower than the min limit voltage configured in BUCKxOUT_MIN_LIMIT registers, the actual buck output is clamped to the limiting voltage set by BUCKxOUT_MAX_LIMIT or BUCKxOUT_MIN_LIMIT registers.

### 7.6.2 LDO

The PCA9460 has five low quiescent LDOs. LDO_SVNS is supposed to supply SNVS core in application processor. This LDO features ultra-low quiescent current, 0.25 µA typical, since it is always ON when VSYS is valid. Each LDO is fully controlled through its respective LDOxCFG and LDOx_OUT registers. LDOxCFG registers enable the user to individually set the LDO configuration and enable and set the operational mode on each regulator using Lx_ENMODE bits [1:0]. While LDOx_OUT registers enable the user to individually set the output voltage according to Table 113 for LDO1; Table 118 for LDO2; Table 125 for LDO3; and Table 130 for LDO4.

Users can set LDO1 into Low Power Mode by setting the L1_LPMODE [1:0] bits on LDO1_CFG register (0x30).

The internal active discharge resistor is installed in each LDO regulator output to discharge voltage on output capacitors when the regulator is off. It is configurable through $I^2C$ register using the following:

- L1_AD bit (bit 7) on LDO1_OUT (0x31)
- Lx_AD bit (bit 4) on LDO2_CFG (0x32), LDO3_CFG (0x35), and LDO4_CFG (0x37)

**Table 14. LDO summary (PCA9460A)**

| LDO# | Input pin | Default VOUT (V) | VOUT range (V) | Step size (mV) | Default ON/ OFF | Current rating (mA) |
|---|---|---|---|---|---|---|
| LDO1 | INL1 | [1] | 0.6 to 1.95 | 50 | ON | 250 |
| LDO2 | INL | 3.3 | 0.8 to 3.3 | 50 | ON | 250 |
| LDO3 | INL | 3.3 | 0.8 to 3.3 | 50 | ON | 250 |
| LDO4 | INL | 1.8 | 0.8 to 3.3 | 50 | ON | 250 |
| LDO_SNVS | VSYS | 3.0 | 0.8 to 3.3 | 50 | ON | 10 |

[1] PCA9460A: 1.1 V, PCA9460B:0.6 V, PCA9460C: 1.2 V

The LDOSNVS regulator is fully controlled through the LDOSNVS_CFG register. Users can enable/disable the internal active discharge resistor using LSNVS_AD bit (Bit 7); enable/disable the regulator using LS_ENMODE bit (bit 6); and use the L_SNVS_OUT bits [5:0] to set the output voltage according to Table 133.

### 7.6.3 Regulator protection

Each regulator output voltage configuration register is protected by lock key. Unlock key must be written with 01011100 (0x5C) to UNLOCK_KEY [7:0] bits in REG_LOCK (0x4E) register before updating the registers. Below are protected registers.

1. BUCK output configuration registers : BUCK1OUT, BUCK4OUT
2. BUCK2, 3 Min/Max output configuration registers : BUCK2OUT_MAX_LIMIT, BUCK2OUT_MIN_LIMIT, BUCK3OUT_MAX_LIMIT, BUCK3OUT_MIN_LIMIT.
3. LDO output configuration registers : LDO1_OUT, LDO2_OUT_L, LDO2_OUT_H, LDO3_OUT, LDO4_OUT

### 7.6.4 Current limit protection

In case a regulator exceeds the current limit (ILIM parameter for the BUCK regulators or ILIMT for the linear regulators) of each target, the output of the regulator will fall below POK (Output Power good) threshold caused by overcurrent limit, then VRFLT1_INT register will generate an interrupt and system transitions to Fault_SD state. Please refer to “Voltage regulator fault in RUN state” fault source in Section 7.4.6 "FAULT_SD state" for details.

## 7.7 Load switch and LED driver

PCA9460 integrates four 150mΩ PMOS switch configurable to Load switch or LED driver through $I^2C$.

When an LSWx_CFG bit in LSW_CFG register is set to 0b, the LSW is configured as Load switch. It is controlled by each LSWx_EN bits in LSW_EN_CTRL register, which provides ON/OFF control automatically in different modes. When it is enabled, it soft-starts to reduce inrush current.

**Table 15. Load SW Enable table**

| LSWx_EN | SNVS State | RUN state | | |
|---|---|---|---|---|
| | | Active Mode | STANDBY | DPSTANDBY |
| 00 | OFF | OFF | OFF | OFF |
| 01 | OFF | ON | ON | ON |
| 10 | OFF | ON | ON | OFF |
| 11 | OFF | ON | OFF | OFF |

When an LSWx_CFG bit is set to 1b, the LSW is configured as LED driver, and its behavior is determined by LEDx_CFG registers including enable mode and brightness configuration.

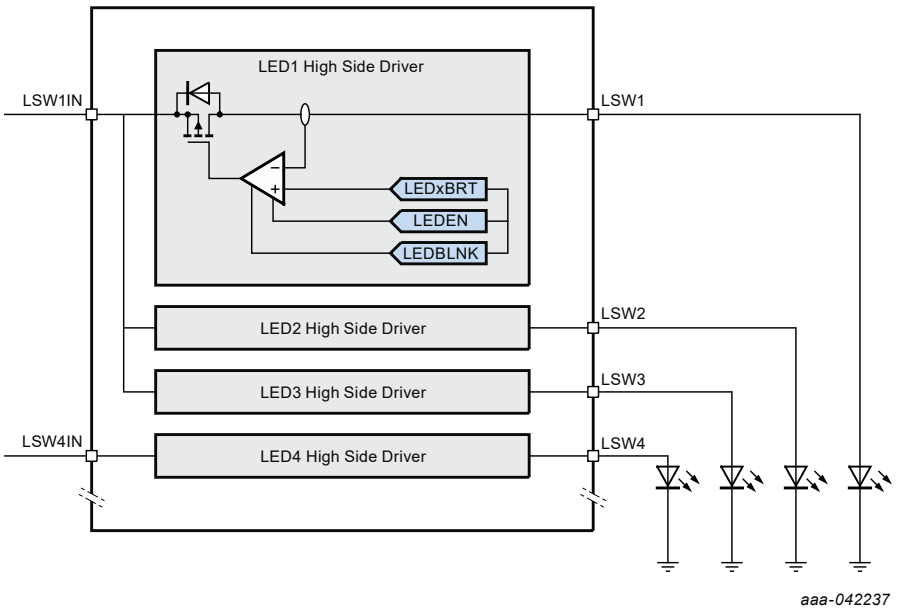



**Figure 20. LED Driver block diagram**

Each LED channel can be assigned to one of constant ON, blinking pattern 1 and blinking pattern 2. Constant ON is to turn ON LED with configured LED brightness until it is forcedly off though $I^2C$.

PCA9460 supports two independent blink patterns which is generated by each LEDRAMP register and LEDBLNK register. The Blink pattern always start with OFF time, and then ramp up to $I_{LED\_BRT}$ by increasing PWM duty cycle from 0 % to 100 % configured in LEDRAMP register. The ramp up time is determined by PWM duty step size(Px_UP_STEP) and delay time(Px_UP_DLY). Once the current reach the target, the LED channel stays for $T_{ON}$. a blink pattern ends up with Ramping down by decreasing PWM duty cycle from 100 % to 0 % configured in LEDRAMP register. The ramp down time is determined by PWM duty step size(Px_DN_STEP) and delay time(Px_DN_DLY). This pattern is repeated until any LED channel doesn't select the pattern any longer. Update on the pattern like brightness change or ON/OFF time change during a BLINK mode takes place in next period.

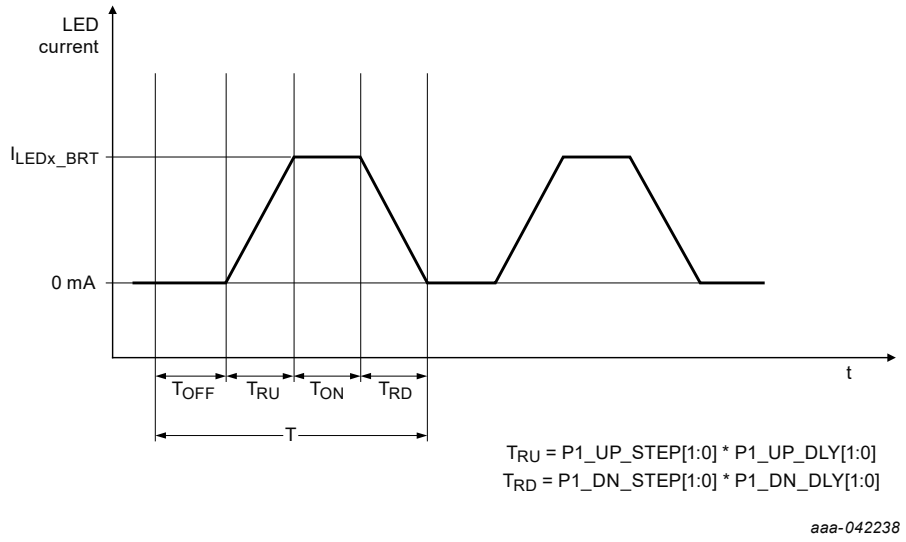



**Figure 21. LED Blink Pattern**

## 7.8 Mode selection

### 7.8.1 MODE0, MODE1, MODE2

MODE[2:0] pins are purposed to control DVS( Dynamic voltage scaling ) for BUCK 2 and BUCK3 by default. Those pins can be configured to control LDO2 voltage selection or each load switch ON/OFF through MODEPIN_CFG register as well.

If any MODE pin is configured to any bits other than 00b in MODEPIN_CFG register, the internal MODE pin in DVS control block is set low. For example, if MODE2_CFG bits are configured to 001b, then MODE2 pin is used to control LDO2 voltage selection, and the pin in DVS control block is set low.

If any MODE pin is not configured to LDO2 voltage selection, internal LDO2_VSEL is set low.

Load switch which is not configured to any MODE pin is controlled by only $I^2C$ register bits, LSWx_EN[1:0] bits.

**Table 16. 0x0D – MODEPIN_CFG**

*Reset Type: 0*

| Bit | Name | Type | Reset | Description |
|---|---|---|---|---|
| 7 to 6 | MODE0_CFG | R/W | 00 | MODE0 pin configuration<br>**00b = DVS control**<br>01b = LDO2 voltage selection<br>10b = LSW1 ON/OFF control<br>11b = LSW4 ON/OFF control |
| 5 to 3 | MODE1_CFG | R/W | 000 | MODE1 pin configuration<br>**000b = DVS control**<br>001b = LDO2 voltage selection<br>010b = LSW1 ON/OFF control<br>011b = LSW2 ON/OFF control<br>100b = LSW3 ON/OFF control<br>101b-111b = LSW4 ON/OFF control |
| 2 to 0 | MODE2_CFG | R/W | 000 | MODE2 pin configuration<br>**000b = DVS control** |

**Table 16. 0x0D – MODEPIN_CFG**...*continued*

*Reset Type: 0*

| Bit | Name | Type | Reset | Description |
|---|---|---|---|---|
| | | | | 001b = LDO2 voltage selection<br>010b = LSW1 ON/OFF control<br>011b = LSW2 ON/OFF control<br>100b = LSW3 ON/OFF control<br>101b-111b = LSW4 ON/OFF control |

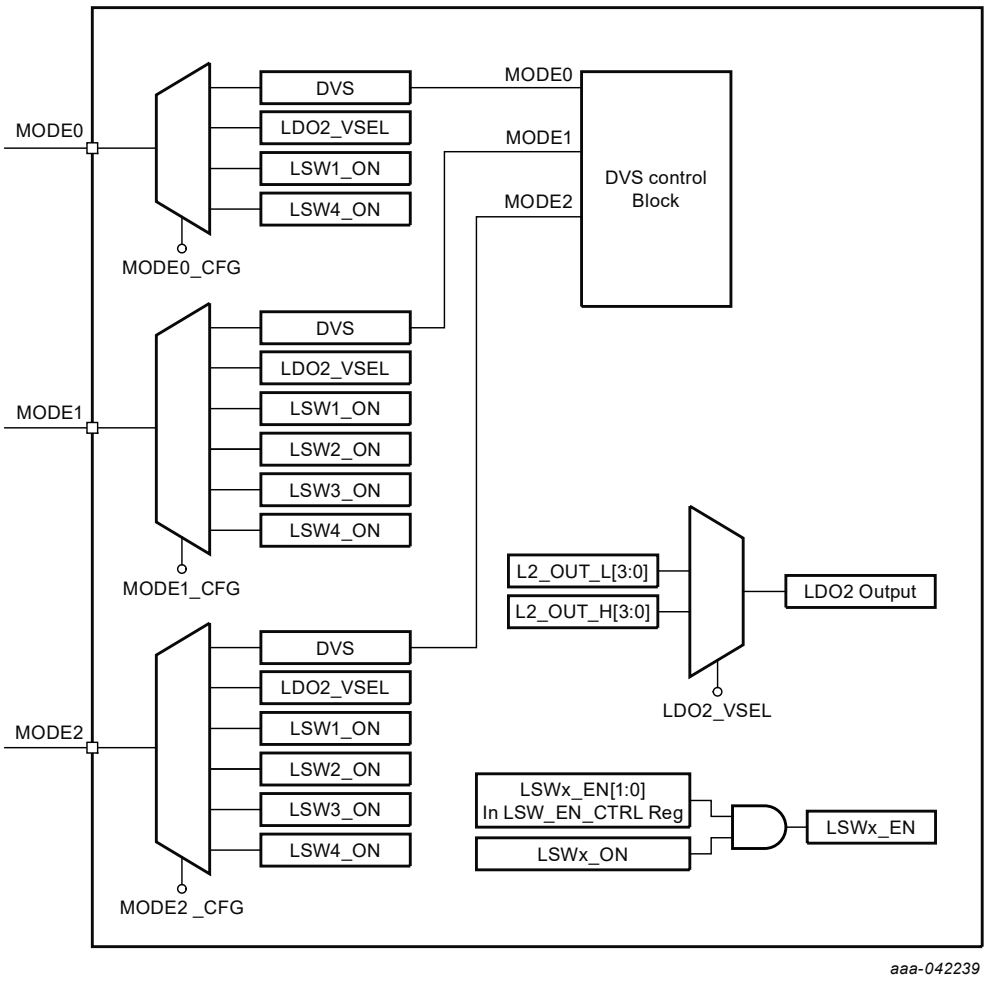



**Figure 22. MODE[2:0] pins multiplex**

## 7.9 Interrupt management

The IRQ_B pin is an interface to the software-controlled system that indicates any interrupt bit status change of INT1 register. The IRQ_B pin is pulled low when any unmasked interrupt bit status is changed, and it is released high once application processor read INT1 register.

The INT1 bits are latched to 1 whenever corresponding INT1_STATUS1 bit is changed and the latch is cleared when the INT1 register is read. The INT1_MASK bits are used to enable or disable individual interrupt bits of INT1 register. The INT1_STATUS1 register indicates the current status and is not latched.

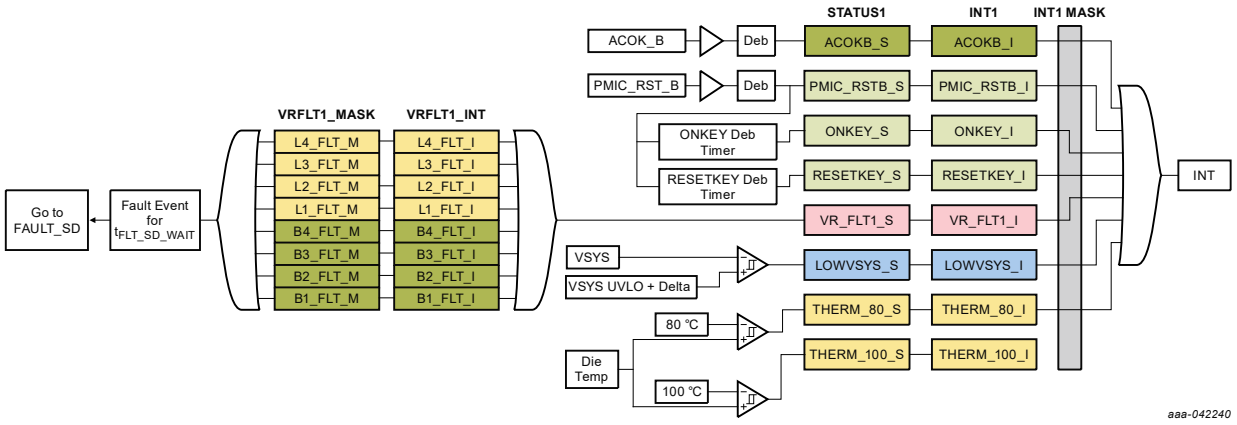



**Figure 23. Interrupt diagram**

# 8 Software interface

PCA9460 implements I$^2$C-bus slave interface and it interfaces with the host system. The host processor can issue commands, monitor status and receive response through this bus. A detailed description of the I$^2$C-bus specification, with applications, is given in UM10204, https://www.nxp.com/docs/en/user-guide/UM10204.pdf[Ref. 4]. PCA9460 supports I$^2$C-bus data transfers in Standard-mode (100 kbit/s), Fast-mode (400 kbit/s) and Fast-mode plus (1 Mbit/s). See Table 17.

**Table 17. I$^2$C address at Power-On Reset**

| | 7-bit Slave Address | 8-bit Write Address | 8-bit Read Address |
|---|---|---|---|
| Default | 0x32, 0b 011 0010 | 0x64, 0b 0110 0100 | 0x65, 0b 0110 0101 |
| OTP1 | 0x33, 0b 011 0011 | 0x66, 0b 0110 0110 | 0x67, 0b 0110 0111 |
| OTP2 | 0x36, 0b 011 0110 | 0x6C, 0b 0110 1100 | 0x6D, 0b 0110 1101 |
| OTP3 | 0x37, 0b 011 0111 | 0x6E, 0b 0110 1110 | 0x6F, 0b 0110 1111 |

### I$^2$C register reset type

There are two type of registers: type O and type S. The differences between them relates to the different conditions that RESET the contents and its corresponding functionality to the default values for those specific registers. Those conditions are shown below for each register type. For more details on whether a register is type S or O refer to Table 18.

Type S : (VSYS < $V_{SYS\_UVLO}$) || (VINT_POK) || ( SW_RST_KEY = 0x09)

Type O : ( VSYS < $V_{SYS\_UVLO}$ ) || (VINT_POK) || ( Cold Reset ) || ( Warm Reset ) || ( Falling edge of PMIC_ON_SRC) || (SW_RST_KEY=0x05) || (SW_RST_KEY=0x09) || ( FAULT_SD ) || ( Thermal SD )

## 8.1 Register map

**Table 18. Register map**

| Add | Name | Description | | | | | | | | R/W | Reset Type | Reset Value[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | | A | B | C |
| 00h | Device_ID | CHIP_ID | | | | REV_ID | | | | R | S | 0x30 | 0x30 | 0x30 |
| 01h | OTP_Ver | OTP_VER | | | | | | | | R | S | 0x00 | 0x10 | 0x20 |
| 02h | INT1 | ACOKB_I | PMIC_RSTB_I | ONKEY_I | RESETKEY_I | VR_FLT1_I | LOWVSYS_I | THERM_80_I | THERM_100_I | R/C | S | 0x00 | 0x00 | 0x00 |

**Table 18. Register map**...*continued*

| Add | Name | Description | | | | | | | | R/W | Reset Type | Reset Value[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | | A | B | C |
| 03h | INT1_MSK | ACOKB_M | PMIC_RSTB_M | ONKEY_M | RESETKEY_M | VR_FLT1_M | LOWVSYS_M | THERM_80_M | THERM_100_M | R/W | S | 0xFF | 0xFF | 0xFF |
| 04h | INT1_STATUS | ACOKB_S | PMIC_RSTB_S | ONKEY_S | RESETKEY_S | VR_FLT12S | LOWVSYS_S | THERM_80_S | THERM_100_S | R | S | 0x00 | 0x00 | 0x00 |
| 05h | VRFLT1_INT | L4_FLT_I | L3_FLT_I | L2_FLT_I | L1_FLT_I | B4_FLT_I | B3_FLT_I | B2_FLT_I | B1_FLT_I | R/W/C | S | 0x00 | 0x00 | 0x00 |
| 06h | VRFLT1_MASK | L4_FLT_M | L3_FLT_M | L2_FLT_M | L1_FLT_M | B4_FLT_M | B3_FLT_M | B2_FLT_M | B1_FLT_M | R/W | S | 0xFF | 0xFF | 0xFF |
| 07h | PWR_STATE | PWR_STAT | | | | PWR_MODE | | | | R | S | 0x00 | 0x00 | 0x00 |
| 08h | RESET_CTRL | WDOGB_CFG | | PMIC_RST_CFG | | TRE START | RSVD | RSVD | RSVD | R/W | S | 0x20 | 0x20 | 0x20 |
| 09h | SW_RST | SWRST | | | | | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 0Ah | PWR_SEQ_CTRL | PMIC_RST_B_ON | ACOK_B_ON | PMIC_RST_B_DEB | ACOK_B_OSTMR | PSQ_TON_STEP | | PSQ_TOFF_STEP | | R/W | S | 0x06 | 0x06 | 0x06 |
| 0Bh | SYS_CFG1 | LOW_VSYS | | STANDBY_CFG | RESETKEY_TIMER | | | TFLT_SD_WAIT | THERM_SD_DIS | R/W | O | 0x54 | 0x54 | 0x54 |
| 0Ch | SYS_CFG2 | ONKEY_TIMER | | PWR_SAVE | | RSVD | POK_PU | VSYS_UVLO | | R/W | S | 0x71 | 0x71 | 0x71 |
| 0Dh | MODEPIN_CFG | MODE0_CFG | | MODE1_CFG | | | MODE2_CFG | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 0Eh-0Fh | RESERVED | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | | | 0x00 | 0x00 | 0x00 |
| 10h | BUCK1CTRL | RSVD | RSVD | B1_LPMODE | | B1_AD | B1_FPWM | B1_ENMODE | | R/W | O | 0x39 | 0x39 | 0x39 |
| 11h | BUCK1OUT | RSVD | B1_OUT | | | | | | | R/W | O | 0x30 | 0x30 | X030 |
| 12h | BUCK23_DVS_CFG1 | B2_DVS_UP | B2_DVS_DN | B3_DVS_UP | B3_DVS_DN | MODE_PULSE | SMART_MODE | MODE2_EN | BUCK_SEL | R/W | O | 0x00 | 0x00 | 0x00 |
| 13h | BUCK23_DVS_CFG2 | B2_DVS_CTRL | | B3_DVS_CTRL | | RSVD | RSVD | RSVD | RSVD | R/W | O | 0x00 | 0x00 | 0x00 |
| 14h | BUCK2CTRL | B2_RAMP | | B2_LPMODE | | B2_AD | B2_FPWM | B2_ENMODE | | R/W | O | 0x79 | 0x79 | 0x79 |
| 15h | BUCK2OUT_DVS0 | RSVD | B2_DVS0 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 16h | BUCK2OUT_DVS1 | RSVD | B2_DVS1 | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 17h | BUCK2OUT_DVS2 | RSVD | B2_DVS2 | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 18h | BUCK2OUT_DVS3 | RSVD | B2_DVS3 | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 19h | BUCK2OUT_DVS4 | RSVD | B2_DVS4 | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 1Ah | BUCK2OUT_DVS5 | RSVD | B2_DVS5 | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 1Bh | BUCK2OUT_DVS6 | RSVD | B2_DVS6 | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 1Ch | BUCK2OUT_DVS7 | RSVD | B2_DVS7 | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 1Dh | BUCK2OUT_STBY | RSVD | B2_DVS_STBY | | | | | | | R/W | O | 0x18 | 0x18 | 0x18 |
| 1Eh | RESERVED | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | | | 0x00 | 0x00 | 0x00 |
| 1Fh | BUCK2OUT | RSVD | B2_MAX_LIMIT | | | | | | | R/W | O | 0x38 | 0x38 | X038 |

**Table 18. Register map**...*continued*

| Add | Name | Description | | | | | | | | R/W | Reset Type | Reset Value[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | | A | B | C |
| | _MAX_LIMIT | | | | | | | | | | | | | |
| 20h | BUCK2OUT _MIN_LIMIT | RSVD | B2_MIN_LIMIT | | | | | | | R/W | O | 0x08 | 0x08 | 0x08 |
| 21h | BUCK3CTRL | B3_RAMP | | B3_LPMODE | | B3_AD | B3 _FPWM | B3_ENMODE | | R/W | O | 0x79 | 0x79 | 0x79 |
| 22h | BUCK3OUT _DVS0 | RSVD | B3_DVS0 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 23h | BUCK3OUT _DVS1 | RSVD | B3_DVS1 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 24h | BUCK3OUT _DVS2 | RSVD | B3_DVS2 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 25h | BUCK3OUT _DVS3 | RSVD | B3_DVS3 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 26h | BUCK3OUT _DVS4 | RSVD | B3_DVS4 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 27h | BUCK3OUT _DVS5 | RSVD | B3_DVS5 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 28h | BUCK3OUT _DVS6 | RSVD | B3_DVS6 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 29h | BUCK3OUT _DVS7 | RSVD | B3_DVS7 | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 2Ah | BUCK3OUT _STBY | RSVD | B3_DVS_STBY | | | | | | | R/W | O | 0x20 | 0x20 | 0x20 |
| 2Bh | RESERVED | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | | | 0x00 | 0x00 | 0x00 |
| 2Ch | BUCK3OUT _MAX_LIMIT | RSVD | B3_MAX_LIMIT | | | | | | | R/W | O | 0x38 | 0x38 | 0x38 |
| 2Dh | BUCK3OUT _MIN_LIMIT | RSVD | B3_MIN_LIMIT | | | | | | | R/W | O | 0x08 | 0x08 | 0x08 |
| 2Eh | BUCK4_CTRL | | RSVD | B4_LPMODE | | B4_AD | B4 _FPWM | B4_ENMODE | | R/W | O | 0x39 | 0x39 | 0x39 |
| 2Fh | BUCK4OUT | RSVD | B4_OUT | | | | | | | R/W | O | 0x14 | 0x14 | 0x18 |
| 30h | LDO1_CFG | L1_CSEL | | L1_LLSEL | | L1_LPMODE | | L1_ENMODE | | R/W | O | 0x9D | 0x9D | 0x9D |
| 31h | LDO1_OUT | L1_AD | L1_INL1 _MDET | L1_INL1 _VSEL | L1_OUT | | | | | R/W | O | 0x8A | 0x80 | 0x8C |
| 32h | LDO2_CFG | RSVD | RSVD | RSVD | L2_AD | RSVD | RSVD | L2_ENMODE | | R/W | O | 0x11 | 0x11 | 0x11 |
| 33h | LDO2_OUT_L | | | L2_OUT_L | | | | | | R/W | O | 0x32 | 0x32 | 0x32 |
| 34h | LDO2_OUT_H | | | L2_OUT_H | | | | | | R/W | O | 0x14 | 0x14 | X014 |
| 35h | LDO3_CFG | RSVD | RSVD | RSVD | L3_AD | RSVD | RSVD | L3_ENMODE | | R/W | O | 0x11 | 0x11 | 0x11 |
| 36h | LDO3_OUT | | | L3_OUT | | | | | | R/W | O | 0x32 | 0x32 | X032 |
| 37h | LDO4_CFG | RSVD | RSVD | RSVD | L4_AD | RSVD | RSVD | L4_ENMODE | | R/W | O | 0x11 | 0x11 | X011 |
| 38h | LDO4_OUT | | | L4_OUT | | | | | | R/W | O | 0x14 | 0x14 | 0x14 |
| 39h | LDOSNVS _CFG | LSNVS _AD | LS_EN MODE | L_SNVS_OUT | | | | | | R/W | O | 0xEC | 0xEC | 0xEC |
| 3Ah-3Fh | RESERVED | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | | | 0x00 | 0x00 | 0x00 |
| 40h | LSW1_CTRL | LSW1 _CFG | RSVD | RSVD | LSW1_AD | RSVD | RSVD | LSW1_EN | | R/W | O | 0x11 | 0x11 | 0x11 |
| 41h | LSW2_CTRL | LSW2 _CFG | RSVD | RSVD | LSW2_AD | RSVD | RSVD | LSW2_EN | | R/W | O | 0x11 | 0x11 | 0x11 |
| 42h | LSW3_CTRL | LSW3 | RSVD | RSVD | LSW3_AD | RSVD | RSVD | LSW3_EN | | R/W | O | 0x11 | 0x11 | 0x11 |

**Table 18. Register map**...*continued*

| Add | Name | Description | | | | | | | | R/W | Reset Type | Reset Value[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | | A | B | C |
| | | _CFG | | | | | | | | | | | | |
| 43h | LSW4_CTRL | LSW4 _CFG | RSVD | RSVD | LSW4_AD | RSVD | RSVD | LSW4_EN | | R/W | O | 0x11 | 0x11 | 0x11 |
| 44h | LED1_CTRL | LED1_EN | | RSVD | LED1_BRT | | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 45h | LED2_CTRL | LED2_EN | | RSVD | LED2_BRT | | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 46h | LED3_CTRL | LED3_EN | | RSVD | LED3_BRT | | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 47h | LED4_CTRL | LED4_EN | | RSVD | LED4_BRT | | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 48h | LED_P1 _RAMP | P1_UP_STEP | | P1_UP_DLY | | P1_DN_STEP | | P1_DN_DLY | | R/W | O | 0x00 | 0x00 | 0x00 |
| 49h | LED_P1 _BLNK | LEDTON1 | | | | LEDTOFF1 | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 4Ah | LED_P2 _RAMP | P2_UP_STEP | | P2_UP_DLY | | P2_DN_STEP | | P2_DN_DLY | | R/W | O | 0x00 | 0x00 | 0x00 |
| 4Bh | LED_P2 _BLNK | LEDTON2 | | | | LEDTOFF2 | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| 4Ch-4Dh | RESERVED | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | | | 0x00 | 0x00 | 0x00 |
| 4Eh | REG_LOCK | UNLOCK_KEY | | | | | | | | R/W | O | 0x00 | 0x00 | 0x00 |
| Note1. A = PCA9460A, B = PCA9460B, C = PCA9460C | | | | | | | | | | | | | | |

[1] A = PCA9460, B = PCA9460B, C = PCA9460C

## 8.2 Register details

### 8.2.1 Device_ID

The device identification code stores a unique identifier for each version and/or revision of a PCA9460, so that the connected processor recognizes it automatically.

**Table 19. Device_ID register (address 00h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | CHIP_ID | | | | CHIP_REV | | | |
| **Reset** | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **Access** | R | R | R | R | R | R | R | R |

**Table 20. Device_ID register (address 00h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 4 | CHIP_ID | Chip ID<br>**0011 —** PCA9460 (default) |
| 3 to 0 | CHIP_REV | Chip Revision<br>**0000 —** revision 0 (default) |

### 8.2.2 OTP_VER

OTP version information

**Table 21. OTP_VER register (address 01h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | OTP_VER | | | | OTP_REV | | | |
| **Reset**[1] | — | — | — | — | — | — | — | — |
| **Access** | R | R | R | R | R | R | R | R |

[1] The reset value depends on the specific otp version as shown in Table 22.

**Table 22. OTP_VER register (address 01h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 4 | OTP_VER | OTP version for each PCA9460 variance<br>**0000 —** PCA9460A<br>**0001 —** PCA9460B<br>**0010 —** PCA9460C<br>…<br>**1111 —** Reserved |
| 3 to 0 | OTP_REV | OTP minor change update<br>**0000 —** revision 0<br>**0001 —** revision 1<br>…<br>**1111 —** Reserved |

### 8.2.3 INT1

Interrupt source register. Either of unmasked register bits is set to 1, IRQB pin is pulled low. This register is Read and Clear.

**Table 23. INT1 register (address 02h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | ACOKB_I | PMIC_ RSTB_I | ONKEY_I | RESETKEY_I | VR_FLT1_I | LOWVSYS_I | THERM_80_I | THERM_ 100_I |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/C | R/C | R/C | R/C | R/C | R/C | R/C | R/C |

**Table 24. INT1 register (address 02h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | ACOKB_I | ACOKB interrupt<br>**0 —** ACOKB_S bit has not been changed (default)<br>**1 —** ACOKB_S bit has been changed |
| 6 | PMIC_RSTB_I | PMIC_RSTB_I interrupt<br>**0 —** PMIC_RSTB_S bit has not been changed (default)<br>**1 —** PMIC_RSTB_S bit has been changed |
| 5 | ONKEY_I | ON Key timer interrupt<br>**0 —** ONKEY_S bit has not been changed (default)<br>**1 —** ONKEY_S bit has been changed |
| 4 | RESETKEY_I | RESET Key timer interrupt<br>**0 —** RESETKEY_S bit has not been changed (default)<br>**1 —** RESETKEY_S bit has been changed |

**Table 24. INT1 register (address 02h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| 3 | VR_FLT1_I | Voltage regulator Group1 Fault<br>**0 —** VR_FLT1_S bit has not been changed (default)<br>**1 —** VR_FLT1_S bit has been changed |
| 2 | LOWVSYS_I | Low-SYS Voltage interrupt<br>**0 —** LOWVSYS_S bit has not been changed (default)<br>**1 —** LOWVSYS_S bit has been changed |
| 1 | THERM_80_I | Die temperature 80 °C interrupt<br>**0 —** THERM_80_S bit has not been changed (default)<br>**1 —** THERM_80_S bit has been changed |
| 0 | THERM_100_I | Die temperature 100 °C interrupt<br>**0 —** THERM_100_S bit has not been changed (default)<br>**1 —** THERM_100_S bit has been changed |

### 8.2.4 INT1_MASK

**Table 25. INT1_MASK register (address 03h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | ACOKB_M | PMIC_ RSTB_M | ONKEY_M | RESETKEY_ M | VR_FLT1_M | LOWVSYS_M | THERM_ 80_M | THERM_ 100_M |
| **Reset** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 26. INT1_MASK register (address 03h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | ACOKB_M | ACOKB_I interrupt mask bit<br>**0 —** Enable ACOKB_I interrupt<br>**1 —** Mask ACOKB_I interrupt (default) |
| 6 | PMIC_RSTB_M | PMIC_RSTB_I interrupt mask bit<br>**0 —** Enable PMIC_RSTB_I interrupt<br>**1 —** Mask PMIC_RSTB_I interrupt (default) |
| 5 | ONKEY_M | ONKEY_I interrupt mask bit<br>**0 —** Enable ONKEY_I interrupt<br>**1 —** Mask ONKEY_I interrupt (default) |
| 4 | RESETKEY_M | RESETKEY_I interrupt mask bit<br>**0 —** Enable RESETKEY_I interrupt<br>**1 —** Mask RESETKEY_I interrupt (default) |
| 3 | VR_FLT1_M | VR_FLT1I interrupt mask bit<br>**0 —** Enable VR_FLT1I interrupt<br>**1 —** Mask VR_FLT1I interrupt (default) |
| 2 | LOWVSYS_M | LOWVINI interrupt mask bit<br>**0 —** Enable LOWVINI interrupt<br>**1 —** Mask LOWVINI interrupt (default) |
| 1 | THERM_80_M | THERM_80 interrupt mask bit<br>**0 —** Enable THERM_80 interrupt<br>**1 —** Mask THERM_80 interrupt (default) |
| 0 | THERM_100_M | THERM_100 interrupt mask bit<br>**0 —** Enable THERM_100 interrupt |

**Table 26. INT1_MASK register (address 03h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **1 —** Mask THERM_100 interrupt (default) |

### 8.2.5 INT1_STATUS

STATUS register shows current status. Any status bit change sets corresponding interrupt bit to 1.

**Table 27. INT1_STATUS register (address 04h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | ACOKB_S | PMIC_ RSTB_S | ONKEY_S | RESETKEY_ S | VR_FLT1_S | LOWVSYS_S | THERM_ 80_S | THERM_ 100_S |
| **Reset** | — | — | — | — | — | — | — | — |
| **Access** | R | R | R | R | R | R | R | R |

**Table 28. INT1_STATUS register (address 04h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | ACOKB_S | ACOK_B pin status after debounce time<br>**0 —** ACOK_B pin is low<br>**1 —** ACOK_B pin is high |
| 6 | PMIC_RSTB_S | PMIC_RST_B pin status<br>**0 —** PMIC_RST_B pin is low<br>**1 —** PMIC_RST_B pin is high |
| 5 | ONKEY_S | ONKEY status bit<br>**0 —** PMIC_RST_B pin is not low for ONKEY timer<br>**1 —** PMIC_RST_B pin is low for ONKEY timer |
| 4 | RESETKEY_S | RESETKEY status bit<br>**0 —** PMIC_RST_B pin is not low for RESETKEY timer<br>**1 —** PMIC_RST_B pin is low for RESETKEY timer |
| 3 | VR_FLT1_S | Voltage Regulator Fault status, See 0x40 Register.<br>**0 —** All voltage regulators are OK<br>**1 —** Either of voltage regulators is in Fault state |
| 2 | LOWVSYS_S | VSYS low voltage status<br>**0 —** Enable LOWVINI interrupt<br>**1 —** Mask LOWVINI interrupt |
| 1 | THERM_80_S | Die temperature 80 °C status<br>**0 —** Die temperature is below 80 °C<br>**1 —** Die temperature is above 80 °C |
| 0 | THERM_100_S | Die temperature 100 °C status<br>**0 —** Die temperature is below 100 °C<br>**1 —** Die temperature is above 100 °C |

### 8.2.6 VRFLT1_INT

Voltage regulator fault interrupt register. It is latched to 1 once corresponding regulator is detected until overwriting "1" to the register. If "1" is overwritten, the corresponding bit is newly updated by current status.

**Table 29. VRFLT1_INT register (address 05h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | L4_FLT_I | L3_FLT_I | L2_FLT_I | L1_FLT_I | B4_FLT_I | B3_FLT_I | B2_FLT_I | B1_FLT_I |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W/C | R/W/C | R/W/C | R/W/C | R/W/C | R/W/C | R/W/C | R/W/C |

**Table 30. VRFLT1_INT register (address 05h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | L4_FLT_I | LDO4 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** LDO4 output is good or LDO4 is OFF (default)<br>**1 —** LDO4 output falls below 80 % of target |
| 6 | L3_FLT_I | LDO3 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** LDO3 output is good or LDO3 is OFF (default)<br>**1 —** LDO3 output falls below 80 % of target |
| 5 | L2_FLT_I | LDO2 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** LDO2 output is good or LDO2 is OFF (default)<br>**1 —** LDO2 output falls below 80 % of target |
| 4 | L1_FLT_I | LDO1 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** LDO1 output is good or LDO1 is OFF (default)<br>**1 —** LDO1 output falls below 80 % of target |
| 3 | B4_FLT_I | BUCK4 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** BUCK4 output is good or BUCK4 is OFF (default)<br>**1 —** BUCK4 output is below 80 % |
| 2 | B3_FLT_I | BUCK3 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** BUCK3 output is good or BUCK3 is OFF (default)<br>**1 —** BUCK3 output falls below 80 % of target |
| 1 | B2_FLT_I | BUCK2 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** BUCK2 output is good or BUCK2 is OFF (default)<br>**1 —** BUCK2 output falls below 80 % of target |
| 0 | B1_FLT_I | BUCK1 Fault interrupt, deglitched with $t_{DEB\_POKB}$<br>**0 —** BUCK1 output is good or BUCK1 is OFF (default)<br>**1 —** BUCK1 output falls below 80 % of target |

### 8.2.7 VRFLT1_MASK

VR fault mask bit. Once the bit is masked, PCA9460 doesn’t enter Fault shutdown even if fault condition of corresponding regulator happens

**Table 31. VRFLT1_MASK register (address 06h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | L4_FLT_M | L3_FLT_M | L2_FLT_M | L1_FLT_M | B4_FLT_M | B3_FLT_M | B2_FLT_M | B1_FLT_M |
| **Reset** | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 32. VRFLT1_MASK register (address 06h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | L4_FLT_M | LDO4 FLT mask |

**Table 32. VRFLT1_MASK register (address 06h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **0 —** Unmask<br>**1 —** Masked (default) |
| 6 | L3_FLT_M | LDO3 FLT mask<br>**0 —** Unmask<br>**1 —** Masked (default) |
| 5 | L2_FLT_M | LDO2 FLT mask<br>**0 —** Unmask<br>**1 —** Masked (default) |
| 4 | L1_FLT_M | LDO1 FLT mask<br>**0 —** Unmask<br>**1 —** Masked (default) |
| 3 | B4_FLT_M | BUCK4 FLT mask<br>**0 —** Unmask<br>**1 —** Masked (default) |
| 2 | B3_FLT_M | BUCK3 FLT mask<br>**0 —** Unmask<br>**1 —** Masked (default) |
| 1 | B2_FLT_M | BUCK2 FLT mask<br>**0 —** Unmask<br>**1 —** Masked (default) |
| 0 | B1_FLT_M | BUCK1 FLT mask<br>**0 —** Unmask<br>**1 —** Masked (default) |

### 8.2.8 PWR_STATE

Power state register shows current PCA9460 power states and modes.

**Table 33. PWR_STATE register (address 07h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | PWR_STAT | | | | PWR_MODE | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R | R | R | R | R | R | R | R |

**Table 34. PWR_STATE register (address 07h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 4 | PWR_STAT | Current PCA9460 STATES<br>**0000 —** OFF (default)<br>**0100 —** SNVS<br>**0101 —** PWRUP<br>**1000 —** RUN<br>**1100 —** PWRDN<br>**1110 —** FAULT_SD<br>**others —** Reserved |
| 3 to 0 | PWR_MODE | Current PCA9460 MODE, only effective at RUN state<br>**0000 —** Active mode – DVS0 (default)<br>**0001 —** Active mode – DVS1<br>**0010 —** Active mode – DVS2 |

**Table 34. PWR_STATE register (address 07h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **0011 —** Active mode – DVS3<br>**0100 —** Active mode – DVS4<br>**0101 —** Active mode – DVS5<br>**0110 —** Active mode – DVS6<br>**0111 —** Active mode – DVS7<br>**1000 —** STANDBY MODE<br>**1010 —** DP_STANDBYMODE<br>**others —** Reserved |

### 8.2.9 RESET_CTRL

Reset behavior configuration register

**Table 35. RESET_CTRL register (address 08h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | WDOGB_CFG | | PMIC_RST_CFG | | TRESTART | RSVD | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 36. RESET_CTRL register (address 08h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | WDOGB_CFG | When WDOG_B is asserted to low, PMIC reset behavior<br>**00 —** WDOG_B reset is disabled (default)<br>**01 —** Warm reset, POR_B pin is asserted low for 20 ms<br>**10 and 11 —** Cold Reset, all voltage regulators are recycled |
| 5 to 4 | PMIC_RST_CFG | When PMIC_RST_B is asserted to low, PMIC reset behavior<br>**00 —** PMIC_RST_B reset is disabled<br>**01 —** Warm Reset, POR_B pin is asserted low for 20 ms<br>**10 and 11 —** Cold Reset, all voltage regulators are recycled (default) |
| 3 | TRESTART | Time to stay regulators off during Cold reset<br>**0 —** 250 ms (default)<br>**1 —** 500 ms |
| 2 to 0 | RSVD | Reserved |

### 8.2.10 SW_RST

Software reset register

**Table 37. SW_RST register (address 09h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | SW_RST_KEY | | | | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 38. SW_RST register (address 09h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 0 | SW_RST_KEY | Software reset register. This register is read back to “0x00” right after writing the value.<br>**0000 0000 —** No action (default)<br>**0000 0101 —** Reset O-type registers to default value<br>**0000 1001 —** Reset O-type registers and S-type registers<br>**0000 1110 —** Cold reset (Power recycle all regulators)<br>**0010 0011 —** Warm Reset (Toggle POR_B for 20 ms)<br>**1110 1110 —** PMIC digital reset (Debug purpose only)<br>**others —** Forbidden |

## 8.2.11 PWR_SEQ_CTRL

Debounce timer configuration register

**Table 39. PWR_SEQ_CTRL register (address 0Ah) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | PMIC_RST_B_ON | ACOK_B_ON | PMIC_RST_B_DEB | ACOK_B_OSTMR | PSQ_TON_STEP | | PSQ_ TOFF_STEP | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 40. PWR_SEQ_CTRL register (address 0Ah) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | PMIC_RST_B_ON | Configure PMIC_RST_B pin as Power ON source<br>**0 —** Mask (default)<br>**1 —** Power ON Source |
| 6 | ACOK_B_ON | Configure ACOK_B pin as Power ON source<br>**0 —** Mask (default)<br>**1 —** Power ON Source |
| 5 | PMIC_RST_B_ DEB | Debounce time for PMIC_RST_B pin for falling edge. ( rising edge doesn’t have debounce time)<br>**0 —** 20 ms (default)<br>**1 —** 100 ms |
| 4 | ACOK_B_OSTMR | Oneshot timer for ACOK_B, Oneshot timer works only at SNVS state<br>**0 —** 2.5 sec (default)<br>**1 —** 5 sec |
| 3 to 2 | PSQ_TON_STEP | Time step configuration during power on sequence<br>**00 —** 1 ms<br>**01 —** 2 ms (default)<br>**10 —** 4 ms<br>**11 —** 8 ms |
| 1 to 0 | PSQ_TOFF_STEP | Time step configuration during power down sequence<br>**00 —** 2 ms<br>**01 —** 4 ms<br>**10 —** 8 ms (default)<br>**11 —** 16 ms |

## 8.2.12 SYS_CFG1

VSYS_UVLO and LOW VSYS configuration register

**Table 41. SYS_CFG1 register (address 0Bh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | LOW_VSYS | | STANDBY_CFG | RESETKEY_TIMER | | | TFLT_SD_WAIT | THERM_SD_DIS |
| Reset | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 42. SYS_CFG1 register (address 0Bh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | LOW_VSYS | Low VSYS threshold above $V_{SYS\_UVLO}$<br>**00 —** 100 mV<br>**01 —** 200 mV (default)<br>**10 —** 300 mV<br>**11 —** 400 mV |
| 5 | STANDBY_CFG | Mode configuration bit when PMIC_STBY_REQ pin is High<br>**0 —** STANDBY mode (default)<br>**1 —** DPSTANDBY mode |
| 4 to 2 | RESETKEY_TIMER | RESETKEY timer configuration after PMIC_RST_B pin falls low<br>**000 —** 100 ms<br>**001 —** 1 sec<br>**010 —** 2 sec<br>**011 —** 4 sec<br>**100 —** 6 sec<br>**101 —** 8 sec (default)<br>**110 —** 10 sec<br>**111 —** 12 sec |
| 1 | TFLT_SD_WAIT | Wait time for AP action when regulator fault occurs<br>**0 —** 100 ms (default)<br>**1 —** 20 µs |
| 0 | THERM_SD_DIS | Thermal shutdown disable bit<br>**0 —** Enable Thermal shutdown (default)<br>**1 —** Disable Thermal shutdown |

### 8.2.13 SYS_CFG2

ONKEY timer, power save mode and VSYS UVLO configuration register

**Table 43. SYS_CFG2 register (address 0Ch) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | ONKEY_TIMER | | PWR_SAVE | | RSVD | POK_PU | VSYS_UVLO | |
| Reset | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 44. SYS_CFG2 register (address 0Ch) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | ONKEY_TIMER | ONKEY timer configuration after PMIC_RST_B pin falls low<br>**00 —** 1 sec<br>**01 —** 2 sec (default) |

**Table 44. SYS_CFG2 register (address 0Ch) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **10 —** 4 sec<br>**11 —** 8 sec |
| 5 to 4 | PWR_SAVE | Power save mode (Disabling High accuracy BG and Thermal shutdown)<br>**00 —** Use Low Iq BG and enable Thermal shutdown<br>**01 —** Power save mode at STANDBY/DPSTANDBY mode<br>**10 —** Power save mode at DPSTANDBY mode<br>**11 —** Normal Power mode (default) |
| 3 | RSVD | Reserved |
| 2 | POK_PU | POK reference during power up<br>**0 —** POK is reference to turn on next power group (default)<br>**1 —** POK is ignored during power up |
| 1 to 0 | VSYS_UVLO | VSYS UVLO threshold, rising threshold<br>**00 —** 2.65 V<br>**01 —** 2.85 V (default)<br>**10 —** 3.0 V<br>**11 —** 3.3V |

## 8.2.14 MODEPIN_CFG

MODE0, MODE1, MODE2 pin control configuration

**Table 45. MODEPIN_CFG register (address 0Dh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | MODE0_CFG | | MODE1_CFG | | | MODE2_CFG | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 46. MODEPIN_CFG register (address 0Dh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | MODE0_CFG | MODE0 pin configuration<br>**00 —** DVS control (default)<br>**01 —** LDO2 voltage selection<br>**10 —** LSW1 ON/OFF control<br>**11 —** LSW4 ON/OFF control |
| 5 to 3 | MODE1_CFG | MODE1 pin configuration<br>**000 —** DVS control (default)<br>**001 —** LDO2 voltage selection<br>**010 —** LSW1 ON/OFF control<br>**011 —** LSW2 ON/OFF control<br>**100 —** LSW3 ON/OFF control<br>**101 and 111 —** LSW4 ON/OFF control |
| 2 to 0 | MODE2_CFG | MODE2 pin configuration<br>**000 —** DVS control (default)<br>**001 —** LDO2 voltage selection<br>**010 —** LSW1 ON/OFF control<br>**011 —** LSW2 ON/OFF control<br>**100 —** LSW3 ON/OFF control<br>**101 and 111 —** LSW4 ON/OFF control |

### 8.2.15 BUCK1CTRL

BUCK1 control register for Active discharge, FPWM and Enable.

**Table 47. BUCK1CTRL register (address 10h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | B1_LPMODE | | B1_AD | B1_FPWM | B1_ENMODE | |
| **Reset** | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 48. BUCK1CTRL register (address 10h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | RSVD | Reserved |
| 5 to 4 | B1_LPMODE | BUCK1 Low power mode<br>**00 —** Automatic transition mode<br>**01 —** Low power mode at STANDBY mode and DPSTANDBY mode<br>**10 —** Low power mode at DPSTANDBY mode<br>**11 —** Normal mode (default) |
| 3 | B1_AD | Buck1 Active discharge<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF(default) |
| 2 | B1_FPWM | Forced PWM mode<br>**0 —** Automatic PFM and PWM mode transition (default)<br>**1 —** Forced PWM mode |
| 1 to 0 | B1_ENMODE | Buck1 enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

### 8.2.16 BUCK1OUT

BUCK1 output voltage configuration register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 49. BUCK1OUT register (address 11h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B1_OUT | | | | | | |
| **Reset** | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 50. BUCK1OUT register (address 11h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B1_OUT | BUCK1 Output voltage<br>Programmable from 0.60 V to 3.40 V in 25 mV steps<br>**011 0000 —** 1.8 V (default) |

**Table 50. BUCK1OUT register (address 11h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | See Table 108 |

## 8.2.17 BUCK23_DVS_CFG1

BUCK2, BUCK3 DVS control configuration register

**Table 51. BUCK23_DVS_CFG1 register (address 12h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | B2_DVS_UP | B2_DVS_DN | B3_DVS_UP | B3_DVS_DN | MODE_ PULSE | SMART_ MODE | MODE2_EN | BUCK_SEL |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 52. BUCK23_DVS_CFG1 register (address 12h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | B2_DVS_UP | BUCK2 increment step from MODE[1:0] pins pulse<br>**0 —** 12.5 mV (default)<br>**1 —** 25 mV |
| 6 | B2_DVS_DN | BUCK2 decrement step from MODE[1:0] pins pulse<br>**0 —** 12.5 mV (default)<br>**1 —** 25 mV |
| 5 | B3_DVS_UP | BUCK3 increment step from MODE[1:0] pins pulse<br>**0 —** 12.5 mV (default)<br>**1 —** 25 mV |
| 4 | B3_DVS_DN | BUCK3 decrement step from MODE[1:0] pins pulse<br>**0 —** 12.5 mV (default)<br>**1 —** 25 mV |
| 3 | MODE_PULSE | Mode pin pulse width configuration<br>**0 —** 0 µs (default)<br>**1 —** 2 µs |
| 2 | SMART_MODE | DVS smart mode configuration<br>**0 —** Smart mode disabled. BUCK2/3 output voltage is determined by BUCKx_OUT_DVSx from MODE[2:0] pin logic combination (default)<br>**1 —** Smart mode enabled |
| 1 | MODE2_EN | MODE2 pin enable bit ( Only when SMART_MODE bit = 1b )<br>**0 —** Mode2 pin is ignored (default)<br>**1 —** Mode2 pin is used to select BUCK2 or BUCK3 for DVS control |
| 0 | BUCK_SEL | BUCK selection in Smart DVS mode when MODE2_EN bit = 0b.<br>**0 —** BUCK2 (default)<br>**1 —** BUCK3 |

## 8.2.18 BUCK23_DVS_CFG2

BUCK2, BUCK3 DVS control configuration register

**Table 53. BUCK23_DVS_CFG2 register (address 13h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | B2_DVS_CTRL | | B3_DVS_CTRL | | RSVD | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 54. BUCK23_DVS_CFG2 register (address 13h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | B2_DVS_CTRL | BUCK2 DVS Control<br>**00 —** DVS control BUCK2OUT_DVS0 Reg through I2C (default)<br>**01 —** DVS control through PMIC_STBY_REQ pin<br>**10 —** DVS control through MODE[2:0] pins in Active mode and the voltage set to BUCK2OUT_STBY when PMIC_STBY_REQ = H<br>**11 —** DVS control through MODE[2:0] pins in RUN state |
| 5 to 4 | B3_DVS_CTRL | BUCK3 DVS Control<br>**00 —** DVS control BUCK3OUT_DVS0 Reg through I2C (default)<br>**01 —** DVS control through PMIC_STBY_REQ pin<br>**10 —** DVS control through MODE[2:0] pins in Active mode and the voltage set to BUCK3OUT_STBY when PMIC_STBY_REQ = H<br>**11 —** DVS control through MODE[2:0] pins in RUN state |
| 3 to 0 | RSVD | Reserved |

## 8.2.19 BUCK2CTRL

BUCK2 control register for Ramp, DVS control, Active discharge, FPWM and Enable.

**Table 55. BUCK2CTRL register (address 14h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | B2_RAMP | | B2_LPMODE | | B2_AD | B2_FPWM | B2_ENMODE | |
| Reset | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 56. BUCK2CTRL register (address 14h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | B2_RAMP | BUCK2 DVS speed<br>**00 —** 25 mV / 1 µs<br>**01 —** 25 mV / 2 µs (default)<br>**10 —** 25 mV / 4 µs<br>**11 —** 25 mV / 8 µs |
| 5 to 4 | B2_LPMODE | BUCK2 power mode<br>**00 —** Automatic transition mode<br>**01 —** Low power mode at STANDBY mode and DPSTANDBY mode<br>**10 —** Low power mode at DPSTANDBY mode<br>**11 —** Normal mode (default) |
| 3 | B2_AD | BUCK2 Active discharge<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 2 | B2_FPWM | Forced PWM mode |

**Table 56. BUCK2CTRL register (address 14h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **0 —** Automatic PFM and PWM mode transition (default)<br>**1 —** Forced PWM mode |
| 1 to 0 | B2_ENMODE | BUCK2 enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

### 8.2.20 BUCK2OUT_DVS0

BUCK2 DVS output voltage when MODE[2:0] = 000 && PMIC_STBY_REQ = L

**Table 57. BUCK2OUT_DVS0 register (address 15h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS0 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 58. BUCK2OUT_DVS0 register (address 15h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS0 | BUCK2 DVS0 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

### 8.2.21 BUCK2OUT_DVS1

BUCK2 DVS output voltage when MODE[2:0] = 001 && PMIC_STBY_REQ = L

**Table 59. BUCK2OUT_DVS1 register (address 16h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS1 | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 60. BUCK2OUT_DVS1 register (address 16h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS1 | BUCK2 DVS1 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

### 8.2.22 BUCK2OUT_DVS2

BUCK2 DVS output voltage when MODE[2:0] = 010 && PMIC_STBY_REQ = L

**Table 61. BUCK2OUT_DVS2 register (address 17h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS2 | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 62. BUCK2OUT_DVS2 register (address 17h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS2 | BUCK1 DVS2 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

### 8.2.23 BUCK2OUT_DVS3

BUCK2 DVS output voltage when MODE[2:0] = 011 && PMIC_STBY_REQ = L

**Table 63. BUCK2OUT_DVS3 register (address 18h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS3 | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 64. BUCK2OUT_DVS3 register (address 18h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS3 | BUCK2 DVS3 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

### 8.2.24 BUCK2OUT_DVS4

BUCK2 DVS output voltage when MODE[2:0] = 100 && PMIC_STBY_REQ = L

**Table 65. BUCK2OUT_DVS4 register (address 19h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS4 | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 66. BUCK2OUT_DVS4 register (address 19h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS4 | BUCK2 DVS4 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

## 8.2.25 BUCK2OUT_DVS5

BUCK2 DVS output voltage when MODE[2:0] = 101 && PMIC_STBY_REQ = L

**Table 67. BUCK2OUT_DVS5 register (address 1Ah) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS5 | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 68. BUCK2OUT_DVS5 register (address 1Ah) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS5 | BUCK2 DVS5 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

## 8.2.26 BUCK2OUT_DVS6

BUCK2 DVS output voltage when MODE[2:0] = 110 && PMIC_STBY_REQ = L

**Table 69. BUCK2OUT_DVS6 register (address 1Bh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS6 | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 70. BUCK2OUT_DVS6 register (address 1Bh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS6 | BUCK2 DVS6 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

## 8.2.27 BUCK2OUT_DVS7

BUCK2 DVS output voltage when MODE[2:0] = 111 && PMIC_STBY_REQ = L

**Table 71. BUCK2OUT_DVS7 register (address 1Ch) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS7 | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 72. BUCK2OUT_DVS7 register (address 1Ch) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS7 | BUCK2 DVS7 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

## 8.2.28 BUCK2OUT_STDBY

BUCK2 DVS output voltage PMIC_STBY_REQ = H

**Table 73. BUCK2OUT_STDBY register (address 1Dh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_DVS_STBY | | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 74. BUCK2OUT_STDBY register (address 1Dh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_DVS_STBY | BUCK2 Output voltage at Standby mode<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**001 1000 —** 0.9 V (default)<br>See Table 107 |

## 8.2.29 BUCK2OUT_MAX_LIMIT

BUCK2 output voltage max limit register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 75. BUCK2OUT_MAX_LIMIT register (address 1Fh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_MAX_LIMIT | | | | | | |
| **Reset** | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 76. BUCK2OUT_MAX_LIMIT register (address 1Fh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_MAX_LIMIT | BUCK2 output voltage maximum limit<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**011 1000 —** 1.3 V (default)<br>See Table 107 |

### 8.2.30 BUCK2OUT_MIN_LIMIT

BUCK2 output voltage Lower limit register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 77. BUCK2OUT_MIN_LIMIT register (address 20h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B2_MIN_LIMIT | | | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 78. BUCK2OUT_MIN_LIMIT register (address 20h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B2_MIN_LIMIT | BUCK2 output voltage minimum limit<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**000 1000 —** 0.7 V (default)<br>See Table 107 |

### 8.2.31 BUCK3CTRL

BUCK3 control register for Ramp, DVS control, Active discharge, FPWM and Enable.

**Table 79. BUCK3CTRL register (address 21h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | B3_RAMP | | B3_LPMODE | | B3_AD | B3_FPWM | B3_ENMODE | |
| **Reset** | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 80. BUCK3CTRL register (address 21h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | B3_RAMP | BUCK3 DVS speed<br>**00 —** 25 mV / 1 µs<br>**01 —** 25 mV / 2 µs (default)<br>**10 —** 25 mV / 4 µs<br>**11 —** 25 mV / 8 µs |
| 5 to 4 | B3_LPMODE | BUCK3 power mode<br>**00 —** Automatic transition mode<br>**01 —** Low power mode at STANDBY mode and DPSTANDBY mode |

**Table 80. BUCK3CTRL register (address 21h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **10 —** Low power mode at DPSTANDBY mode<br>**11 —** Normal mode (default) |
| 3 | B3_AD | BUCK3 Active discharge<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 2 | B3_FPWM | Forced PWM mode<br>**0 —** Automatic PFM and PWM mode transition (default)<br>**1 —** Forced PWM mode |
| 1 to 0 | B3_ENMODE | BUCK3 enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

## 8.2.32 BUCK3OUT_DVS0

BUCK3 DVS output voltage when MODE[2:0] = 000 && PMIC_STBY_REQ = L

**Table 81. BUCK3OUT_DVS0 register (address 22h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS0 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 82. BUCK3OUT_DVS0 register (address 22h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_DVS0 | BUCK3 DVS0 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.33 BUCK3OUT_DVS1

BUCK3 DVS output voltage when MODE[2:0] = 001 && PMIC_STBY_REQ = L

**Table 83. BUCK3OUT_DVS1 register (address 23h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS1 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 84. BUCK3OUT_DVS1 register (address 23h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |

**Table 84. BUCK3OUT_DVS1 register (address 23h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| 6 to 0 | B3_DVS1 | BUCK3 DVS1 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.34 BUCK3OUT_DVS2

BUCK3 DVS output voltage when MODE[2:0] = 010 && PMIC_STBY_REQ = L

**Table 85. BUCK3OUT_DVS2 register (address 24h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS2 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 86. BUCK3OUT_DVS2 register (address 24h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_DVS2 | BUCK1 DVS2 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.35 BUCK3OUT_DVS3

BUCK3 DVS output voltage when MODE[2:0] = 011 && PMIC_STBY_REQ = L

**Table 87. BUCK3OUT_DVS3 register (address 25h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS3 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 88. BUCK3OUT_DVS3 register (address 25h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_DVS3 | BUCK3 DVS3 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.36 BUCK3OUT_DVS4

BUCK3 DVS output voltage when MODE[2:0] = 100 && PMIC_STBY_REQ = L

**Table 89. BUCK3OUT_DVS4 register (address 26h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS4 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 90. BUCK3OUT_DVS4 register (address 26h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_DVS4 | BUCK3 DVS4 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.37 BUCK3OUT_DVS5

BUCK3 DVS output voltage when MODE[2:0] = 101 && PMIC_STBY_REQ = L

**Table 91. BUCK3OUT_DVS5 register (address 27h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS5 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 92. BUCK3OUT_DVS5 register (address 27h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_DVS5 | BUCK3 DVS5 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.38 BUCK3OUT_DVS6

BUCK3 DVS output voltage when MODE[2:0] = 110 && PMIC_STBY_REQ = L

**Table 93. BUCK3OUT_DVS6 register (address 28h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS6 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 94. BUCK3OUT_DVS6 register (address 28h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |

**Table 94. BUCK3OUT_DVS6 register (address 28h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| 6 to 0 | B3_DVS6 | BUCK3 DVS6 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.39 BUCK3OUT_DVS7

BUCK3 DVS output voltage when MODE[2:0] = 111 && PMIC_STBY_REQ = L

**Table 95. BUCK3OUT_DVS7 register (address 29h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS7 | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 96. BUCK3OUT_DVS7 register (address 29h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_DVS7 | BUCK3 DVS7 Output voltage<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.40 BUCK3OUT_STDBY

BUCK3 DVS output voltage PMIC_STBY_REQ = H

**Table 97. BUCK3OUT_STDBY register (address 2Ah) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_DVS_STBY | | | | | | |
| **Reset** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 98. BUCK3OUT_STDBY register (address 2Ah) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_DVS_STBY | BUCK3 Output voltage at Standby mode<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**010 0000 —** 1.0 V (default)<br>See Table 107 |

## 8.2.41 BUCK3OUT_MAX_LIMIT

BUCK3 output voltage max limit register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 99. BUCK3OUT_MAX_LIMIT register (address 2Ch) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_MAX_LIMIT | | | | | | |
| **Reset** | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 100. BUCK3OUT_MAX_LIMIT register (address 2Ch) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_MAX_LIMIT | BUCK3 output voltage max limit<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**011 1000 —** 1.3 V (default)<br>See Table 107 |

## 8.2.42 BUCK3OUT_MIN_LIMIT

BUCK3 output voltage lower limit register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 101. BUCK3OUT_MIN_LIMIT register (address 2Dh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B3_MIN_LIMIT | | | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 102. BUCK3OUT_MIN_LIMIT register (address 2Dh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B3_MIN_LIMIT | BUCK3 output voltage minimum limit<br>Programmable from 0.60 V to 2.1875 V in 12.5 mV steps<br>**000 1000 —** 0.7 V (default)<br>See Table 107 |

## 8.2.43 BUCK4CTRL

BUCK4 control register for Active discharge, FPWM and Enable.

**Table 103. BUCK4CTRL register (address 2Eh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | B4_LPMODE | | B4_AD | B4_FPWM | B4_ENMODE | |
| **Reset** | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 104. BUCK4CTRL register (address 2Eh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | RSVD | Reserved |
| 5 to 4 | B4_LPMODE | BUCK4 power mode<br>**00 —** Automatic transition mode<br>**01 —** Low power mode at STANDBY mode and DPSTANDBY mode<br>**10 —** Low power mode at DPSTANDBY mode<br>**11 —** Normal mode (default) |
| 3 | B4_AD | Buck4 Active discharge<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 2 | B4_FPWM | Forced PWM mode<br>**0 —** Automatic PFM and PWM mode transition (default)<br>**1 —** Forced PWM mode |
| 1 to 0 | B4_ENMODE | Buck4 enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

## 8.2.44 BUCK4OUT

BUCK4 output voltage configuration register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 105. BUCK4OUT register (address 2Fh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | B4_OUT | | | | | | |
| **Reset**[1] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

[1] The reset value depends on the specific otp version as shown in Table 106.

**Table 106. BUCK4OUT register (address 2Fh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | RSVD | Reserved |
| 6 to 0 | B4_OUT | BUCK4 Output voltage<br>Programmable from 0.60 V to 3.4 V in 25 mV steps<br>***Note:*** *PCA9460A and PCA9450B: 001 0100b (1.1 V), PCA9460C: 001 1000b (1.2 V)*<br>See Table 108 |

**Table 107. BUCK2, BUCK3 Output voltage table**

| Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
|---|---|---|---|---|---|---|---|
| 0x00 | 0.6000 V | 0x20 | 1.0000 V | 0x40 | 1.4000 V | 0x60 | 1.8000 V |
| 0x01 | 0.6125 V | 0x21 | 1.0125 V | 0x41 | 1.4125 V | 0x61 | 1.8125 V |
| 0x02 | 0.6250 V | 0x22 | 1.0250 V | 0x42 | 1.4250 V | 0x62 | 1.8250 V |
| 0x03 | 0.6375 V | 0x23 | 1.0375 V | 0x43 | 1.4375 V | 0x63 | 1.8375 V |

**Table 107. BUCK2, BUCK3 Output voltage table***...continued*

| Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
|---|---|---|---|---|---|---|---|
| 0x04 | 0.6500 V | 0x24 | 1.0500 V | 0x44 | 1.4500 V | 0x64 | 1.8500 V |
| 0x05 | 0.6625 V | 0x25 | 1.0625 V | 0x45 | 1.4625 V | 0x65 | 1.8625 V |
| 0x06 | 0.6750 V | 0x26 | 1.0750 V | 0x46 | 1.4750 V | 0x66 | 1.8750 V |
| 0x07 | 0.6875 V | 0x27 | 1.0875 V | 0x47 | 1.4875 V | 0x67 | 1.8875 V |
| 0x08 | 0.7000 V | 0x28 | 1.1000 V | 0x48 | 1.5000 V | 0x68 | 1.9000 V |
| 0x09 | 0.7125 V | 0x29 | 1.1125 V | 0x49 | 1.5125 V | 0x69 | 1.9125 V |
| 0x0A | 0.7250 V | 0x2A | 1.1250 V | 0x4A | 1.5250 V | 0x6A | 1.9250 V |
| 0x0B | 0.7375 V | 0x2B | 1.1375 V | 0x4B | 1.5375 V | 0x6B | 1.9375 V |
| 0x0C | 0.7500 V | 0x2C | 1.1500 V | 0x4C | 1.5500 V | 0x6C | 1.9500 V |
| 0x0D | 0.7625 V | 0x2D | 1.1625 V | 0x4D | 1.5625 V | 0x6D | 1.9625 V |
| 0x0E | 0.7750 V | 0x2E | 1.1750 V | 0x4E | 1.5750 V | 0x6E | 1.9750 V |
| 0x0F | 0.7875 V | 0x2F | 1.1875 V | 0x4F | 1.5875 V | 0x6F | 1.9875 V |
| 0x10 | 0.8000 V | 0x30 | 1.2000 V | 0x50 | 1.6000 V | 0x70 | 2.0000 V |
| 0x11 | 0.8125 V | 0x31 | 1.2125 V | 0x51 | 1.6125 V | 0x71 | 2.0125 V |
| 0x12 | 0.8250 V | 0x32 | 1.2250 V | 0x52 | 1.6250 V | 0x72 | 2.0250 V |
| 0x13 | 0.8375 V | 0x33 | 1.2375 V | 0x53 | 1.6375 V | 0x73 | 2.0375 V |
| 0x14 | 0.8500 V | 0x34 | 1.2500 V | 0x54 | 1.6500 V | 0x74 | 2.0500 V |
| 0x15 | 0.8625 V | 0x35 | 1.2625 V | 0x55 | 1.6625 V | 0x75 | 2.0625 V |
| 0x16 | 0.8750 V | 0x36 | 1.2750 V | 0x56 | 1.6750 V | 0x76 | 2.0750 V |
| 0x17 | 0.8875 V | 0x37 | 1.2875 V | 0x57 | 1.6875 V | 0x77 | 2.0875 V |
| 0x18 | 0.9000 V | 0x38 | 1.3000 V | 0x58 | 1.7000 V | 0x78 | 2.1000 V |
| 0x19 | 0.9125 V | 0x39 | 1.3125 V | 0x59 | 1.7125 V | 0x79 | 2.1125 V |
| 0x1A | 0.9250 V | 0x3A | 1.3250 V | 0x5A | 1.7250 V | 0x7A | 2.1250 V |
| 0x1B | 0.9375 V | 0x3B | 1.3375 V | 0x5B | 1.7375 V | 0x7B | 2.1375 V |
| 0x1C | 0.9500 V | 0x3C | 1.3500 V | 0x5C | 1.7500 V | 0x7C | 2.1500 V |
| 0x1D | 0.9625 V | 0x3D | 1.3625 V | 0x5D | 1.7625 V | 0x7D | 2.1625 V |
| 0x1E | 0.9750 V | 0x3E | 1.3750 V | 0x5E | 1.7750 V | 0x7E | 2.1750 V |
| 0x1F | 0.9875 V | 0x3F | 1.3875 V | 0x5F | 1.7875 V | 0x7F | 2.1875 V |

**Table 108. BUCK1, BUCK4 Output voltage table**

| Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
|---|---|---|---|---|---|---|---|
| 0x00 | 0.600 V | 0x20 | 1.400 V | 0x40 | 2.200 V | 0x60 | 3.000 V |
| 0x01 | 0.625 V | 0x21 | 1.425 V | 0x41 | 2.225 V | 0x61 | 3.025 V |
| 0x02 | 0.650 V | 0x22 | 1.450 V | 0x42 | 2.250 V | 0x62 | 3.050 V |
| 0x03 | 0.675 V | 0x23 | 1.475 V | 0x43 | 2.275 V | 0x63 | 3.075 V |
| 0x04 | 0.700 V | 0x24 | 1.500 V | 0x44 | 2.300 V | 0x64 | 3.100 V |

**Table 108. BUCK1, BUCK4 Output voltage table***...continued*

| Code | Voltage | Code | Voltage | Code | Voltage | Code | Voltage |
|---|---|---|---|---|---|---|---|
| 0x05 | 0.725 V | 0x25 | 1.525 V | 0x45 | 2.325 V | 0x65 | 3.125 V |
| 0x06 | 0.750 V | 0x26 | 1.550 V | 0x46 | 2.350 V | 0x66 | 3.150 V |
| 0x07 | 0.775 V | 0x27 | 1.575 V | 0x47 | 2.375 V | 0x67 | 3.175 V |
| 0x08 | 0.800 V | 0x28 | 1.600 V | 0x48 | 2.400 V | 0x68 | 3.200 V |
| 0x09 | 0.825 V | 0x29 | 1.625 V | 0x49 | 2.425 V | 0x69 | 3.225 V |
| 0x0A | 0.850 V | 0x2A | 1.650 V | 0x4A | 2.450 V | 0x6A | 3.250 V |
| 0x0B | 0.875 V | 0x2B | 1.675 V | 0x4B | 2.475 V | 0x6B | 3.275 V |
| 0x0C | 0.900 V | 0x2C | 1.700 V | 0x4C | 2.500 V | 0x6C | 3.300 V |
| 0x0D | 0.925 V | 0x2D | 1.725 V | 0x4D | 2.525 V | 0x6D | 3.325 V |
| 0x0E | 0.950 V | 0x2E | 1.750 V | 0x4E | 2.550 V | 0x6E | 3.350 V |
| 0x0F | 0.975 V | 0x2F | 1.775 V | 0x4F | 2.575 V | 0x6F | 3.375 V |
| 0x10 | 1.000 V | 0x30 | 1.800 V | 0x50 | 2.600 V | 0x70 | 3.400 V |
| 0x11 | 1.025 V | 0x31 | 1.825 V | 0x51 | 2.625 V | 0x71 | 3.400 V |
| 0x12 | 1.050 V | 0x32 | 1.850 V | 0x52 | 2.650 V | 0x72 | 3.400 V |
| 0x13 | 1.075 V | 0x33 | 1.875 V | 0x53 | 2.675 V | 0x73 | 3.400 V |
| 0x14 | 1.100 V | 0x34 | 1.900 V | 0x54 | 2.700 V | 0x74 | 3.400 V |
| 0x15 | 1.125 V | 0x35 | 1.925 V | 0x55 | 2.725 V | 0x75 | 3.400 V |
| 0x16 | 1.150 V | 0x36 | 1.950 V | 0x56 | 2.750 V | 0x76 | 3.400 V |
| 0x17 | 1.175 V | 0x37 | 1.975 V | 0x57 | 2.775 V | 0x77 | 3.400 V |
| 0x18 | 1.200 V | 0x38 | 2.000 V | 0x58 | 2.800 V | 0x78 | 3.400 V |
| 0x19 | 1.225 V | 0x39 | 2.025 V | 0x59 | 2.825 V | 0x79 | 3.400 V |
| 0x1A | 1.250 V | 0x3A | 2.050 V | 0x5A | 2.850 V | 0x7A | 3.400 V |
| 0x1B | 1.275 V | 0x3B | 2.075 V | 0x5B | 2.875 V | 0x7B | 3.400 V |
| 0x1C | 1.300 V | 0x3C | 2.100 V | 0x5C | 2.900 V | 0x7C | 3.400 V |
| 0x1D | 1.325 V | 0x3D | 2.125 V | 0x5D | 2.925 V | 0x7D | 3.400 V |
| 0x1E | 1.350 V | 0x3E | 2.150 V | 0x5E | 2.950 V | 0x7E | 3.400 V |
| 0x1F | 1.375 V | 0x3F | 2.175 V | 0x5F | 2.975 V | 0x7F | 3.400 V |

### 8.2.45 LDO1_CFG

LDO1 enable control and active discharge resistor configuration register

**Table 109. LDO1_CFG register (address 30h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | L1_CSEL | | L1_LLSEL | | L1_LPMODE | | L1_ENMODE | |
| **Reset** | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 110. LDO1_CFG register (address 30h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | L1_CSEL | Total Output capacitor selection<br>**00 —** Setting for Cout < 5 µF<br>**01 —** Setting for Cout < 5 µF<br>**10 and 11 —** Auto Cout detection (default) |
| 5 to 4 | L1_LLSEL | Output trace resistance compensation<br>**00 —** No Compensation<br>**01 —** 15 mΩ (default)<br>**10 —** 30 mΩ<br>**11 —** 45 mΩ |
| 3 to 2 | L1_LPMODE | LDO1 power mode<br>**00 —** Low power mode at RUN state<br>**01 —** Low power mode at STANDBY mode and DPSTANDBY mode<br>**10 —** Low power mode at DPSTANDBY mode<br>**11 —** Normal mode (default) |
| 1 to 0 | L1_ENMODE | LDO1 Enable mode<br>**00 —**OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

## 8.2.46 LDO1_OUT

LDO1 output voltage register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 111. LDO1_OUT register (address 31h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | L1_AD | L1_INL1_MDET | L1_INL1_VSEL | L1_OUT | | | | |
| **Reset** | 1 | 0 | 0 | | | | | |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 112. LDO1_OUT register (address 31h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | L1_AD | LDO1 Active discharge enable<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 6 | L1_INL1_MDET | Manual detection for INL1 supply<br>**0 —** Auto detection (default)<br>**1 —** Manual configuration |
| 5 | L1_INL1_VSEL | INL1 voltage selection, effective only when L1_INL1_MDET = 1b<br>**0 —** (VSYS – VINL1) ≤ 0.7 (default)<br>**1 —** (VSYS – VINL1) > 0.7 |
| 4 to 0 | L1_OUT | LDO1 output voltage<br>Programmable from 0.6 V to 1.95 V in 50 mV steps<br>See Table 113[1] |

[1]
- PCA9460A: 0 1010 (1.1 V)
- PCA9460B: 0 0000 (0.6 V)
- PCA9460C: 0 1100 (1.2 V)

**Table 113. L1_OUT values**

| | | | |
|---|---|---|---|
| **0x00 : 0.60 V** | 0x8 : 1.00 V | 0x10 : 1.40 V | 0x18 : 1.80 V |
| 0x01 : 0.65 V | 0x9 : 1.05 V | 0x11 : 1.45 V | 0x19 : 1.85 V |
| 0x02 : 0.70 V | **0xA : 1.10 V** | 0x12 : 1.50 V | 0x1A : 1.90 V |
| 0x03 : 0.75 V | 0xB : 1.15 V | 0x13 : 1.55 V | 0x1B : 1.95 V |
| 0x04 : 0.80 V | **0xC : 1.20 V** | 0x14 : 1.60 V | 0x1C : 1.95 V |
| 0x05 : 0.85 V | 0xD : 1.25 V | 0x15 : 1.65 V | 0x1D : 1.95 V |
| 0x06 : 0.90 V | 0xE : 1.30 V | 0x16 : 1.70 V | 0x1E : 1.95 V |
| 0x07 : 0.95 V | 0xF : 1.35 V | 0x17 : 1.75 V | 0x1F : 1.95 V |

### 8.2.47 LDO2_CFG

LDO2 enable control and active discharge resistor configuration register

**Table 114. LDO2_CFG register (address 32h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | | L2_AD | RSVD | | L2_ENMODE | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 115. LDO2_CFG register (address 32h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 5 | L4_FLT_M | Reserved |
| 4 | L1_FLT_M | LDO2 Active discharge enable<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 3 to 2 | B4_FLT_M | Reserved |
| 1 to 0 | B2_FLT_M | LDO2 Enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

### 8.2.48 LDO2_OUT_L

LDO2 output voltage register when LDO2_VSEL is low. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 116. LDO2_OUT_L register (address 33h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | L2_OUT_L | | | | | |
| **Reset** | 0 | 0 | Reset value is 11 0010 (3.3 V)<br>Table 118 | | | | | |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 117. LDO2_OUT_L register (address 33h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | RSVD | Total Output capacitor selection<br>**00 —** Setting for Cout < 5 µF<br>**01 —** Setting for Cout < 5 µF<br>**10 and 11 —** Auto Cout detection (default) |
| 5 to 0 | L2_OUT_L | LDO2 output voltage when LDO2_VSEL = Low<br>Programmable from 0.8 V to 3.3 V in 50 mV steps<br>**11 0010 —** 3.3 V (default)<br>See Table 118 |

**Table 118. L2_OUT_L values**

| | | | |
|---|---|---|---|
| 0x00 : 0.80 V | 0x10 : 1.60 V | 0x20 : 2.40 V | 0x30 : 3.20 V |
| 0x01 : 0.85 V | 0x11 : 1.65 V | 0x21 : 2.45 V | 0x31 : 3.25 V |
| 0x02 : 0.90 V | 0x12 : 1.70 V | 0x22 : 2.50 V | **0x32 : 3.30 V** |
| 0x03 : 0.95 V | 0x13 : 1.75 V | 0x23 : 2.55 V | 0x33 : 3.30 V |
| 0x04 : 1.00 V | 0x14 : 1.80 V | 0x24 : 2.60 V | 0x34 : 3.30 V |
| 0x05 : 1.05 V | 0x15 : 1.85 V | 0x25 : 2.65 V | 0x35 : 3.30 V |
| 0x06 : 1.10 V | 0x16 : 1.90 V | 0x26 : 2.70 V | 0x36 : 3.30 V |
| 0x07 : 1.15 V | 0x17 : 1.95 V | 0x27 : 2.75 V | 0x37 : 3.30 V |
| 0x08 : 1.20 V | 0x18 : 2.00 V | 0x28 : 2.80 V | 0x38 : 3.30 V |
| 0x09 : 1.25 V | 0x19 : 2.05 V | 0x29 : 2.85 V | 0x39 : 3.30 V |
| 0x0A : 1.30 V | 0x1A : 2.10 V | 0x2A : 2.90 V | 0x3A : 3.30 V |
| 0x0B : 1.35 V | 0x1B : 2.15 V | 0x2B : 2.95 V | 0x3B : 3.30 V |
| 0x0C : 1.40 V | 0x1C : 2.20 V | 0x2C : 3.00 V | 0x3C : 3.30 V |
| 0x0D : 1.45 V | 0x1D : 2.25 V | 0x2D : 3.05 V | 0x3D : 3.30 V |
| 0x0E : 1.50 V | 0x1E : 2.30 V | 0x2E : 3.10 V | 0x3E : 3.30 V |
| 0x0F : 1.55 V | 0x1F : 2.35 V | 0x2F : 3.15 V | 0x3F : 3.30 V |

### 8.2.49 LDO2_OUT_H

LDO2 output voltage register when LDO2_VSEL is High. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 119. LDO2_OUT_H register (address 34h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | L2_OUT_H | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 120. LDO2_OUT_H register (address 34h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | RSVD | Reserved |
| 5 to 0 | L2_OUT_H | LDO2 output voltage when LDO2_VSEL = High<br>Programmable from 0.8 V to 3.3 V in 50 mV steps<br>**01 0100 —** 1.8 V (default)<br>See Table 118 |

## 8.2.50 LDO3_CFG

LDO3 enable control and active discharge resistor configuration register

**Table 121. LDO3_CFG register (address 35h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | | L3_AD | RSVD | | L3_ENMODE | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 122. LDO3_CFG register (address 35h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 5 | RSVD | Reserved |
| 4 | L3_AD | LDO3 Active discharge enable<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 3 to 2 | RSVD | Reserved |
| 1 to 0 | L3_ENMODE | LDO3 Enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

## 8.2.51 LDO3_OUT

LDO3 output voltage register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 123. LDO3_OUT register (address 36h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | L3_OUT | | | | | |
| **Reset** | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 124. LDO3_OUT register (address 36h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | RSVD | Reserved |
| 5 to 0 | L3_AD | LDO3 output voltage<br>Programmable from 0.8 V to 3.3 V in 50 mV steps |

**Table 124. LDO3_OUT register (address 36h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **11 0010 —** 3.3 V (default)<br>See Table 125 |

**Table 125. L3_OUT values**

| | | | |
|---|---|---|---|
| 0x00 : 0.80 V | 0x10 : 1.60 V | 0x20 : 2.40 V | 0x30 : 3.20 V |
| 0x01 : 0.85 V | 0x11 : 1.65 V | 0x21 : 2.45 V | 0x31 : 3.25 V |
| 0x02 : 0.90 V | 0x12 : 1.70 V | 0x22 : 2.50 V | **0x32 : 3.30 V** |
| 0x03 : 0.95 V | 0x13 : 1.75 V | 0x23 : 2.55 V | 0x33 : 3.30 V |
| 0x04 : 1.00 V | 0x14 : 1.80 V | 0x24 : 2.60 V | 0x34 : 3.30 V |
| 0x05 : 1.05 V | 0x15 : 1.85 V | 0x25 : 2.65 V | 0x35 : 3.30 V |
| 0x06 : 1.10 V | 0x16 : 1.90 V | 0x26 : 2.70 V | 0x36 : 3.30 V |
| 0x07 : 1.15 V | 0x17 : 1.95 V | 0x27 : 2.75 V | 0x37 : 3.30 V |
| 0x08 : 1.20 V | 0x18 : 2.00 V | 0x28 : 2.80 V | 0x38 : 3.30 V |
| 0x09 : 1.25 V | 0x19 : 2.05 V | 0x29 : 2.85 V | 0x39 : 3.30 V |
| 0x0A : 1.30 V | 0x1A : 2.10 V | 0x2A : 2.90 V | 0x3A : 3.30 V |
| 0x0B : 1.35 V | 0x1B : 2.15 V | 0x2B : 2.95 V | 0x3B : 3.30 V |
| 0x0C : 1.40 V | 0x1C : 2.20 V | 0x2C : 3.00 V | 0x3C : 3.30 V |
| 0x0D : 1.45 V | 0x1D : 2.25 V | 0x2D : 3.05 V | 0x3D : 3.30 V |
| 0x0E : 1.50 V | 0x1E : 2.30 V | 0x2E : 3.10 V | 0x3E : 3.30 V |
| 0x0F : 1.55 V | 0x1F : 2.35 V | 0x2F : 3.15 V | 0x3F : 3.30 V |

### 8.2.52 LDO4_CFG

LDO4 enable control and active discharge resistor configuration register

**Table 126. LDO4_CFG register (address 37h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | | L4_AD | RSVD | | L4_ENMODE | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 127. LDO4_CFG register (address 37h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 5 | RSVD | Reserved |
| 4 | L4_AD | LDO4 Active discharge enable<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 3 to 2 | RSVD | Reserved |
| 1 to 0 | L4_ENMODE | LDO4 Enable mode<br>**00 —** OFF |

**Table 127. LDO4_CFG register (address 37h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

### 8.2.53 LDO4_OUT

LDO4 output voltage register. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 128. LDO4_OUT register (address 38h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | RSVD | | L4_OUT | | | | | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 129. LDO4_OUT register (address 38h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | RSVD | Reserved |
| 5 to 0 | L4_OUT | LDO4 output voltage<br>Programmable from 0.8 V to 3.3 V in 50 mV steps<br>**01 0100 —** 1.8 V (default)<br>See Table 130 |

**Table 130. L4_OUT values**

| | | | |
|---|---|---|---|
| 0x00 : 0.80 V | 0x10 : 1.60 V | 0x20 : 2.40 V | 0x30 : 3.20 V |
| 0x01 : 0.85 V | 0x11 : 1.65 V | 0x21 : 2.45 V | 0x31 : 3.25 V |
| 0x02 : 0.90 V | 0x12 : 1.70 V | 0x22 : 2.50 V | 0x32 : 3.30 V |
| 0x03 : 0.95 V | 0x13 : 1.75 V | 0x23 : 2.55 V | 0x33 : 3.30 V |
| 0x04 : 1.00 V | **0x14 : 1.80 V** | 0x24 : 2.60 V | 0x34 : 3.30 V |
| 0x05 : 1.05 V | 0x15 : 1.85 V | 0x25 : 2.65 V | 0x35 : 3.30 V |
| 0x06 : 1.10 V | 0x16 : 1.90 V | 0x26 : 2.70 V | 0x36 : 3.30 V |
| 0x07 : 1.15 V | 0x17 : 1.95 V | 0x27 : 2.75 V | 0x37 : 3.30 V |
| 0x08 : 1.20 V | 0x18 : 2.00 V | 0x28 : 2.80 V | 0x38 : 3.30 V |
| 0x09 : 1.25 V | 0x19 : 2.05 V | 0x29 : 2.85 V | 0x39 : 3.30 V |
| 0x0A : 1.30 V | 0x1A : 2.10 V | 0x2A : 2.90 V | 0x3A : 3.30 V |
| 0x0B : 1.35 V | 0x1B : 2.15 V | 0x2B : 2.95 V | 0x3B : 3.30 V |
| 0x0C : 1.40 V | 0x1C : 2.20 V | 0x2C : 3.00 V | 0x3C : 3.30 V |
| 0x0D : 1.45 V | 0x1D : 2.25 V | 0x2D : 3.05 V | 0x3D : 3.30 V |
| 0x0E : 1.50 V | 0x1E : 2.30 V | 0x2E : 3.10 V | 0x3E : 3.30 V |
| 0x0F : 1.55 V | 0x1F : 2.35 V | 0x2F : 3.15 V | 0x3F : 3.30 V |

### 8.2.54 LDOSNVS_CFG

LDO_SNVS control register for enable and voltage. This register is protected by Lock key, 0x4E register should be written with unlock key before updating this register.

**Table 131. LDOSNVS_CFG register (address 39h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LSNVS_AD | LS_ENMODE | L_SNVS_OUT | | | | | |
| **Reset** | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 132. LDOSNVS_CFG register (address 39h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | LSNVS_AD | SNVS LDO Active discharge enable<br>**0 —** Always disable Active discharge resistor<br>**1 —** Enable Active discharge resistor when regulator is OFF (default) |
| 6 | LS_ENMODE | LDO_SNVS Enable mode<br>**0 —** OFF<br>**1 —** Always ON (default) |
| 5 to 0 | L_SNVS_OUT | LDO_SNVS output voltage<br>Programmable from 0.8 V to 3.3 V in 50 mV steps<br>**10 1100 —** 3.0 V (default)<br>See Table 133 |

**Table 133. L_SNVS_OUT values**

| | | | |
|---|---|---|---|
| 0x00 : 0.80 V | 0x10 : 1.60 V | 0x20 : 2.40 V | 0x30 : 3.20 V |
| 0x01 : 0.85 V | 0x11 : 1.65 V | 0x21 : 2.45 V | 0x31 : 3.25 V |
| 0x02 : 0.90 V | 0x12 : 1.70 V | 0x22 : 2.50 V | 0x32 : 3.30 V |
| 0x03 : 0.95 V | 0x13 : 1.75 V | 0x23 : 2.55 V | 0x33 : 3.30 V |
| 0x04 : 1.00 V | 0x14 : 1.80 V | 0x24 : 2.60 V | 0x34 : 3.30 V |
| 0x05 : 1.05 V | 0x15 : 1.85 V | 0x25 : 2.65 V | 0x35 : 3.30 V |
| 0x06 : 1.10 V | 0x16 : 1.90 V | 0x26 : 2.70 V | 0x36 : 3.30 V |
| 0x07 : 1.15 V | 0x17 : 1.95 V | 0x27 : 2.75 V | 0x37 : 3.30 V |
| 0x08 : 1.20 V | 0x18 : 2.00 V | 0x28 : 2.80 V | 0x38 : 3.30 V |
| 0x09 : 1.25 V | 0x19 : 2.05 V | 0x29 : 2.85 V | 0x39 : 3.30 V |
| 0x0A : 1.30 V | 0x1A : 2.10 V | 0x2A : 2.90 V | 0x3A : 3.30 V |
| 0x0B : 1.35 V | 0x1B : 2.15 V | 0x2B : 2.95 V | 0x3B : 3.30 V |
| 0x0C : 1.40 V | 0x1C : 2.20 V | **0x2C : 3.00 V** | 0x3C : 3.30 V |
| 0x0D : 1.45 V | 0x1D : 2.25 V | 0x2D : 3.05 V | 0x3D : 3.30 V |
| 0x0E : 1.50 V | 0x1E : 2.30 V | 0x2E : 3.10 V | 0x3E : 3.30 V |
| 0x0F : 1.55 V | 0x1F : 2.35 V | 0x2F : 3.15 V | 0x3F : 3.30 V |

### 8.2.55 LSW1_CTRL

Load switch 1 configuration register

**Table 134. LSW1_CTRL register (address 40h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LSW1_CFG | RSVD | | LSW1_AD | RSVD | | LSW1_EN | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 135. LSW1_CTRL register (address 40h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | LSW1_CFG | Load SW 1 Configuration<br>**0 —** Load switch (default)<br>**1 —** LED driver |
| 6 to 5 | RSVD | Reserved |
| 4 | LSW1_AD | Load SW 1 active discharge, if it is configured to LED, active discharge resistor is always off.<br>**0 —** Disabled<br>**1 —** Enabled when Load SW1 is off (default) |
| 3 to 2 | RSVD | Reserved |
| 1 to 0 | LSW1_EN | Load SW 1 Enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

### 8.2.56 LSW2_CTRL

Load switch 2 configuration register

**Table 136. LSW2_CTRL register (address 41h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LSW2_CFG | RSVD | | LSW2_AD | RSVD | | LSW2_EN | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 137. LSW2_CTRL register (address 41h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | LSW2_CFG | Load SW 2 Configuration<br>**0 —** Load switch (default)<br>**1 —** LED driver |
| 6 to 5 | RSVD | Reserved |
| 4 | LSW2_AD | Load SW 2 active discharge, if it is configured to LED, active discharge resistor is always off.<br>**0 —** Disabled<br>**1 —** Enabled when Load SW1 is off (default) |
| 3 to 2 | RSVD | Reserved |
| 1 to 0 | LSW2_EN | Load SW 2 Enable mode |

**Table 137. LSW2_CTRL register (address 41h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

## 8.2.57 LSW3_CTRL

Load switch 3 configuration register

**Table 138. LSW3_CTRL register (address 42h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LSW3_CFG | RSVD | | LSW3_AD | RSVD | | LSW3_EN | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 139. LSW3_CTRL register (address 42h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | LSW3_CFG | Load SW 3 Configuration<br>**0 —** Load switch (default)<br>**1 —** LED driver |
| 6 to 5 | RSVD | Reserved |
| 4 | LSW3_AD | Load SW 3 active discharge, if it is configured to LED, active discharge resistor is always off.<br>**0 —** Disabled<br>**1 —** Enabled when Load SW1 is off (default) |
| 3 to 2 | RSVD | Reserved |
| 1 to 0 | LSW3_EN | Load SW 3 Enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

## 8.2.58 LSW4_CTRL

Load switch 4 configuration register

**Table 140. LSW4_CTRL register (address 43h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LSW4_CFG | RSVD | | LSW4_AD | RSVD | | LSW4_EN | |
| **Reset** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 141. LSW4_CTRL register (address 43h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 | LSW4_CFG | Load SW 4 Configuration<br>**0 —** Load switch (default) |

**Table 141. LSW4_CTRL register (address 43h) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| | | **1 —** LED driver |
| 6 to 5 | RSVD | Reserved |
| 4 | LSW4_AD | Load SW 4 active discharge, if it is configured to LED, active discharge resistor is always off.<br>**0 —** Disabled<br>**1 —** Enabled when Load SW1 is off (default) |
| 3 to 2 | RSVD | Reserved |
| 1 to 0 | LSW4_EN | Load SW 4 Enable mode<br>**00 —** OFF<br>**01 —** ON at RUN State (default)<br>**10 —** ON at ACTIVE mode or STANDBY mode, OFF at DPSTANDBY<br>**11 —** ON at ACTIVE mode, OFF at STANDBY or DPSTANDBY |

## 8.2.59 LED1_CTRL

LED1 Enable and brightness configuration

**Table 142. LED1_CTRL register (address 44h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LED1_EN | | RSVD | LED1_BRT | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 143. LED1_CTRL register (address 44h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | LED1_EN | Load SW1 LED enable mode only when LSW1_CFG is set to 01b.<br>**00 —** OFF (default)<br>**01 —** Enable with Constant current<br>**10 —** Enable with Pattern 1 BLINK mode<br>**11 —** Enable with Pattern 2 BLINK mode |
| 5 | RSVD | Reserved |
| 4 to 0 | LED1_BRT | LED1 brightness setting<br>Programmable from 0.625 mA to 20 mA in 0.625 mA steps<br>See Table 144 |

**Table 144. LED1_BRT values**

| | | | |
|---|---|---|---|
| **0x00 : 0.625 mA** | 0x08 : 5.625 mA | 0x10 : 10.625 mA | 0x18 : 15.625 mA |
| 0x01 : 1.250 mA | 0x09 : 6.250 mA | 0x11 : 11.250 mA | 0x19 : 16.250 mA |
| 0x02 : 1.875 mA | 0x0A : 6.875 mA | 0x12 : 11.875 mA | 0x1A : 16.875 mA |
| 0x03 : 2.500 mA | 0x0B : 7.500 mA | 0x13 : 12.500 mA | 0x1B : 17.500 mA |
| 0x04 : 3.125 mA | 0x0C : 8.125 mA | 0x14 : 13.125 mA | 0x1C : 18.125 mA |
| 0x05 : 3.750 mA | 0x0D : 8.750 mA | 0x15 : 13.750 mA | 0x1D : 18.750 mA |
| 0x06 : 4.375 mA | 0x0E : 9.375 mA | 0x16 : 14.375 mA | 0x1E : 19.375 mA |
| 0x07 : 5.000 mA | 0x0F : 10.000 mA | 0x17 : 15.000 mA | 0x1F : 20.000 mA |

### 8.2.60 LED2_CTRL

LED2 Enable and brightness configuration

**Table 145. LED2_CTRL register (address 45h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LED2_EN | | RSVD | LED2_BRT | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 146. LED2_CTRL register (address 45h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | LED2_EN | Load SW2 LED enable mode only when LSW2_CFG is set to 01b.<br>**00 —** OFF (default)<br>**01 —** Enable with Constant current<br>**10 —** Enable with Pattern 1 BLINK mode<br>**11 —** Enable with Pattern 2 BLINK mode |
| 5 | RSVD | Reserved |
| 4 to 0 | LED2_BRT | LED2 brightness setting<br>Programmable from 0.625 mA to 20 mA in 0.625 mA steps<br>See Table 147 |

**Table 147. LED2_BRT values**

| | | | |
|---|---|---|---|
| **0x00 : 0.625 mA** | 0x08 : 5.625 mA | 0x10 : 10.625 mA | 0x18 : 15.625 mA |
| 0x01 : 1.250 mA | 0x09 : 6.250 mA | 0x11 : 11.250 mA | 0x19 : 16.250 mA |
| 0x02 : 1.875 mA | 0x0A : 6.875 mA | 0x12 : 11.875 mA | 0x1A : 16.875 mA |
| 0x03 : 2.500 mA | 0x0B : 7.500 mA | 0x13 : 12.500 mA | 0x1B : 17.500 mA |
| 0x04 : 3.125 mA | 0x0C : 8.125 mA | 0x14 : 13.125 mA | 0x1C : 18.125 mA |
| 0x05 : 3.750 mA | 0x0D : 8.750 mA | 0x15 : 13.750 mA | 0x1D : 18.750 mA |
| 0x06 : 4.375 mA | 0x0E : 9.375 mA | 0x16 : 14.375 mA | 0x1E : 19.375 mA |
| 0x07 : 5.000 mA | 0x0F : 10.000 mA | 0x17 : 15.000 mA | 0x1F : 20.000 mA |

### 8.2.61 LED3_CTRL

LED3 Enable and brightness configuration

**Table 148. LED3_CTRL register (address 46h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LED3_EN | | RSVD | LED3_BRT | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 149. LED3_CTRL register (address 46h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | LED3_EN | Load SW3 LED enable mode only when LSW3_CFG is set to 01b.<br>**00 —** OFF (default)<br>**01 —** Enable with Constant current<br>**10 —** Enable with Pattern 1 BLINK mode<br>**11 —** Enable with Pattern 2 BLINK mode |
| 5 | RSVD | Reserved |
| 4 to 0 | LED3_BRT | LED3 brightness setting<br>Programmable from 0.625 mA to 20 mA in 0.625 mA steps<br>See Table 150 |

**Table 150. LED3_BRT values**

| | | | |
|---|---|---|---|
| **0x00 : 0.625 mA** | 0x08 : 5.625 mA | 0x10 : 10.625 mA | 0x18 : 15.625 mA |
| 0x01 : 1.250 mA | 0x09 : 6.250 mA | 0x11 : 11.250 mA | 0x19 : 16.250 mA |
| 0x02 : 1.875 mA | 0x0A : 6.875 mA | 0x12 : 11.875 mA | 0x1A : 16.875 mA |
| 0x03 : 2.500 mA | 0x0B : 7.500 mA | 0x13 : 12.500 mA | 0x1B : 17.500 mA |
| 0x04 : 3.125 mA | 0x0C : 8.125 mA | 0x14 : 13.125 mA | 0x1C : 18.125 mA |
| 0x05 : 3.750 mA | 0x0D : 8.750 mA | 0x15 : 13.750 mA | 0x1D : 18.750 mA |
| 0x06 : 4.375 mA | 0x0E : 9.375 mA | 0x16 : 14.375 mA | 0x1E : 19.375 mA |
| 0x07 : 5.000 mA | 0x0F : 10.000 mA | 0x17 : 15.000 mA | 0x1F : 20.000 mA |

### 8.2.62 LED4_CTRL

LED4 Enable and brightness configuration

**Table 151. LED4_CTRL register (address 47h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LED4_EN | | RSVD | LED4_BRT | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 152. LED4_CTRL register (address 47h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | LED4_EN | Load SW4 LED enable mode only when LSW4_CFG is set to 01b.<br>**00 —** OFF (default)<br>**01 —** Enable with Constant current<br>**10 —** Enable with Pattern 1 BLINK mode<br>**11 —** Enable with Pattern 2 BLINK mode |
| 5 | RSVD | Reserved |
| 4 to 0 | LED4_BRT | LED4 brightness setting<br>Programmable from 0.625 mA to 20 mA in 0.625 mA steps<br>See Table 153 |

**Table 153. LED4_BRT values**

| | | | |
|---|---|---|---|
| **0x00 : 0.625 mA** | 0x08 : 5.625 mA | 0x10 : 10.625 mA | 0x18 : 15.625 mA |
| 0x01 : 1.250 mA | 0x09 : 6.250 mA | 0x11 : 11.250 mA | 0x19 : 16.250 mA |
| 0x02 : 1.875 mA | 0x0A : 6.875 mA | 0x12 : 11.875 mA | 0x1A : 16.875 mA |
| 0x03 : 2.500 mA | 0x0B : 7.500 mA | 0x13 : 12.500 mA | 0x1B : 17.500 mA |
| 0x04 : 3.125 mA | 0x0C : 8.125 mA | 0x14 : 13.125 mA | 0x1C : 18.125 mA |
| 0x05 : 3.750 mA | 0x0D : 8.750 mA | 0x15 : 13.750 mA | 0x1D : 18.750 mA |
| 0x06 : 4.375 mA | 0x0E : 9.375 mA | 0x16 : 14.375 mA | 0x1E : 19.375 mA |
| 0x07 : 5.000 mA | 0x0F : 10.000 mA | 0x17 : 15.000 mA | 0x1F : 20.000 mA |

### 8.2.63 LED_P1_RAMP

Pattern 1 LED ramp up down configuration

**Table 154. LED_P1_RAMP register (address 48h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | P1_UP_STEP | | P1_UP_DLY | | P1_DN_STEP | | P1_DN_DLY | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 155. LED_P1_RAMP register (address 48h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | P1_UP_STEP | Pattern 1 LED Ramp Up PWM duty step size from 0 % to 100 %<br>**00 —** 128 steps (default)<br>**01 —** 64 steps<br>**10 —** 32 steps<br>**11 —** 16 step |
| 5 to 4 | P1_UP_DLY | Pattern 1 LED Ramp Up delay per step<br>**00 —** 4.096 ms (default)<br>**01 —** 8.192 ms<br>**10 —** 12.288 ms<br>**11 —** 16.384 ms |
| 3 to 2 | P1_DN_STEP | Pattern 1 LED Ramp Down PWM duty step size from 0 % to 100 %<br>**00 —** 128 steps (default)<br>**01 —** 64 steps<br>**10 —** 32 steps<br>**11 —** 16 step |
| 1 to 0 | P1_DN_DLY | Pattern 1 LED Ramp Down delay per step<br>**00 —** 4.096 ms (default)<br>**01 —** 8.192 ms<br>**10 —** 12.288 ms<br>**11 —** 16.384 ms |

### 8.2.64 LED_P1_BLNK

Pattern 1 LED blink time configuration

**Table 156. LED_P1_BLNK register (address 49h) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LEDTON1 | | | | LEDTOFF1 | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 157. LED_P1_BLNK register (address 49h) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | LEDTON1 | Pattern 1 LED ON Time Settings<br>See Table 158 |
| 5 to 4 | LEDTOFF1 | Pattern 1 LED OFF Time Settings<br>See Table 159 |

**Table 158. LEDTON1 values**

| | | | |
|---|---|---|---|
| **0x0 : 0.10 s** | 0x4 : 0.50 s | 0x8 : 1.50 s | 0xC : 2.50 s |
| 0x1 : 0.20 s | 0x5 : 0.75 s | 0x9 : 1.75 s | 0xD : 2.75 s |
| 0x2 : 0.30 s | 0x6 : 1.00 s | 0xA : 2.00 s | 0xE : 3.00 s |
| 0x3 : 0.40 s | 0x7 : 1.25 s | 0xB : 2.25 s | 0xF : 3.25 s |

**Table 159. LEDTOFF1 values**

| | | | |
|---|---|---|---|
| **0x0 : 0.10 s** | 0x4 : 0.50 s | 0x8 : 1.50 s | 0xC : 2.50 s |
| 0x1 : 0.20 s | 0x5 : 0.75 s | 0x9 : 1.75 s | 0xD : 2.75 s |
| 0x2 : 0.30 s | 0x6 : 1.00 s | 0xA : 2.00 s | 0xE : 3.00 s |
| 0x3 : 0.40 s | 0x7 : 1.25 s | 0xB : 2.25 s | 0xF : 3.25 s |

### 8.2.65 LED_P2_RAMP

Pattern 2 LED ramp up down configuration

**Table 160. LED_P2_RAMP register (address 4Ah) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | P2_UP_STEP | | P2_UP_DLY | | P2_DN_STEP | | P2_DN_DLY | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 161. LED_P2_RAMP register (address 4Ah) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 6 | P2_UP_STEP | Pattern 2 LED Ramp Up PWM duty step size from 0 % to 100 %<br>**00 —** 128 steps (default)<br>**01 —** 64 steps<br>**10 —** 32 steps<br>**11 —** 16 step |

**Table 161. LED_P2_RAMP register (address 4Ah) bit descriptions***...continued*

| Bit | Symbol | Description |
|---|---|---|
| 5 to 4 | P2_UP_DLY | Pattern 2 LED Ramp Up delay per step<br>**00 —** 4.096 ms (default)<br>**01 —** 8.192 ms<br>**10 —** 12.288 ms<br>**11 —** 16.384 ms |
| 3 to 2 | P2_DN_STEP | Pattern 2 LED Ramp Down PWM duty step size from 0 % to 100 %<br>**00 —** 128 steps (default)<br>**01 —** 64 steps<br>**10 —** 32 steps<br>**11 —** 16 step |
| 1 to 0 | P2_DN_DLY | Pattern 2 LED Ramp Down delay per step<br>**00 —** 4.096 ms (default)<br>**01 —** 8.192 ms<br>**10 —** 12.288 ms<br>**11 —** 16.384 ms |

## 8.2.66 LED_P2_BLNK

Pattern 2 LED blink time configuration

**Table 162. LED_P2_BLNK register (address 4Bh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | LEDTON2 | | | | LEDTOFF2 | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 163. LED_P2_BLNK register (address 4Bh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 4 | LEDTON2 | Pattern 2 LED ON Time Settings<br>See Table 164 |
| 3 to 0 | LEDTOFF2 | Pattern 2 LED OFF Time Settings<br>See Table 165 |

**Table 164. LEDTON2**

| | | | |
|---|---|---|---|
| **0x0 : 0.10 s** | 0x4 : 0.50 s | 0x8 : 1.50 s | 0xC : 2.50 s |
| 0x1 : 0.20 s | 0x5 : 0.75 s | 0x9 : 1.75 s | 0xD : 2.75 s |
| 0x2 : 0.30 s | 0x6 : 1.00 s | 0xA : 2.00 s | 0xE : 3.00 s |
| 0x3 : 0.40 s | 0x7 : 1.25 s | 0xB : 2.25 s | 0xF : 3.25 s |

**Table 165. LEDTOFF2**

| | | | |
|---|---|---|---|
| **0x0 : 0.10 s** | 0x4 : 0.50 s | 0x8 : 1.50 s | 0xC : 2.50 s |
| 0x1 : 0.20 s | 0x5 : 0.75 s | 0x9 : 1.75 s | 0xD : 2.75 s |

**Table 165. LEDTOFF2*...continued***

| | | | |
|---|---|---|---|
| 0x2 : 0.30 s | 0x6 : 1.00 s | 0xA : 2.00 s | 0xE : 3.00 s |
| 0x3 : 0.40 s | 0x7 : 1.25 s | 0xB : 2.25 s | 0xF : 3.25 s |

### 8.2.67 REG_LOCK

Output voltage configuration unlock key

**Table 166. REG_LOCK register (address 4Eh) bit allocation**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | UNLOCK_KEY | | | | | | | |
| **Reset** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Access** | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Table 167. REG_LOCK register (address 4Eh) bit descriptions**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 0 | UNLOCK_KEY | Unlock key is written to change regulator output configuration.<br>**01011100 —** Unlock regulator output configuration registers<br>**Others —** Lock regulator output configuration registers |

# 9 Application design-in information

## 9.1 Reference schematic

PCA9460 reference schematic with 8ULP is illustrated in Figure 24.

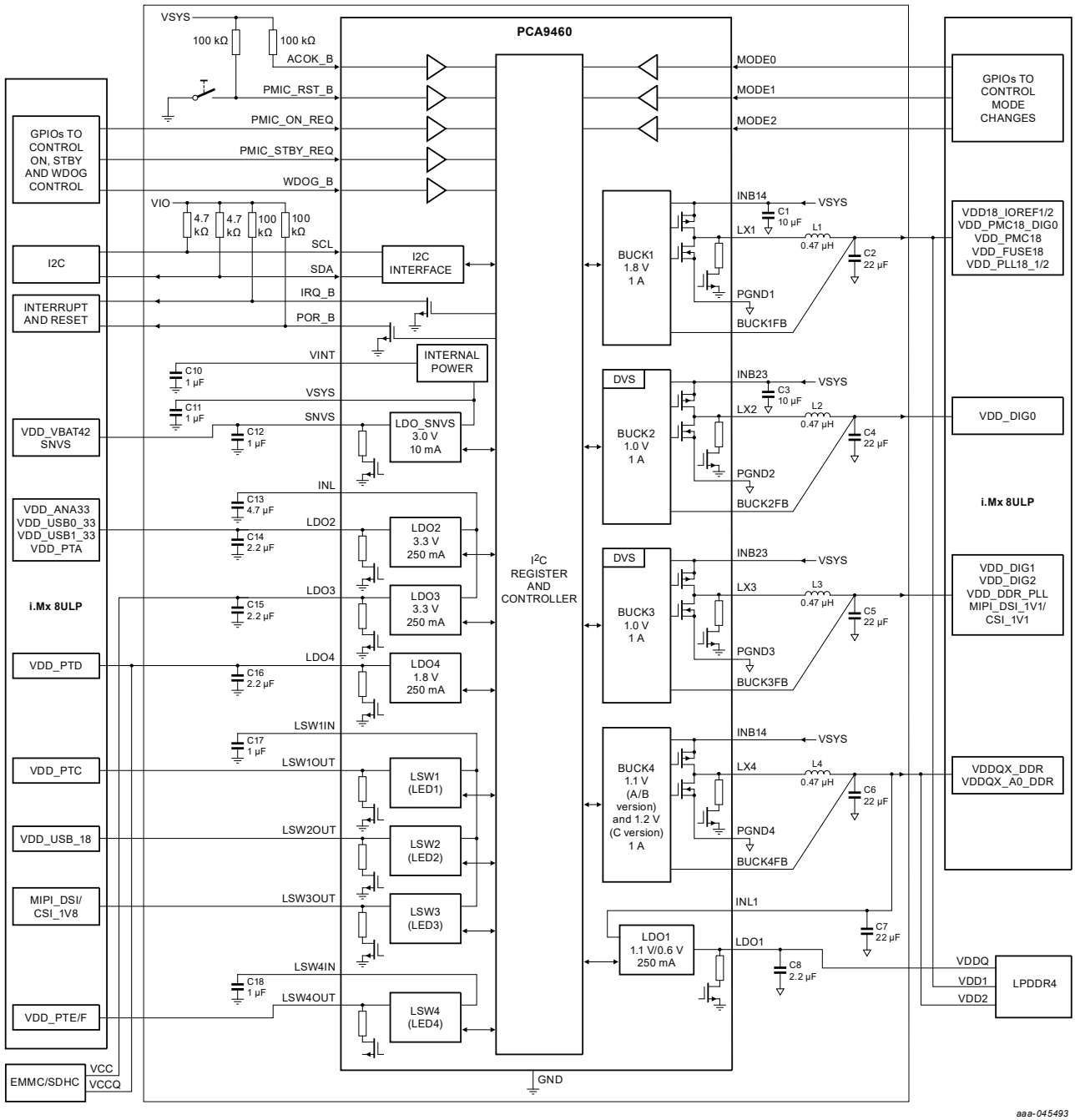



**Figure 24. PCA9460 i.Mx 8ULP application schematic**

### 9.1.1 External BOM in reference schematic

Table 168 shows external BOM in reference schematic

**Table 168. External BOM**

| Ref | Block | Pin | Part number | Size [mm] | Value |
|---|---|---|---|---|---|
| L1 | BUCK | LX1 | WPN252012ER47MT | 2012 | 0.47 µH |

**Table 168. External BOM***...continued*

| Ref | Block | Pin | Part number | Size [mm] | Value |
|---|---|---|---|---|---|
| L2 | BUCK | LX2 | WPN252012ER47MT | 2012 | 0.47 µH |
| L3 | BUCK | LX3 | WPN252012ER47MT | 2012 | 0.47 µH |
| L4 | BUCK | LX4 | WPN252012ER47MT | 2012 | 0.47 µH |
| C1 | BUCK | INB14 | GRM188R60J106ME | 1608 | 10 µF |
| C2 | BUCK | Buck Output | GRM158C80G226ME | 1005 | 22 µF |
| C3 | BUCK | INB23 | GRM188R60J106ME | 1608 | 10 µF |
| C4 | BUCK | BUCK Output | GRM158C80G226ME | 1005 | 22 µF |
| C5 | BUCK | BUCK Output | GRM158C80G226ME | 1005 | 22 µF |
| C6 | BUCK | BUCK Output | GRM158C80G226ME | 1005 | 22 µF |
| C7 | LDO | INL1 | GRM155R61C225KE | 1005 | 2.2 µF |
| C8 | LDO | LDO1 | GRM155R61C225KE | 1005 | 2.2 µF |
| C10 | VINT | VINT | GRM155R61C105KA | 1005 | 1 µF |
| C11 | VSYS | VSYS | GRM155R61C105KA | 1005 | 1 µF |
| C12 | LDO | LDOSNVS | GRM155R61C105KA | 1005 | 1 µF |
| C13 | LDO | INL | GRM155R60J475ME | 1005 | 4.7 µF |
| C14 | LDO | LDO2 | GRM155R61C225KE | 1005 | 2.2 µF |
| C15 | LDO | LDO3 | GRM155R61C225KE | 1005 | 2.2 µF |
| C16 | LDO | LDO4 | GRM155R61C225KE | 1005 | 2.2 µF |
| C17 | LSW | LSW1IN | GRM155R61C105KA | 1005 | 1 µF |
| C18 | LSW | LSW4IN | GRM155R61C105KA | 1005 | 1 µF |

## 9.2 Typical application

The PCA9460 devices have only a few design requirements. Use the following parameters for the design

- 1 µF bypass capacitor on VINT and VSYS, located as close as possible to those pins to ground
- Input capacitors must be present on the INB and INL supplies if used
- Output inductors and capacitors must be used on the outputs of the BUCK converters if used
- Output capacitors must be used on the outputs of the LDOs

### 9.2.1 Detailed design procedure

### 9.2.2 Inductor selection for buck converters

Each of the converters in the PCA9460 typically use a 0.47 µH output inductor which has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance must be selected for highest efficiency.

Equation 1 calculates the peak-to-peak inductor ripple current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 2. This is needed because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = V_{out} \times \frac{1-\frac{V_{out}}{V_{in\_max}}}{L \times f} \quad (1)$$

$$I_{L.max} = I_{out.max} + \frac{\Delta I_L}{2} \quad (2)$$

Where

f = switching frequency ( 2 MHz )

L = Inductance

$\Delta I_L$ = Peak to peak inductor ripple current

$I_{L.max}$ = Maximum inductor current

$I_{out.max}$ = Maximum output DC current

A conservative approach is to select the inductor current rating just for the maximum switch current of the PCA9460

### 9.2.3 Output capacitor selection for buck converters

The fast response adaptive constant ON time control scheme of the buck converters implemented in the PCA9460 allow the use of small ceramic capacitors with a typical value of 22 µF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 19 for recommended.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated in Equation 3.

$$I_{RMS.COUT} = \mathrm{Vout} \times \frac{1-\frac{\mathrm{Vout}}{\mathrm{Vin}}}{\mathrm{L} \times \mathrm{f}} \times \frac{1}{2\sqrt{3}} \quad (3)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta \mathrm{Vout} = \mathrm{Vout} \times \frac{1-\frac{Vout}{Vin}}{\mathrm{L} \times \mathrm{f}} \times \left( \frac{1}{8 \times Cout \times f} + ESR \right) \quad (4)$$

Where

The highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in PFM mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1 % of the nominal output voltage.

### 9.2.4 Input capacitor selection for buck converters

Low ESR input capacitor is highly recommended for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes because of the nature of buck converter. Each DC-DC

converter requires a 10 µF ceramic input capacitor on its input pins. The input capacitor could be increased without any limit for better input voltage filtering.

## 9.3 Layout guide

Figure 25 shows layout guidance.

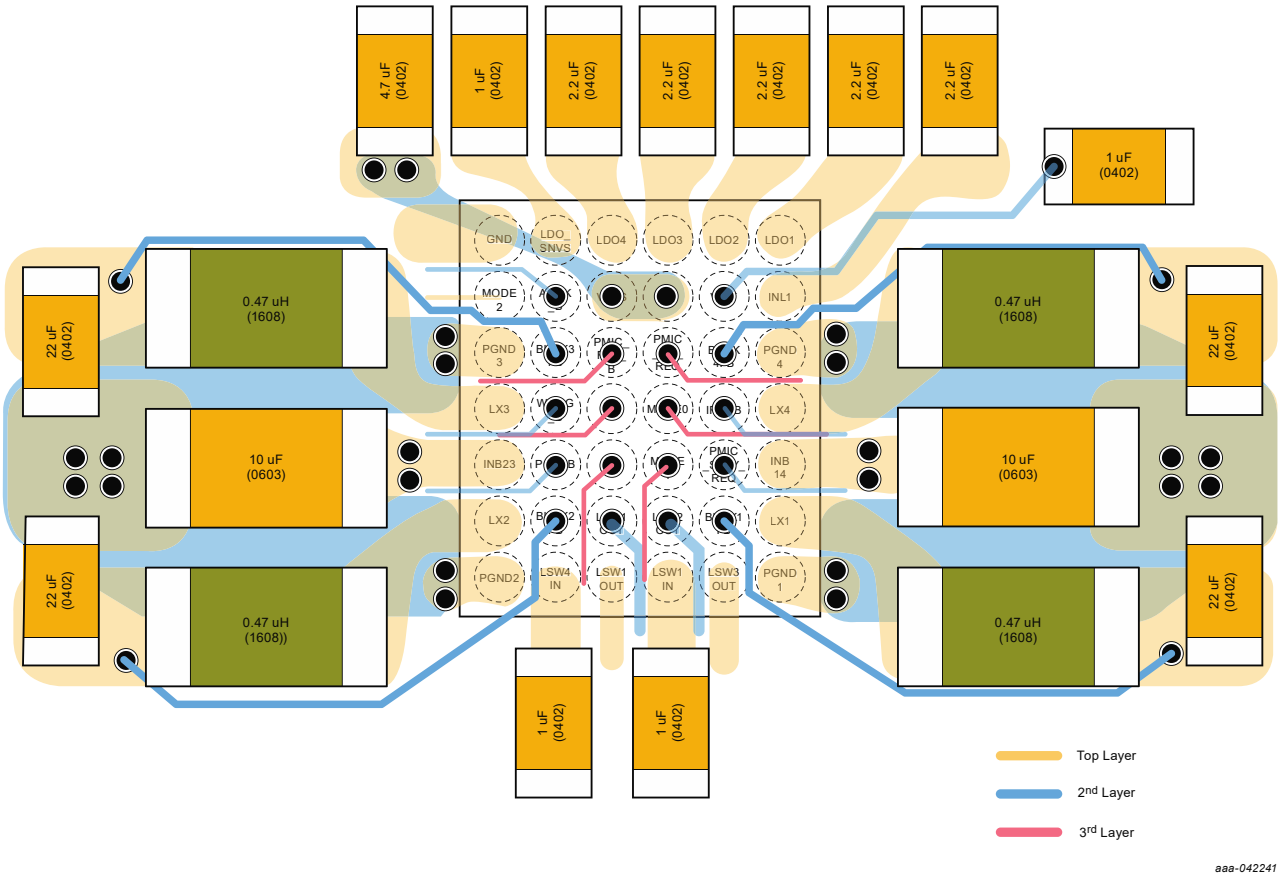



**Figure 25. PCA9460 layout**

# 10 Limiting values

**Table 169. Limiting values (Absolute Maximum Ratings)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{range(gnd)}$ | voltage range (with respect to GND) | pins VSYS, INL | -0.5 | +6.0 | V |
| | | pins INB14, INB23, INL1 | -0.5 | VSYS + 0.5 | V |
| | | pins LX1, LX4 | -0.5 | INB14 + 0.5 | V |
| | | pins LX2, LX3 | -0.5 | INB23 + 0.5 | V |
| | | pins BUCK1FB, BUCK2FB, BUCK3FB, BUCK4FB | -0.5 | VSYS + 0.5 | V |
| | | pin LDO1 | -0.5 | $V_{INL1}$+0.5 | V |
| | | pins LDO2, LDO3, LDO4 | -0.5 | $V_{INL}$+0.5 | V |

**Table 169. Limiting values (Absolute Maximum Ratings)*...continued***

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| | | pin VINT | -0.5 | +1.8 | V |
| | | pins LSWx_CFG = 0, LSW; LSW1IN, LSW4IN | -0.5 | VSYS + 0.5 | V |
| | | pins LSWx_CFG = 1, LED; LSW1IN, LSW4IN | -0.5 | +6.0 | V |
| | | pins LSW1OUT, LSW2 OUT, LSW3OUT | -0.5 | $V_{LSW1IN}$+0.5 | V |
| | | pins LSW4OUT | -0.5 | $V_{LSW4IN}$+0.5 | V |
| | | pins PMIC_ON_REQ, POR_B PMIC_STBY_ REQ, WDOG_B, IRQ_B, SCL, SDA, MODE0, MODE1, MODE2 | -0.5 | VSYS + 0.5 | V |
| | | pins ACOK_B, PMIC_ RST_B | -0.5 | VSYS + 0.5 | V |
| $I_O$ | output current | pins LX1, LX2, LX3, LX4; RMS current | | 1.5 | A |
| | | pins LSW1OUT, LSW2 OUT, LSW3OUT, LSW4OUT | | 0.3 | A |
| $T_j$ | junction temperature | | -40 | +150 | °C |
| $V_{ESD}$ | electrostatic discharge voltage - all pins | HBM (JESD22-001) | -2 | +2 | kV |
| | | CDM (JESD22-C101E) | -500 | 500 | V |

# 11 Recommended operating conditions

**Table 170. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{range(gnd)}$ | voltage range (with respect to GND) | on pins VSYS, INL1, INL | 2.7 | 5.5 | V |
| | | on pins INB14, INB23 | 2.7 | 5.5 | V |
| | | on pins LSW1IN, LSW4IN | 1.2 | 5.5 | V |
| $T_j$ | junction temperature | | -40 | +125 | °C |
| $T_{amb}$ | ambient temperature | | -40 | +85 | °C |
| $T_{stg}$ | storage temperature | | -55 | +85 | °C |

# 12 Thermal characteristics

**Table 171. Thermal characteristics**

| Symbol | Parameter | Board Type[1] | Typ | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance from junction to ambient[2] | JESD51-9, 2s2p | 46 | °C/W |

**Table 171. Thermal characteristics**...*continued*

| Symbol | Parameter | Board Type[1] | Typ | Unit |
|---|---|---|---|---|
| $\Psi_{JT}$ | Junction to Top of package Thermal Characterization Parameter[2] | JESD51-9, 2s2p | 2 | °C/W |

[1] Thermal test board meets JEDEC specification for this package (JESD51-9)
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

## 12.1 Rating data

Junction to ambient thermal resistance nomenclature: the JEDEC specification reserves the symbol RθJA or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in a natural convection environment. RθJMA or θJMA (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated the generic name, Theta-JA, continues to be commonly used. The JEDEC standards can be consulted at http://www.jedec.org.

## 12.2 Estimation of junction temperature

An estimation of the chip junction temperature TJ can be obtained from the equation:

TJ = TA + (RθJA x PD)

with:

TA = Ambient temperature for the package in °C

RθJA = Junction to ambient thermal resistance in °C/W

PD = Power dissipation in the package in W

The junction-to-ambient thermal resistance is an industry standard value providing a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board RθJA and the value obtained on a four-layer board RθJMA. Actual application PCBs show a performance close to the simulated four-layer board value, although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature TJ is estimated using the following equation:

TJ = TB + (RθJB x PD)

with:

TB = Board temperature at the package perimeter in °C

RθJB = Junction to board thermal resistance in °C/W

PD = Power dissipation in the package in W

# 13 Electrical characteristics

## 13.1 Top level parameter

**Table 172. Top level parameter description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Quiescent Current** | | | | | | | |
| $I_{Q\_Shutdown}$ | Shutdown Current | LDOSNVS are ON and no load, PMIC_ ON_REQ = L | 25 °C | | 1.4 | 3 | µA |
| | | | -40 °C ~ 85 °C | | 1.4 | 20 | |
| $I_{Q\_STDBY\_1}$ | System Standby current at low power mode | LDOSNVS and BUCK1 are ON and no load. PWR_SAVE = 01b, Bx_LPMODE = 01b, PMIC_STBY_REQ= H | 25 °C | | 3.5 | 7 | µA |
| | | | -40 °C ~ 85 °C | | 3.5 | 22 | |
| $I_{Q\_STDBY\_2}$ | System Standby current | All Regulators are ON and no load. PWR_SAVE = 01b, Bx_LPMODE = 01b, PMIC_STBY_REQ= H | 25 °C | | 8.8 | 20 | µA |
| | | | –40 °C ~ 85 °C | | 8.8 | 35 | |
| | | All Regulators are ON and no load. PWR_SAVE = 11b, Bx_LPMODE = 01b, PMIC_STBY_REQ= H | 25 °C | | 20 | 32 | µA |
| | | | –40 °C ~ 85 °C | | 20 | 55 | |
| $I_{Q\_ACTIVE}$ | System Active current | All Regulators are ON and no load. PWR_SAVE = 01b, Bx_LPMODE = 11b, PMIC_STBY_REQ= L | –40 °C ~ 85 °C | 20 | 35 | 85 | µA |
| **VSYS** | | | | | | | |
| $V_{SYS\_UVLO}$ | VSYS UVLO | Rising – OTP Programmable<br>00b = 2.65 V<br>**01b = 2.85 V**<br>10b = 3.0 V<br>11b = 3.3 V | | 2.7 | 2.85 | 3.0 | V |
| $V_{SYS\_UVLO\_H}$ | VSYS UVLO Hysteresis | Falling | | | 200 | | mV |
| **VINT** | | | | | | | |
| VINT | Internal Power supply | VSYS = 3.8 V | | 1.4 | 1.5 | 1.6 | V |
| **Low VSYS** | | | | | | | |
| $V_{LOW\_VSYS}$ | Low VSYS | Low VSYS threshold above $V_{SYS\_UVLO}$, LOW_VSYS [7:6] = 01b | | 150 | 200 | 250 | mV |
| $V_{LOW\_VSYS\_HYS}$ | Low VSYS Hysteresis | | | | 100 | | mV |
| **Thermal Shutdown** | | | | | | | |
| $T_{JSHDN}$ | Thermal Shutdown | Tj Rising, 15°C hysteresis | | | 150 | | °C |
| $T_{J80}$ | Thermal interrupt1 | Tj Rising, 15°C hysteresis | | | 80 | | °C |
| $T_{J100}$ | Thermal interrupt2 | Tj Rising, 15°C hysteresis | | | 100 | | °C |
| $T_{JHYS}$ | Thermal Hysteresis | | | | 15 | | °C |
| **Logic and Control signals** | | | | | | | |
| $V_{IL}$ | Input Low level | PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, MODE0, MODE1, MODE2, PMIC_RST_B, ACOK_B | | | | 0.4 | V |

**Table 172. Top level parameter description***...continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High level | PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, MODE0, MODE1, MODE2, PMIC_RST_B, ACOKB | 1.4 | | | V |
| $I_{LEAK}$ | Logic Input leakage current | PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, MODE0, MODE1, MODE2, PMIC_RST_B, ACOKB $V_{Logic}$ = 5.5 V, VSYS = 5.5 V | -1 | | +1 | µA |
| $V_{OL}$ | Output Low level | IRQ_B, POR_B, $I_{OL}$ = 6mA | | | 0.4 | V |
| $I_{LEAK}$ | Output high leakage current | IRQ_B, POR_B, $V_{Logic}$ = 5.5 V, VSYS = 5.5 V | -1 | | +1 | µA |
| **Timing spec** | | | | | | |
| $t_{SNVS}$ | Maximum time to enable LDO_SNVS from VSYS UVLO detected | | | 20 | | ms |
| $t_{ON\_DEB}$ | PMIC_ON_REQ debounce time | | 40 | 50 | 60 | µs |
| $t_{ACOK\_B\_DEB}$ | ACOK_B debounce time | Falling | 40 | 50 | 60 | ms |
| $t_{ACOK\_ONESHOT}$ | ACOK_B Oneshot timer | Programmable, ACOK_B_OSTMR = 0b | | 2.5 | | sec |
| $t_{DEB\_PMIC\_RST\_B}$ | Debounce time of PMIC_RST_B | Programmable, PMIC_RST_B_DEB = 0b | 16 | 20 | 24 | ms |
| $t_{ONKEY}$ | ON KEY timer of PMIC_RST_B | Programmable, ONKEY_TIMER = 01b | 1.6 | 2 | 2.4 | sec |
| $t_{RESETKEY}$ | RESET KEY timer of PMIC_RST_B | Programmable, RESETKEY_TIMER = 101b | 7.2 | 8 | 9.6 | sec |
| $t_{RESET\_WAIT}$ | Wait time from RESETKEY detection to perform reset | | 80 | 100 | 120 | ms |
| $t_{ON\_STEP}$ | Time step to turn on each regulator | Programmable, PSQ_TON_STEP = 01b | 1.6 | 2 | 2.4 | ms |
| $t_{POK\_EXP}$ | POK wait timerout during power ON sequence | | 8 | 10 | 12 | ms |
| $t_{OFF\_STEP}$ | Time step to turn off each regulator | Programmable, PSQ_TOFF_STEP = 10b | 6 | 8 | 10 | ms |
| $t_{RSTB}$ | Time from PUD_T16 Gr POK to POR_B release during Power on seq | | 16 | 20 | 24 | ms |
| $t_{FLT\_THSD\_DEB}$ | Debounce Time for Thermal fault | | 16 | 20 | 24 | µs |
| $t_{DEB\_POKB}$ | Debounce time of regulator POKB | | 240 | 300 | 360 | µs |
| $t_{FLT\_SD\_WAIT}$ | Wait time to enter FAULT_SD after fault interrupt | At Standby and Run mode, programmable, tFLT_SD_WAIT = 0b | 80 | 100 | 120 | ms |
| $t_{FLT\_SD\_STAY}$ | Time to stay at FAULT_SD to move other mode | | 80 | 100 | 120 | ms |
| $t_{RESTART}$ | Wait time to start power up after power down at cold reset | Programmable, Trestart = 0b | 200 | 250 | 300 | ms |
| $t_{PWR\_HOLD\_RST}$ | Power Hold time after reset is performed | | 80 | 100 | 120 | ms |
| $t_{RESET}$ | POR_B low time at Warm reset | | 16 | 20 | 24 | ms |
| $t_{DEB\_WDOGB}$ | Debounce time of WDOG_B | | 40 | 50 | 60 | µs |
| $t_{FLT\_POK\_MSK}$ | POK mask time when regulator is enabled at RUN/Standby mode | | 2.4 | 3 | 3.6 | ms |

**Table 172. Top level parameter description***...continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DVS Timing spec** | | | | | | |
| $t_{MAX\_DIFF}$ | Maximum latency of MODE pins | SMART_MODE = 0b | | | 0.1 | µs |
| $t_{DVS\_EFF}$ | | SMART_MODE = 0b | | 3 | 4 | µs |
| $t_{SETUP\_MODE2}$ | MODE2 pin Setup time to select BUCK regulator | SMART_MODE = 1b | 3 | | | µs |
| $t_{MIN\_H}$ | MODE0, MODE1 pin Minimum High time | SMART_MODE = 1b | 3 | | | µs |
| $t_{MIN\_L}$ | MODE0, MODE1 pin Minimum Low time | SMART_MODE = 1b | 2 | | | µs |
| $t_{MIN\_GAP}$ | Minimum time to start MODE1 from falling edge of MODE0, vice versa | SMART_MODE = 1b | 3 | | | µs |

## 13.2 BUCK1

**Table 173. BUCK1 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{INB1}$ | Input voltage range | INB14 pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Low power mode, IOUT = 0A, 25 °C | | 1.3 | 2.5 | µA |
| | | Normal mode, IOUT = 0A [1] | | 5.2 | 11 | µA |
| $I_{OUT\_MAX}$ | Max Output Current | Low power mode, $V_{BUCK1}$ = 1.8 V | | | 100 | mA |
| | | Normal mode | 1000 | | | mA |
| $V_{BUCK1\_RANGE}$ | Programmable Output voltage range | $I^2C$ programmable, 25 mV/step | 0.6 | | 3.4 | V |
| $V_{BUCK1}$ | DC Output Voltage Accuracy | $V_{INB1}$ = 3.8 V, $V_{BUCK1}$ = 1.8 V, IOUT = 0A, FPWM mode, Normal mode | -2 | | 2 | % |
| | | $V_{INB1}$ = 3.8 V, $V_{BUCK1}$ = 1.8 V, IOUT = 10 mA, Low power mode | -3 | | 3 | % |
| $\Delta V_{OUT(\Delta VINB)}$ | DC Line regulation | $V_{INB1}$ = 3 V to 5 V, $I_{OUT}$= $I_{OUT\_MAX}$ [1] | | 2 | | mV/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | 0 mA < $I_{OUT}$ < $I_{OUT\_MAX}$, $V_{BUCK1}$ = 1.8 V [1] | | 3 | | mV/A |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $I_{OUT}$ changes 0 to $I_{OUT\_MAX}$ ( 1A/us slope ), $V_{BUCK1}$ = 1.8 V [1] | | 50 | | mV |
| $\Delta V_{OUT}$ | Output voltage Ripple | FPWM mode [1] | | 10 | | mV |
| $f_{SW}$ | Switching Frequency in CCM | | | 2 | | MHz |
| $R_{DSON}$ | High Side P-FET $R_{DSON}$ | $V_{INB1}$ = 3.8 V | | 200 | | mΩ |
| | Low Side N-FET $R_{DSON}$ | $V_{INB1}$ = 3.8 V | | 90 | | mΩ |
| $I_{LIM}$ | High side current limit | $V_{INB1}$ = 3.8 V | 2.2 | 2.4 | 2.6 | A |
| | Low side current limit | $V_{INB1}$ = 3.8 V | 0.8 | 1 | 1.2 | A |
| $t_{START}$ | Startup time | EN rising to 90 % of output voltage [1] | | 500 | 700 | µs |
| $V_{RAMP}$ | Output voltage slew rate | Programmable, RAMP[1:0] = 01b [1] | | 12.5 | | mV/us |
| $V_{soft\_strup}$ | Soft-start slew rate | [1] | | 12.5 | | mV/us |
| $R_{DIS}$ | Output Active Discharge Resistance | | | 100 | 150 | Ω |

**Table 173. BUCK1 description**...*continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| POK | Output Power good | | | 85 | 95 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| L | Inductor value | [1] | | 0.47 | | µH |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 22 | | | µF |

[1] Not tested in production. Guaranteed by design

## 13.3 BUCK2

**Table 174. BUCK2 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{INB2}$ | Input voltage range | INB23 pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Low power mode, IOUT = 0A, 25 °C | | 1.3 | 2.5 | µA |
| | | Normal mode, IOUT = 0A [1] | | 5.2 | 11 | µA |
| $I_{OUT\_MAX}$ | Max Output Current | Low power mode | | | 100 | mA |
| | | Normal mode | 1000 | | | mA |
| $V_{BUCK2\_RANGE}$ | Programmable Output voltage range | $I^2C$ programmable, 12.5 mV/step | 0.6 | | 2.1875 | V |
| $V_{BUCK2}$ | DC Output Voltage Accuracy | $V_{INB2}$ = 3.8 V, $V_{BUCK2}$ = 1.0 V, IOUT = 0A, FPWM mode, Normal mode | -2 | | 2 | % |
| | | $V_{INB2}$ = 3.8 V, $V_{BUCK2}$ = 1.0 V, IOUT = 10 mA, Low power mode | -3 | | 3 | % |
| $\Delta V_{OUT(\Delta VINB)}$ | DC Line regulation | $V_{INB2}$ = 3 V to 5 V, $I_{OUT}$= $I_{OUT\_MAX}$ [1] | | 2 | | mV/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | 0 mA < $I_{OUT}$ < $I_{OUT\_MAX}$, $V_{BUCK2}$ = 1.0 V [1] | | 3 | | mV/A |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $I_{OUT}$ changes 0 to $I_{OUT\_MAX}$ ( 1A/ us slope ), $V_{BUCK2}$ = 1.0 V [1] | | 50 | | mV |
| $\Delta V_{OUT}$ | Output voltage Ripple | FPWM mode [1] | | 10 | | mV |
| $f_{SW}$ | Switching Frequency in CCM | | | 2 | | MHz |
| $R_{DSON}$ | High Side P-FET $R_{DSON}$ | $V_{INB2}$ = 3.8 V | | 200 | | mΩ |
| | Low Side N-FET $R_{DSON}$ | $V_{INB2}$ = 3.8 V | | 90 | | mΩ |
| $I_{LIM}$ | High side current limit | $V_{INB2}$ = 3.8 V | 2.2 | 2.4 | 2.6 | A |
| | Low side current limit | $V_{INB2}$ = 3.8 V | 0.8 | 1 | 1.2 | A |
| $t_{START}$ | Startup time | EN rising to 90 % of output voltage [1] | | 500 | 700 | µs |
| $V_{RAMP}$ | Output voltage slew rate | Programmable, RAMP[1:0] = 01b [1] | | 12.5 | | mV/us |

**Table 174. BUCK2 description**...*continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{soft\_strup}$ | Soft-start slew rate | [1] | | 12.5 | | mV/us |
| POK | Output Power good | | 75 | 85 | 95 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| $R_{DIS}$ | Output Active Discharge Resistance | | | 100 | 150 | Ω |
| L | Inductor value | [1] | | 0.47 | | µH |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 20 | | | µF |

[1] Not tested in production. Guaranteed by design

## 13.4 BUCK3

**Table 175. BUCK3 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{INB3}$ | Input voltage range | INB23 pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Low power mode, IOUT = 0A, 25 °C | | 1.3 | 2.5 | µA |
| | | Normal mode, IOUT = 0A [1] | | 5.2 | 11 | µA |
| $I_{OUT\_MAX}$ | Max Output Current | Low power mode | | | 100 | mA |
| | | Normal mode | 1000 | | | mA |
| $V_{BUCK3\_RANGE}$ | Programmable Output voltage range | $I^2C$ programmable, 12.5 mV/step | 0.6 | | 2.1875 | V |
| $V_{BUCK3}$ | DC Output Voltage Accuracy | $V_{INB3}$ = 3.8 V, $V_{BUCK3}$ = 1.0 V, IOUT = 0A, FPWM mode, Normal mode | | | | |
| | | • -40 °C to 85 °C | -1.0 | | +3.0 | % |
| | | • 0 °C to 85 °C | -0.5 | | 2.25 | % |
| | | $V_{INB3}$ = 3.8 V, $V_{BUCK3}$ = 1.0 V, IOUT = 10 mA, Low power mode | | | | |
| | | • -40 °C to 85 °C | -2.0 | | +4.0 | % |
| $\Delta V_{OUT(\Delta VINB)}$ | DC Line regulation | $V_{INB3}$ = 3 V to 5 V, $I_{OUT}$= $I_{OUT\_MAX}$ [1] | | 2 | | mV/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | 0 mA < $I_{OUT}$ < $I_{OUT\_MAX}$, $V_{BUCK3}$ = 1.0 V [1] | | 3 | | mV/A |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $I_{OUT}$ changes 0 to $I_{OUT\_MAX}$ ( 1A/ us slope ), $V_{BUCK3}$ = 1.0 V [1] | | 50 | | mV |
| $\Delta V_{OUT}$ | Output voltage Ripple | FPWM mode [1] | | 10 | | mV |
| $f_{SW}$ | Switching Frequency in CCM | | | 2 | | MHz |
| $R_{DSON}$ | High Side P-FET $R_{DSON}$ | $V_{INB3}$ = 3.8 V | | 200 | | mΩ |

**Table 175. BUCK3 description***...continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Low Side N-FET $R_{DSON}$ | $V_{INB3}$ = 3.8 V | | 90 | | mΩ |
| $I_{LIM}$ | High side current limit | $V_{INB3}$ = 3.8 V | 2.2 | 2.4 | 2.6 | A |
| | Low side current limit | $V_{INB3}$ = 3.8 V | 0.8 | 1 | 1.2 | A |
| $t_{START}$ | Startup time | EN rising to 90 % of output voltage [1] | | 500 | 700 | µs |
| $V_{RAMP}$ | Output voltage slew rate | Programmable, RAMP[1:0] = 01b [1] | | 12.5 | | mV/us |
| $V_{soft\_strup}$ | Soft-start slew rate | [1] | | 12.5 | | mV/us |
| POK | Output Power good | | 75 | 85 | 95 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| $R_{DIS}$ | Output Active Discharge Resistance | | | 100 | 150 | Ω |
| L | Inductor value | [1] | | 0.47 | | µH |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 20 | | | µF |

[1] Not tested in production. Guaranteed by design

## 13.5 BUCK4

**Table 176. BUCK4 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{INB4}$ | Input voltage range | INB14 pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Low power mode, IOUT = 0A, 25 °C | | 1.3 | 2.5 | µA |
| | | Normal mode, IOUT = 0A [1] | | 5.2 | 11 | µA |
| $I_{OUT\_MAX}$ | Max Output Current | Low power mode | | | 100 | mA |
| | | Normal mode | 1000 | | | mA |
| $V_{BUCK4\_RANGE}$ | Programmable Output voltage range | $I^2C$ programmable, 25 mV/step | 0.6 | | 3.4 | V |
| $V_{BUCK4}$ | DC Output Voltage Accuracy | $V_{INB4}$ = 3.8 V, $V_{BUCK3}$ = 1.1V, IOUT = 0A, FPWM mode, Normal mode | -2 | | 2 | % |
| | | $V_{INB4}$ = 3.8 V, $V_{BUCK3}$ = 1.1V, IOUT = 10 mA, Low power mode | -3 | | 3 | % |
| $\Delta V_{OUT(\Delta VINB)}$ | DC Line regulation | $V_{INB4}$ = 3 V to 5 V, $I_{OUT}$= $I_{OUT\_MAX}$ [1] | | 2 | | mV/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | 0 mA < $I_{OUT}$ < $I_{OUT\_MAX}$, $V_{BUCK4}$ = 1.8 V [1] | | 3 | | mV/A |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $I_{OUT}$ changes 0 to $I_{OUT\_MAX}$ ( 1A/ us slope ), $V_{BUCK4}$ = 1.1V [1] | | 50 | | mV |

**Table 176. BUCK4 description***...continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{OUT}$ | Output voltage Ripple | FPWM mode [1] | | 10 | | mV |
| $f_{SW}$ | Switching Frequency in CCM | | | 2 | | MHz |
| $R_{DSON}$ | High Side P-FET $R_{DSON}$ | $V_{INB4}$ = 3.8 V | | 200 | | mΩ |
| | Low Side N-FET $R_{DSON}$ | $V_{INB4}$ = 3.8 V | | 90 | | mΩ |
| $I_{LIM}$ | High side current limit | $V_{INB4}$ = 3.8 V | 2.2 | 2.4 | 2.6 | A |
| | Low side current limit | $V_{INB4}$ = 3.8 V | 0.8 | 1 | 1.2 | A |
| $t_{START}$ | Startup time | EN rising to 90 % of output voltage [1] | | 500 | 700 | µs |
| $V_{RAMP}$ | Output voltage slew rate | Programmable, RAMP[1:0] = 01b [1] | | 12.5 | | mV/us |
| $V_{soft\_strup}$ | Soft-start slew rate | [1] | | 12.5 | | mV/us |
| $R_{DIS}$ | Output Active Discharge Resistance | | | 100 | 150 | Ω |
| POK | Output Power good | | | 85 | 95 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| L | Inductor value | [1] | | 0.47 | | µH |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 20 | | | µF |

[1] Not tested in production. Guaranteed by design

## 13.6 LDO_SNVS

**Table 177. LDO_SNVS description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LDOSNVS}$ = 3.0 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | VSYS pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Regulator enabled, No load | | 0.23 | 0.5 | µA |
| $I_{OUT\_MAX}$ | Maximum Output DC Current | $V_{LDOSNVS}$ = 3.3 V | 10 | | | mA |
| $I_{LIMIT}$ | Short Current Limit | Output shorted to GND | 20 | | | mA |
| $V_{DO}$ | Dropout Voltage | $I_{OUT}$ = $I_{OUT\_MAX}$, $V_{SYS}$ = 3.2V, $V_{LDOSNVS}$ =3.3 V | | 25 | 50 | mV |
| $V_{LDOSNVS}$ | Nominal output voltage | $I^2C$ Programmable, 100mV step | 0.8 | | 3.3 | V |
| | Default voltage | | | 3.0 | | V |
| | DC accuracy | $V_{LDOSNVS}$ = 3.0 V, $I_{Load}$ = 5mA | -3 | | 3 | % |
| $V_{NOISE}$ | Output noise | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{MAX}$, $V_{LDOSNVS}$ = 3.0 V [1] | | 450 | | µV |
| $\Delta V_{OUT(\Delta VINL)}$ | DC Line regulation | $V_{LDOSNVS}$ +0.3 V < $V_{SYS}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ | | 0.2 | | %/V |

**Table 177. LDO_SNVS description**...*continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LDOSNVS}$ = 3.0 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | $V_{SYS}$ = $V_{LDOSNVS}$ +0.3 V to 5.5 V, 0 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ | | 0.25 | | % |
| $\Delta V_{OUT(\Delta VINL)}$ | Transient Line Response | $V_{LDOSNVS}$ +0.3 V < $V_{SYS}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ [1] | | 3 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $V_{SYS}$ = $V_{LDOSNVS}$ +0.3 V to 5.5 V, 1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ , tr = 10 µs, $V_{LDOSNVS}$ = 3.3 V, $T_A$= 25 °C [1] | -1 | | 1 | % |
| PSRR | Power Supply Rejection ratio | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ [1] | | 36 | | dB |
| $V_{soft\_strup}$ | Soft-start slew rate | $I_{OUT}$ = 0 mA, 10 % to 90 % of $V_{LDOSNVS}$ [1] | | 6.0 | | mV/µs |
| $V_{ov\_srtup}$ | Overshoot at startup | $I_{OUT}$ = 0 mA [1] | | | 10 | mV |
| $t_{EN}$ | Enable time | EN rising to 90 % of output voltage [1] | | 700 | 1500 | µs |
| POK_90 | Output Power good | Percentage of $V_{LDOSNVS}$ configuration | 86 | 90 | 94 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| $R_{DIS}$ | Active Discharge Resistance | | 50 | 100 | 150 | Ω |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 1 | | | µF |

[1] Not tested in production. Guaranteed by design

## 13.7 LDO1

**Table 178. LDO1 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = 1.1V ($V_{BUCK4}$), $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | INL1 pin, VSYS > $V_{LDO1}$ + 1.5 V [1] | $V_{LDO1}$ + $V_{DO}$ | | 5.5 | V |
| $I_Q$ | Quiescent current | Regulator enabled, No load, Low power mode | | 0.35 | 0.6 | µA |
| | | Regulator enabled, No load, Normal power mode | | 0.5 | 0.8 | µA |
| $I_{OUT\_MAX}$ | Maximum Output DC Current | $V_{INL1}$ > $V_{LDO1}$ + 0.2 V, $V_{LDO1}$ = 0.6 V | 250 | | | mA |
| $I_{LIMIT}$ | Short Current Limit | Output shorted to GND | 260 | | | mA |
| $V_{DO}$ | Dropout Voltage | $I_{OUT}$ = $I_{OUT\_MAX}$, $V_{INL1}$ = 1.8 V, L1_OUT = 2V, VSYS > $V_{LDO1}$ + 1.5 V | | 100 | 175 | mV |
| $V_{LDO1}$ | Nominal output voltage | $I^2C$ Programmable, 50 mV/step | 0.6 | | 1.95 | V |
| | Default voltage | | | 0.6 | | V |

**Table 178. LDO1 description**...*continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = 1.1V ($V_{BUCK4}$), $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | DC accuracy | $V_{LDO1}$ = 0.6 V, $I_{Load}$ = 5 mA | -2 | | 2 | % |
| $V_{NOISE}$ | Output noise | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{MAX}$, $V_{LDO1}$ = 0.6 V [1] | | 66 | | µV |
| $\Delta V_{OUT(\Delta VINL)}$ | DC Line regulation | $V_{LDO1}$ +0.3 V < $V_{INL1}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ | | 0.01 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | $V_{INL1}$ = $V_{LDO1}$ +0.3 V to 5.5 V, 0.1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ | | 0.15 | | % |
| $\Delta V_{OUT(\Delta VINL)}$ | Transient Line Response | $V_{LDO1}$ +0.3 V < $V_{INL1}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$, tr = 10 µs [1] | | 3 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $V_{INL1}$ = $V_{LDO1}$ +0.3 V to 5.5 V, 1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ , tr = 10 µs, $V_{LDO1}$ = 1.1 V [1] | -3 | | 5 | % |
| PSRR | Power Supply Rejection ratio | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ [1] | | 55 | | dB |
| $V_{soft\_strup}$ | Soft-start slew rate | $I_{OUT}$ = 0 mA, 10 % to 90 % of $V_{LDO1}$ [1] | | 10 | | mV/µs |
| $V_{ov\_srtup}$ | Overshoot at startup | $I_{OUT}$ = 0 mA [1] | | | 18 | mV |
| $t_{EN}$ | Enable time | EN rising to 90 % of output voltage at $V_{LDO1}$ = 0.6 V [1] | | 200 | 250 | µs |
| POK_90 | Output Power good | Delta from $V_{LDO1}$ Target | 87 | 90 | 93 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| $R_{DIS}$ | Active Discharge Resistance | | | 100 | 180 | Ω |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 2.2 | | 10 | µF |

[1] Not tested in production. Guaranteed by design

## 13.8 LDO2

**Table 179. LDO2 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | INL pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Regulator enabled, No load | | 0.23 | 0.5 | µA |
| $I_{OUT\_MAX}$ | Maximum Output DC Current | $V_{LDO2}$ = 3.3 V | 250 | | | mA |
| $I_{LIMIT}$ | Short Current Limit | Output shorted to GND | 260 | 310 | | mA |
| $V_{DO}$ | Dropout Voltage | $I_{OUT}$ = $I_{OUT\_MAX}$, $V_{INL}$ = 3.2 V, L2_OUT = 3.3 V | | 60 | 100 | mV |
| $V_{LDO2}$ | Nominal output voltage | $I^2C$ Programmable, 50 mV/step | 0.8 | | 3.3 | V |
| | Default voltage | VSEL = L | | 3.3 | | V |
| | Default voltage | VSEL = H | | 1.8 | | V |

**Table 179. LDO2 description**...*continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | DC accuracy | $V_{LDO2}$ = 3.3 V, $I_{Load}$ = 5 mA | -2 | | 2 | % |
| $V_{NOISE}$ | Output noise | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{MAX}$, $V_{LDO2}$ = 1.8 V [1] | | 150 | | µV |
| $\Delta V_{OUT(\Delta VINL)}$ | DC Line regulation | $V_{LDO2}$ +0.3 V < $V_{INL}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ | | 0.15 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | $V_{INL}$ = $V_{LDO2}$ +0.3 V to 5.5 V, 0.1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ | | 0.15 | | % |
| $\Delta V_{OUT(\Delta VINL)}$ | Transient Line Response | $V_{LDO2}$ +0.3 V < $V_{INL}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$, tr = 10 µs [1] | | 3 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $V_{INL}$ = $V_{LDO2}$ +0.3 V to 5.5 V, 1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ , tr = 10 µs, $V_{LDO2}$ = 3.3 V [1] | -3 | | 3 | % |
| PSRR | Power Supply Rejection ratio | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ [1] | | 40 | | dB |
| $V_{soft\_strup}$ | Soft-start slew rate | $I_{OUT}$ = 0 mA, 10 % to 90 % of $V_{LDO2}$ [1] | | 6.0 | | mV/µs |
| $V_{ov\_srtup}$ | Overshoot at startup | $I_{OUT}$ = 0 mA [1] | | | 20 | mV |
| $t_{EN}$ | Enable time | EN rising to 90 % of output voltage, $V_{LDO2}$ = 3.3 V [1] | | 800 | 1800 | µs |
| POK_90 | Output Power good | Percentage of $V_{LDO2}$ configuration | 86 | 90 | 94 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| $R_{DIS}$ | Active Discharge Resistance | | | 100 | 200 | Ω |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 2.2 | | 10 | µF |

[1] Not tested in production. Guaranteed by design

## 13.9 LDO3

**Table 180. LDO3 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | INL pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Regulator enabled, No load | | 0.23 | 0.5 | µA |
| $I_{OUT\_MAX}$ | Maximum Output DC Current | $V_{LDO3}$ = 3.3 V | 250 | | | mA |
| $I_{LIMIT}$ | Short Current Limit | Output shorted to GND | 260 | 310 | | mA |
| $V_{DO}$ | Dropout Voltage | $I_{OUT}$ = $I_{OUT\_MAX}$, $V_{INL}$ = 3.2 V, L3_OUT = 3.3 V | | 60 | 100 | mV |
| $V_{LDO3}$ | Nominal output voltage | $I^2C$ Programmable, 50mV/step | 0.8 | | 3.3 | V |
| | Default voltage | | | 3.3 | | V |
| | DC accuracy | $V_{LDO3}$ = 3.3 V, $I_{Load}$ = 5 mA | -2 | | 2 | % |

**Table 180. LDO3 description**...*continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{NOISE}$ | Output noise | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{MAX}$, $V_{LDO3}$ = 3.3 V [1] | | 170 | | µV |
| $\Delta V_{OUT(\Delta VINL)}$ | DC Line regulation | $V_{LDO3}$ +0.3 V < $V_{INL}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ | | 0.15 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | $V_{INL}$ = $V_{LDO3}$ +0.3 V to 5.5 V, 0.1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ | | 0.15 | | % |
| $\Delta V_{OUT(\Delta VINL)}$ | Transient Line Response | $V_{LDO3}$ +0.3 V < $V_{INL}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$, tr = 10 µs [1] | | 3 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $V_{INL}$ = $V_{LDO3}$ +0.3 V to 5.5 V, 1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ , tr = 10 µs, $V_{LDO3}$ = 3.3 V [1] | -3 | | 3 | % |
| PSRR | Power Supply Rejection ratio | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ [1] | | 40 | | dB |
| $V_{soft\_strup}$ | Soft-start slew rate | $I_{OUT}$ = 0 mA, 10 % to 90 % of $V_{LDO3}$ [1] | | 6.0 | | mV/µs |
| $V_{ov\_srtup}$ | Overshoot at startup | $I_{OUT}$ = 0 mA [1] | | | 20 | mV |
| $t_{EN}$ | Enable time | EN rising to 90 % of output voltage, $V_{LDO3}$ = 3.3 V [1] | | 800 | 1800 | µs |
| POK_90 | Output Power good | Percentage of $V_{LDO3}$ configuration | 86 | 90 | 94 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| $R_{DIS}$ | Active Discharge Resistance | | | 100 | 200 | Ω |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 2.2 | | 10 | µF |

[1] Not tested in production. Guaranteed by design

## 13.10 LDO4

**Table 181. LDO4 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | INL pin [1] | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent current | Regulator enabled, No load | | 0.23 | 0.5 | µA |
| $I_{OUT\_MAX}$ | Maximum Output DC Current | $V_{LDO4}$ = 1.8 V | 250 | | | mA |
| $I_{LIMIT}$ | Short Current Limit | Output shorted to GND | 260 | | | mA |
| $V_{DO}$ | Dropout Voltage | $I_{OUT}$ = $I_{OUT\_MAX}$, $V_{INL}$ = 3.2 V, L4_OUT = 3.3 V | | 60 | 100 | mV |
| $V_{LDO4}$ | Nominal output voltage | $I^2C$ Programmable, 50 mV/step | 0.8 | | 3.3 | V |
| | Default voltage | | | 1.8 | | V |
| | DC accuracy | $V_{LDO4}$ = 1.8 V, $I_{Load}$ = 5 mA | -2 | | 2 | % |
| $V_{NOISE}$ | Output noise | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{MAX}$, $V_{LDO4}$ = 1.8 V [1] | | 150 | | µV |

**Table 181. LDO4 description**...*continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{OUT(\Delta VINL)}$ | DC Line regulation | $V_{LDO4}$ +0.3 V < $V_{INL}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ | | 0.15 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | DC Load regulation | $V_{INL}$ = $V_{LDO4}$ +0.3 V to 5.5 V, 0.1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ | | 0.15 | | % |
| $\Delta V_{OUT(\Delta VINL)}$ | Transient Line Response | $V_{LDO4}$ +0.3 V < $V_{INL}$ < 5.5 V, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$, tr = 10 µs [1] | | 3 | | %/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Transient Load Response | $V_{INL}$ = $V_{LDO4}$ +0.3 V to 5.5 V, 1 mA < $I_{OUT}$ < $I_{OUT\_MAX}$ , tr = 10 µs, $V_{LDO4}$ = 1.8 V [1] | -3 | | 3 | % |
| PSRR | Power Supply Rejection ratio | f = 10 Hz to 10 KHz, $I_{OUT}$ = 10 % of $I_{OUT\_MAX}$ [1] | | 40 | | dB |
| $V_{soft\_strup}$ | Soft-start slew rate | $I_{OUT}$ = 0 mA, 10 % to 90 % of $V_{LDO4}$ [1] | | 6.0 | | mV/µs |
| $V_{ov\_srtup}$ | Overshoot at startup | $I_{OUT}$ = 0 mA [1] | | | 20 | mV |
| $t_{EN}$ | Enable time | EN rising to 90 % of output voltage, $V_{LDO4}$ = 1.8 V [1] | | 300 | 500 | µs |
| POK_90 | Output Power good | Percentage of $V_{LDO4}$ configuration | 86 | 90 | 94 | % |
| $t_{POK\_Deb}$ | POK debounce time | POK falling | | 300 | | µs |
| $R_{DIS}$ | Active Discharge Resistance | | | 100 | 200 | Ω |
| $C_{OUT}$ | Output capacitance | Minimum nominal capacitance [1] | 2.2 | | 10 | µF |

[1] Not tested in production. Guaranteed by design

## 13.11 LSW1

**Table 182. LSW1 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LSW1IN}$ = $V_{LSWW4IN}$ = 3.3 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{LSW1IN}$ | Input voltage range | LSW1IN pin [1] | 1.2 | | 5.5 | V |
| $I_Q$ | Quiescent current | Switch enabled, No load, $V_{LSW1IN}$ = 1.8 V | | 0.5 | 50 | nA |
| $I_{SHDN}$ | Shutdown current | $V_{LSW1IN}$ = 3.3 V | | 5 | 700 | nA |
| $R_{DSON}$ | Switch ON resistance | $V_{LSW1IN}$ = 1.8 V, $I_{LOAD}$ = 150 mA | | 150 | 220 | mΩ |
| $t_{EN}$ | Enable time | Time to LSW1OUT 10 % from EN, $V_{LSW1IN}$ = 1.8 V [1] | | 70 | 110 | µs |
| $t_{RAMP}$ | Output rise time | CL = 10 µF, $V_{SWIN}$ = 1.8 V, LSW1OUT 10 % to 90 % [1] | 6 | 12 | 18 | mV/us |
| $R_{DIS}$ | Active Discharge Resistance | Load switch is off | | 95 | 150 | Ω |

[1] Not tested in production. Guaranteed by design

## 13.12 LSW2

**Table 183. LSW2 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LSW1IN}$ = $V_{LSWW4IN}$ = 3.3 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VLSW1IN | Input voltage range | VLSW1IN pin [1] | 1.2 | | 5.5 | V |
| $I_Q$ | Quiescent current | Switch enabled, No load, $V_{LSW1IN}$ = 1.8 V | | 0.5 | 50 | nA |
| $I_{SHDN}$ | Shutdown current | $V_{LSW1IN}$ = 3.3 V | | 5 | 700 | nA |
| $R_{DSON}$ | Switch ON resistance | $V_{LSW1IN}$ = 1.8 V, $I_{LOAD}$ = 150 mA | | 150 | 220 | mΩ |
| $t_{EN}$ | Enable time | Time to LSW2OUT 10 % from EN, $V_{LSW1IN}$ = 1.8 V [1] | | 70 | 110 | µs |
| $t_{RAMP}$ | Output rise time | CL = 10 µF, $V_{SWIN}$ = 1.8 V, LSW2OUT 10 % to 90 % [1] | 6 | 12 | 18 | mV/us |
| $R_{DIS}$ | Active Discharge Resistance | Load switch is off | | 95 | 150 | Ω |

[1] Not tested in production. Guaranteed by design

## 13.13 LSW3

**Table 184. LSW3 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LSW1IN}$ = $V_{LSWW4IN}$ = 3.3 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VLSW1IN | Input voltage range | VLSW1IN pin [1] | 1.2 | | 5.5 | V |
| $I_Q$ | Quiescent current | Switch enabled, No load, $V_{LSW1IN}$ = 1.8 V | | 0.5 | 50 | nA |
| $I_{SHDN}$ | Shutdown current | $V_{LSW1IN}$ = 3.3 V | | 5 | 700 | nA |
| $R_{DSON}$ | Switch ON resistance | $V_{LSW1IN}$ = 1.8 V, $I_{LOAD}$ = 150 mA | | 150 | 220 | mΩ |
| $t_{EN}$ | Enable time | Time to LSW3OUT 10 % from EN, $V_{LSW1IN}$ = 1.8 V [1] | | 70 | 110 | µs |
| $t_{RAMP}$ | Output rise time | CL = 10 µF, $V_{SWIN}$ = 1.8 V, LSW3OUT 10 % to 90 % [1] | 6 | 12 | 18 | mV/us |
| $R_{DIS}$ | Active Discharge Resistance | Load switch is off | | 95 | 150 | Ω |

[1] Not tested in production. Guaranteed by design

## 13.14 LSW4

**Table 185. LSW4 description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LSW1IN}$ = $V_{LSWW4IN}$ = 3.3 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{LSW4IN}$ | Input voltage range | LSW4IN pin [1] | 1.2 | | 5.5 | V |

**Table 185. LSW4 description***...continued*

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LSW1IN}$ = $V_{LSWW4IN}$ = 3.3 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent current | Switch enabled, No load, $V_{LSW4IN}$ = 1.8 V | | 0.5 | 50 | nA |
| $I_{SHDN}$ | Shutdown current | $V_{LSW4IN}$ = 3.3 V | | 5 | 700 | nA |
| $R_{DSON}$ | Switch ON resistance | $V_{LSW4IN}$ = 1.8 V, $I_{LOAD}$ = 150 mA | | 150 | 220 | mΩ |
| $t_{EN}$ | Enable time | Time to LSW4OUT 10 % from EN, $V_{LSWxIN}$ = 1.8 V [1] | | 70 | 110 | µs |
| $t_{RAMP}$ | Output rise time | CL = 10 µF, $V_{LSW4IN}$ = 1.8 V, LSW4OUT 10 % to 90 % [1] | 6 | 12 | 18 | mV/us |
| $R_{DIS}$ | Active Discharge Resistance | Load switch is off | | 95 | 150 | Ω |

[1] Not tested in production. Guaranteed by design

## 13.15 LED driver (LED1/LED2/LED3/LED4)

**Table 186. LED driver (LED1/LED2/LED3/LED4) description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LSW1IN}$ = $V_{LSWW4IN}$ = 3.3 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{LEDIN}$ | Input voltage range | LSW1IN, LSW4IN pin [1] | 3.0 | | 5.5 | V |
| $I_Q$ | Quiescent current | $V_{LSW1IN}$ = $V_{LSW4IN}$ = 3.3 V, All LED channels are enabled, load = 0 mA | | 80 | 100 | µA |
| $I_{LED}$ | LED current range | Current programmable range | 0.625 | | 20 | mA |
| $I_{LED\_STEP}$ | LED current step | | | 0.625 | | mA |
| $V_{HR}$ | Headroom voltage | $V_{LEDIN}$ – $V_{LEDx}$ | | 168 | 200 | mV |
| $I_{LED\_ACC}$ | Current accuracy | $I_{LEDx}$ = 10 mA, $T_A$ = 25 °C | –1.5 | 0 | 1.5 | % |
| | | $I_{LEDx}$ = 10 mA, $T_A$ = -40 ~ 85 °C | -4 | 0 | 4 | % |
| $I_{LED\_MIS}$ | Current mismatch | $I_{LEDx}$ = 10 mA | -3 | 0 | 3 | % |
| $t_{ON}$ | LED ON time | BLINK Mode, LED_TON = 0x1 | 180 | 200 | 220 | ms |
| $t_{OFF}$ | LED OFF time | BLINK Mode, LED_TOFF = 0x1 | 180 | 200 | 220 | ms |
| $t_{RU}$ | LED Ramp Up time | BLINK Mode, P1_UP_STEP = 0x0, P1_UP_DLY = 0x0 | 470 | 523 | 575 | ms |
| $t_{RD}$ | LED Ramp Down time | BLINK Mode, P1_DN_STEP = 0x0, P1_DN_DLY = 0x0 | 470 | 523 | 575 | ms |

[1] Not tested in production. Guaranteed by design

## 13.16 I²C interface and logic I/O

**Table 187. I²C interface and logic I/O description**

*Unless otherwise specified, VSYS = 3.8 V, $V_{INB14}$ = $V_{INB23}$ = 3.8 V, $V_{INL}$ = 3.8 V, $V_{INL1}$ = $V_{BUCK4}$, $V_{LSW1IN}$ = $V_{LSWW4IN}$ = 3.3 V, $T_A$= –40 °C ~ +85 °C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SCL, SDA** | | | | | | |
| $f_{I^2C}$ | I²C Clock frequency | | — | — | 1 | MHz |
| $V_{IH}$ | High-level Input voltage | SCL, SDA; VSYS= 3.0 V to 5.5 V | 1.2 | — | — | V |
| $V_{IL}$ | Low-level Input voltage | SCL, SDA; VSYS= 3.0 V to 5.5 V | — | — | 0.4 | V |
| $V_{hys}$ | Hysteresis of Schmitt trigger inputs | | 0.01 | — | — | V |
| $V_{OL}$ | Low-level output voltage | SDA, Iload = 20 mA, VSYS = 3.0 V to 5.5 V | 0 | — | 0.4 | V |
| $t_{HD,STA}$ | Hold time (repeated) START condition | Fast mode plus; After this period, the first clock pulse is generated [1] | 0.26 | — | — | µs |
| $t_{LOW}$ | LOW period of I²C clock | Fast mode plus [1] | 0.5 | — | — | µs |
| $t_{HIGH}$ | HIGH period of I²C clock | Fast mode plus [1] | 0.26 | — | — | µs |
| $t_{SU,STA}$ | Setup time (repeated) START condition | Fast mode plus [1] | 0.26 | — | — | µs |
| $t_{HD,DAT}$ | Data Hold time | Fast mode plus [1] | 0 | — | — | µs |
| $t_{SU,DAT}$ | Data Setup time | Fast mode plus [1] | 50 | — | — | ns |
| $t_r$ | Rise time of I2C_SCL and I2C_SDA signals | Fast mode plus [1] | — | — | 120 | ns |
| $t_f$ | Fall time of I2C_SCL and I2C_SDA signals | Fast mode plus [1] | — | — | 120 | ns |
| $t_{SU,STO}$ | Setup time for STOP condition | Fast mode plus [1] | 0.26 | — | — | µs |
| $t_{BUF}$ | Bus free time between STOP and START condition | Fast mode plus [1] | 0.5 | — | — | µs |
| $t_{VD,DAT}$ | Data valid time | Fast mode plus [1] | | — | 0.45 | µs |
| $t_{VD,ACK}$ | Data valid acknowledge time | Fast mode plus [1] | | — | 0.45 | µs |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by input filter | [1] | 0 | — | 50 | ns |

[1] Not tested in production. Guaranteed by design

## 14 Package outline

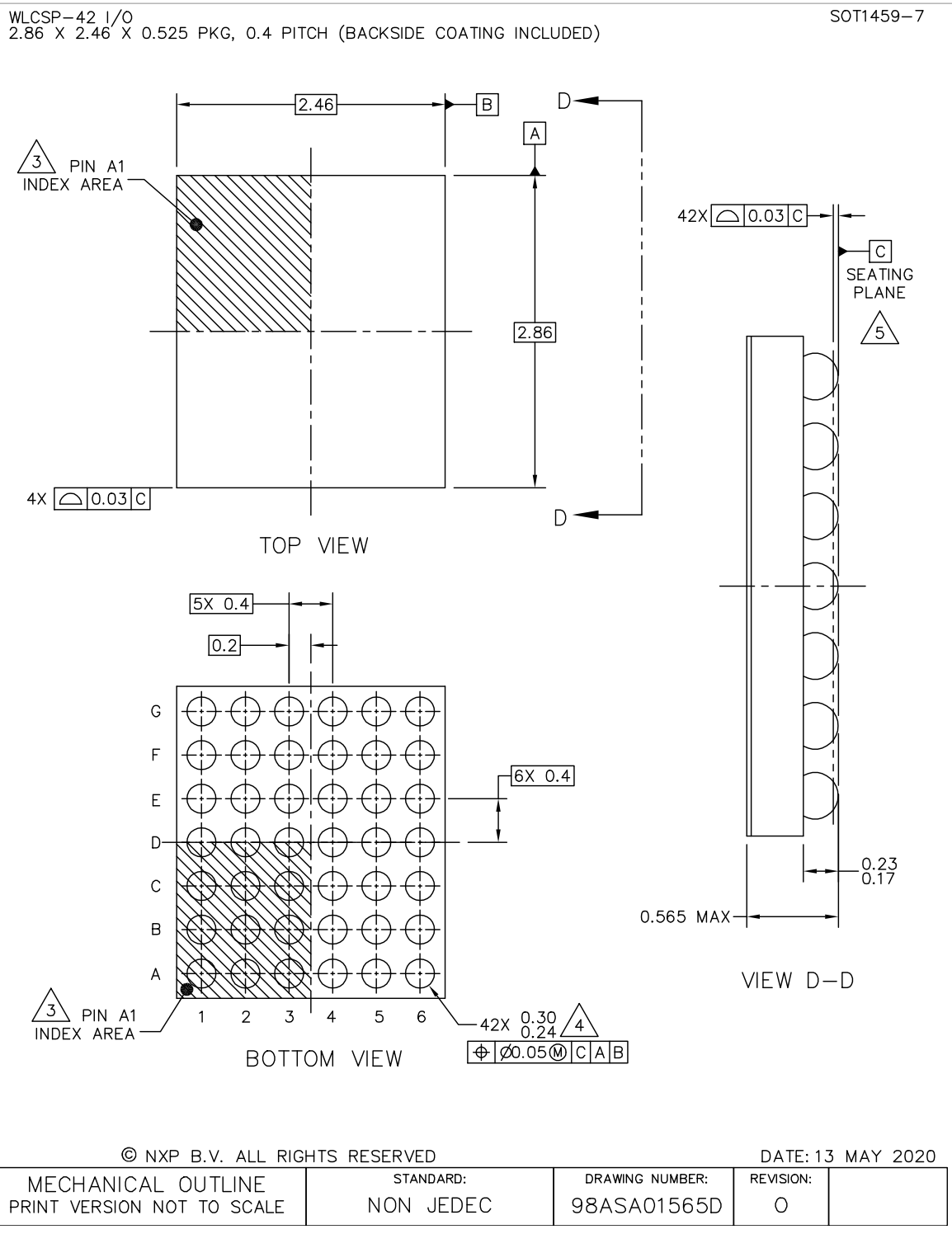
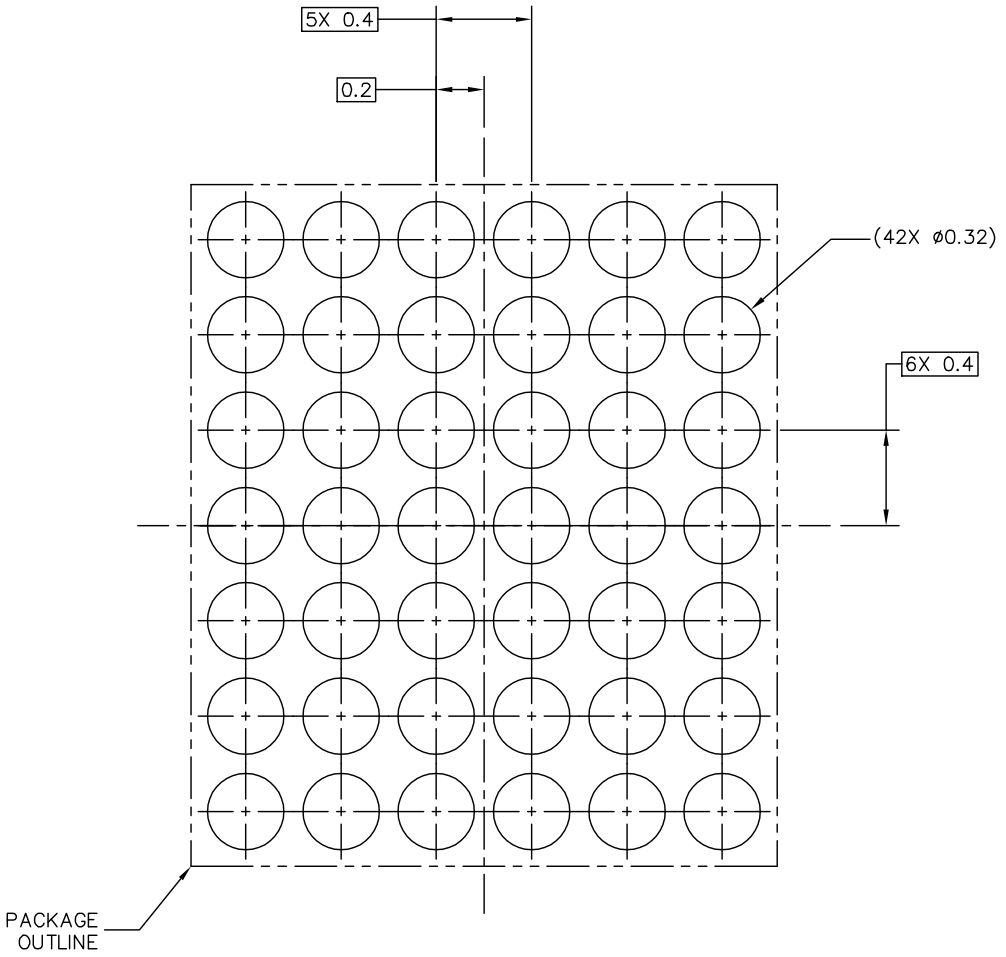



**Figure 26. Package outline WLCSP-42**

WLCSP−42 I/O
2.86 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459−7




PCB DESIGN GUIDELINES − SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



DATE: 13 MAY 2020

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01565D | REVISION:<br>O | |
|---|---|---|---|---|

**Figure 27. PCB Design Guidelines – Solder Mask Opening Pattern**

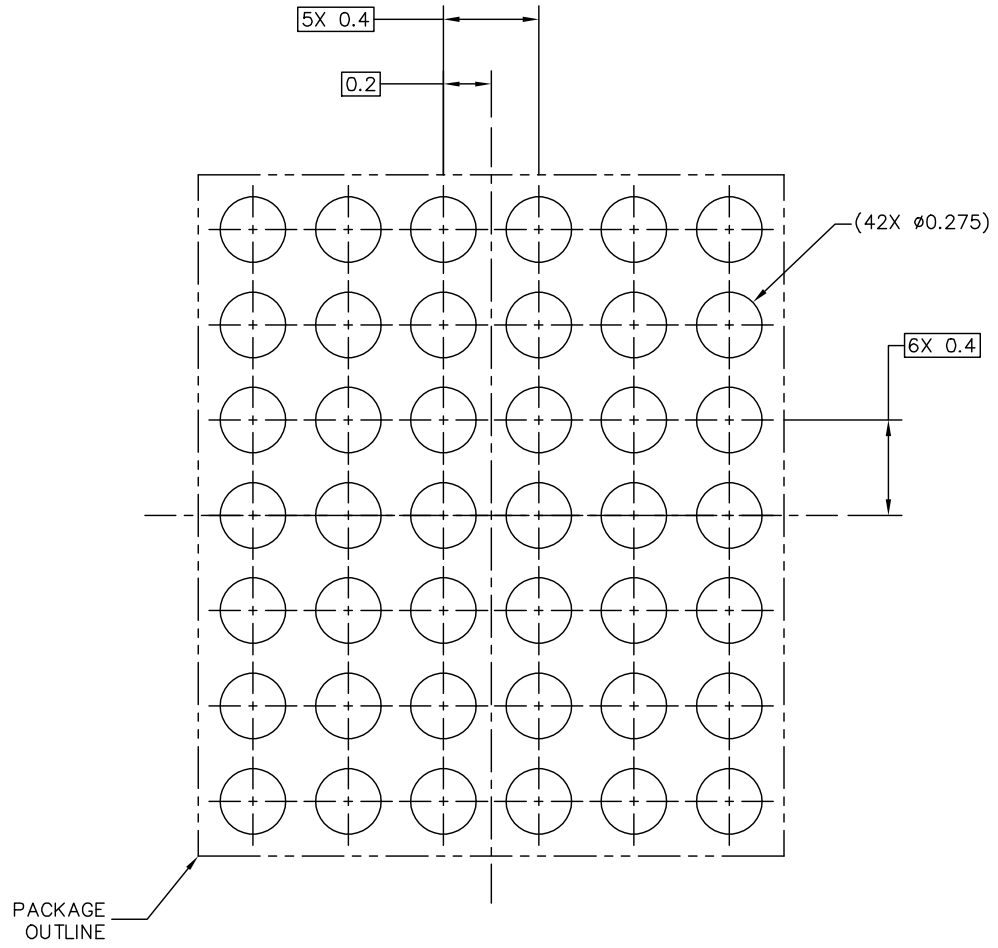



**Figure 28. PCB Design Guidelines – Solder Paste Stencil**

# 15 Revision history

**Table 188. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA9460 v.3.4 | 20240110 | Product data sheet | — | PCA9460 v. 3.3 |
| Modifications | • Table 169: Updated format of table; no change to min/max values<br>• Table 170: Added characteristics for $T_{stg}$; updated format of table; no change to min/max values | | | |
| PCA9460 v.3.3 | 20231006 | Product data sheet | — | PCA9460 v. 3.2 |
| PCA9460 v.3.2 | 20230901 | Product data sheet | — | PCA9460 v. 3.1 |
| PCA9460 v.3.1 | 20230217 | Product data sheet | — | PCA9460 v. 3.0 |
| PCA9460 v. 3.0 | 20221128 | Product data sheet | 202211037I | PCA9460 v. 2.0 |
| PCA9460 v. 2.0 | 20220309 | Product data sheet | — | PCA9460 v.1.0 |
| PCA9460 v.1.0 | 20210804 | Preliminary data sheet | — | — |

# Legal information

## Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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