AN14208

Migration Guide from MCXN to MCXA

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Document information

Information	Content
Keywords	AN14208, MCXN (N94x, N54x), MCXA (A143/2, A153/2)
Abstract	This document provides information required to migrate from MCXN (N94x, N54x) microcontrollers to MCXA (A143/2, A153/2) microcontrollers.

1 Introduction

This document provides information required to migrate from MCXN (N94x, N54x) microcontrollers to MCXA (A143/2, A153/2) microcontrollers. Migration between the two devices requires hardware and software changes. The following sections describe the changes required when migrating from MCXN to MCXA microcontrollers.

2 Part number selection

The MCXN series (N94x, N54x) MCU is an advanced MCU that offers extensive integration, including a 32-bit Arm Dual Cortex-M33, Neural Processor Unit, and up to 2 MB flash size. It is offered in two package options, which are 100HLQFP and 184MAPBGA.

On the other hand, the MCXA series (A143/2, A153/2) MCU focuses on the cost-effectiveness and ease of use. If you have already designed MCXN-based products and intend to migrate from MCXN to MCXA for cost reduction, you must select the right part number destination first.

To select the right MCU for your product, check the available device options. Currently, there are 12 MCXA part numbers available (see Table 1), with more MCXA parts to be released soon that will provide a lot of options in memory set and performance to address different customer needs. The advantage of those parts is that they are software compatible, pin compatible within the MCXA series. So, you can go to market with these 12 parts that are launched first, then you have the freedom to upgrade or downgrade within the whole MCXA series.

The following is a simple decoder, which can help you understand the three numbers that come after MCXA. The first number, which is 1, is considered the baseline and indicates cost-effectiveness. The second number indicates the core speed, where 4 stands for 48 MHz and 5 stands for 96 MHz. Finally, the third number indicates the memory size, where 2 represents 64 KB flash.

For the package of MCXA, you can choose from the following three packages: 64LQFP, 48HVQFN, and 32HVQFN.

Table 1. MCXA part number destination

Orderable part number[1]	Part number [2]	Embedded memory		Core Cortex-M33 (MHz)	Core cache (KB)	GPIO	Package	
		Flash (KB)	SRAM (KB)				Pin count	Type
MCXA143	MCXA143VLH	128	32	48	4	52	64	LQFP
MCXA143	MCXA143VFT	128	32	48	4	41	48	QFN
MCXA143	MCXA143VFM	128	32	48	4	26	32	QFN
MCXA142	MCXA142VLH	64	16	48	4	52	64	LQFP
MCXA142	MCXA142VFT	64	16	48	4	41	48	QFN
MCXA142	MCXA142VFM	64	16	48	4	26	32	QFN
MCXA153	MCXA153VLH	128	32	96	4	52	64	LQFP
MCXA153	MCXA153VFT	128	32	96	4	41	48	QFN
MCXA153	MCXA153VFM	128	32	96	4	26	32	QFN
MCXA152	MCXA152VLH	64	16	96	4	52	64	LQFP
MCXA152	MCXA152VFT	64	16	96	4	41	48	QFN
MCXA152	MCXA152VFM	64	16	96	4	26	32	QFN

[1] To confirm the current availability of orderable part numbers, visit https://www.nxp.com and perform a part number search.
[2] As marked on the package

Table 2. MCXN part number origin

Orderable part number[1]	Part number [2]	Embedded memory		Features			Package	
		Flash (MB)	SRAM (K)	Tamper pins (max)	GPIOs (max)	SRAM PUF	Pin count	Type
(P)MCXN547VNLT	(P)MCXN547VNLT	2	512	2	74	Y	100	HLQFP
(P)MCXN546VNLT	(P)MCXN546VNLT	1	352	2	74	Y	100	HLQFP
(P)MCXN547VDFT	(P)MCXN547VDFT	2	512	8	124	Y	184	VFBGA
(P)MCXN546VDFT	(P)MCXN546VDFT	1	352	8	124	Y	184	VFBGA
(P)MCXN947VDFT	(P)MCXN947VDFT	2	512	8	124	Y	184	VFBGA
(P)MCXN947VNLT	(P)MCXN947VNLT	2	512	2	78	Y	100	HLQFP
(P)MCXN946VNLT	(P)MCXN946VNLT	1	352	2	78	Y	100	HLQFP
(P)MCXN946VDFT	(P)MCXN946VDFT	1	352	8	124	Y	184	VFBGA

[1] To confirm the current availability of orderable part numbers, visit https://www.nxp.com and perform a part number search.
[2] As marked on the package

3 Feature comparison

This section provides a feature comparison between the MCXN and MCXA device.

3.1 High-level feature comparison

There are a significant number of differences between the two devices. However, a logical migration path exists between the two devices. The power management, system control architecture, and most of the peripherals on MCXA are reused from MCXN, providing exceptional continuity and compatibility across the devices. Table 3 outlines the system-level differences at a high level.

Table 3. High-level feature comparison between MCXA and MCXN

Module	MCXN	MCXA
Core	2x CM33F w TZ @ 150 MHz EZH, BSP32, PQ, Neutron, CoolFlux BSP32	CM33 @ 96 MHz w/o FPU MPU DSP
Clocking	2x PLL, FRO144M, FRO12M, OSC48M, OSC32K, FRO16K	FRO192M, FRO12M, OSC48M, FRO16K
Flash	2x 1 MB array, w RWW NPX(FMC+Prince), MSF	1x 128 KB array FMC, MSF
RAM	512 KB with 32 KB ECC, Configurable ECC 16 KB LPCAC, 16 KB FlexSPI Cache	32 KB with 8 KB ECC 4 KB LPCAC
ROM	256 KB Secure Boot, Secure Image Update, TP Flow	16 KB ROM Boot 24 KB flashloader
System	2x DMA3, CRC, 2x WWDT, SPC, SCG, EIM, ERM, INTM, EWM, SYSCON, WUU, CMC, VBAT	1x DMA3, CRC, WWDT, SPC, SCG, CMC, VBAT, EIM, ERM, SYSCON, WUU
Power supply	DCDC, SYS_LDO, CORE_LDO, VBAT, SRAM_LDO, SRPG, TRO 1.2 V / 1.1 V / 1.0 V RUN Mode	CORE_LDO, SRAM_RET_LDO 1.1 V / 1.0 V RUN Mode

Table 3. High-level feature comparison between MCXA and MCXN*...continued*

Module	MCXN	MCXA
Power modes	Active / Sleep / Deep Sleep / Power Down/Deep Power Down / VBAT	Active / Sleep / Deep Sleep / Power Down / Deep Power Down
High-speed interface	USB HS, FlexSPI, SDHC, ENET, eSPI, SPI-filter LPSPI (LP_FlexCOMM)	LPSPI
Communications	USB FS, 10x LP_FLEXCOMM, 2x FlexCAN, 2x SAI, 2x I3C, FlexIO, 2x EMVSIM	3x LPUART, 2x LPSPI, 1x LPI2C, 1x I3C
Timers	• 2x FlexPWM with four submodules each • 2x QDC (quadrature decoder) • 5x Ctimer (general-purpose timer) • 1x FREQME (frequency measurement timer) • 1x Micro-Tick timer • 1x OS event timer • 2x LPTMR (low-power timer) • 1x RTC (real-time clock) • 1x MRT (multirate timer) • 1x SCT	• 1x FlexPWM with three submodules • 1x QDC (quadrature decoder) • 3x CTimer (general-purpose timer) • 1x FREQME (frequency measurement timer) • 1x Micro-Tick timer • 1x OS Event timer • 1x LPTimer (low-power timer) • 1x Wake timer
Analog	2x 16 bit ADC, 3x DAC, 3x CMP, 3x OPAMP, VREF, TSI	1x 16 bit ADC, 2x CMP
IO	Up to 124 GPIO, 100M / 50M / 25M IO	Up to 52 GPIO, 50M / 25M IO High-drive IO, 5 V Tolerant IO
Security	S50, PKC, PUF, TRNG, SM3, 2x GDET, Tamper, eFuse, ITRC, 2x CDOG, LVD/HVD	LVD/HVD, ROP, 1x CDOG, GLIKEY
Package	184VFBGA 9 x 9 x 0.86 mm, 0.5 mm 100HLQFP 14 x 14 x 1.4 mm, 0.5 mm	64LQFP 10 x 10 x 1.4 mm, 0.5 mm 32QFN 5 x 5 x 0.9 mm, 0.5 mm 48QFN 7 x 7 x 0.9 mm, 0.5 mm

3.2 System module comparison

This section outlines the system module differences when migrating from the MCXN device to the MCXA device.

3.2.1 Memory map comparison

The memory map of the MCXA device is different from the MCXN device. It is important that you update your linker control file and do not try to use the MCXN device linker control file when compiling your MCXA project or vice versa. Table 4 is a side-by-side comparison of the two memory maps.

Table 4. Side-by-side comparison of the two memory maps

MCXN (Nonsecure)				MCXA			
Start address	End address	Size	Destination slave	Start address	End address	Size	Destination slave
0000_0000	001F_FFFF	2 MB	Program flash	0000_0000	0001_FFFF	128 KB	Program Flash
0300_0000	0303_FFFF	256 KB	ROM-BOOT	0300_0000	0300_3FFF	16 KB	ROM-BOOT
0400_0000	0401_7FFF	96 KB	RAMX	0400_0000	0400_1FFF	8 KB	RAM X0
0800_0000	0FFF_FFFF	128 MB	FlexSPI	0400_2000	0400_2FFF	4 KB	RAM X1

Table 4. Side-by-side comparison of the two memory maps*...continued*

MCXN (Nonsecure)				MCXA			
Start address	**End address**	**Size**	**Destination slave**	**Start address**	**End address**	**Size**	**Destination slave**
2000_0000	2000_7FFF	32 KB	RAMA	2000_0000	2000_1FFF	8 KB	RAM A0
2000_8000	2000_FFFF	32 KB	RAMB	2000_2000	2000_5FFF	16 KB	RAM A1
2001_0000	2001_FFFF	64 KB	RAMC	2000_6000	2000_7FFF	8 KB	RAM X0 Alias
2002_0000	2002_FFFF	64 KB	RAMD	-	-		-
2003_0000	2003_FFFF	64 KB	RAME	-	-		-
2004_0000	2004_FFFF	64 KB	RAMF	-	-		-
2005_0000	2005_FFFF	64 KB	RAMG	-	-		-
2006_0000	2006_7FFF	32 KB	RAMH	-	-		-

3.2.2 Internal flash memory feature comparison

MCXN embeds up to 2 MB of flash. It is implemented as 2 x 1 MB flash block instances.

MCXA embeds 128 KB of single-array flash, sector size of 8 Kbytes.

Table 5. Flash memory feature comparison

Feature	Description	MCXN	MCXA
Flash array - phrase	Represents the smallest portion of the flash memory that can be programmed in one operation	16 bytes	16 bytes
Flash array - sector	Represents the smallest portion of the flash memory that can be erased in one operation.	8 KB	8 KB
Flash array - page	Represents the largest portion of the flash memory that can be programmed in one operation.	128 bytes	128 bytes
Flash memory controller - prefetch buffer	Prefetch the next 128-bit flash memory location.	16 bytes	16 bytes
Flash memory controller - cache	Flash cache memory stores already fetched data. This code is immediately available for repeated execution without any wait states, if needed. It is a one-set, four-way associative cache with 128-bit (or 16-byte) size entries.	64 bytes	16 bytes
Functional safety - Flash ECC	-	One-bit error correction; Two-bits error detection capability	One-bit error correction; Two-bits error detection capability
Functional safety - Flash ERM	ERM provides information and optional interrupt	Report ECC two-bits error	Report ECC two-bits error

Table 5. Flash memory feature comparison*...continued*

Feature	Description	MCXN	MCXA
	notification on memory ECC and parity error events.		
Functional safety - Flash EIM	EIM provides a method for diagnostic coverage of internal memories. It enables you to induce artificial errors on error-checking mechanisms.	Single-bit error injection Double-bit error injection	Single-bit error injection Double-bit error injection
Flash performance - Access frequency	Configured by FCTRL[RWSC].	150 MHz / 4 = 37.5 MHz; when RWSC = 3	96 MHz SD mode, 3 wait states. 96 MHz / 3 = 32 MHz; when RWSC=2. 48 MHz, MD mode, 1 wait state. 48 MHz / 2= 24 MHz; when RWSC=1.

3.2.3 Clocking comparison

The system clocking module provides the clock signals to the core, memories, and peripherals (register interfaces and peripheral clocks).

MCXN system clock generation (SCG) module includes these clock sources:

- FRO high-speed output (fro_hf) from internal oscillator. By default, its speed is 48 MHz. fro_hf is the default main clock.
- 12 MHz free-running oscillator (FRO) output (FRO_12M) from internal oscillator.
- External oscillator.
- Output of PLL0.
- Output of PLL1.
- RTC 32 kHz oscillator.
- Output of USB PLL (usb_pll_clk).

MCXA system clock generation (SCG-Lite) is simplified, includes:

- FRO192M: FRO high-speed output (fro_hf) from internal oscillator. By default, its speed is 48 MHz. fro_hf is the default main clock.
- FRO12M: 12 MHz free-running oscillator (FRO) output (FRO_12M) from internal oscillator.
- FRO16K: 16.384 kHz clock output from FRO16K. It is the clock of peripherals in the VSYS domain.
- External oscillator, 8 MHz – 50 MHz.

It is important to note the differences in the clocking diagrams as these differences can significantly affect the setup of your application.

Figure 1 shows the MCXN clocking diagram and Figure 2 shows the MCXA clocking diagram.

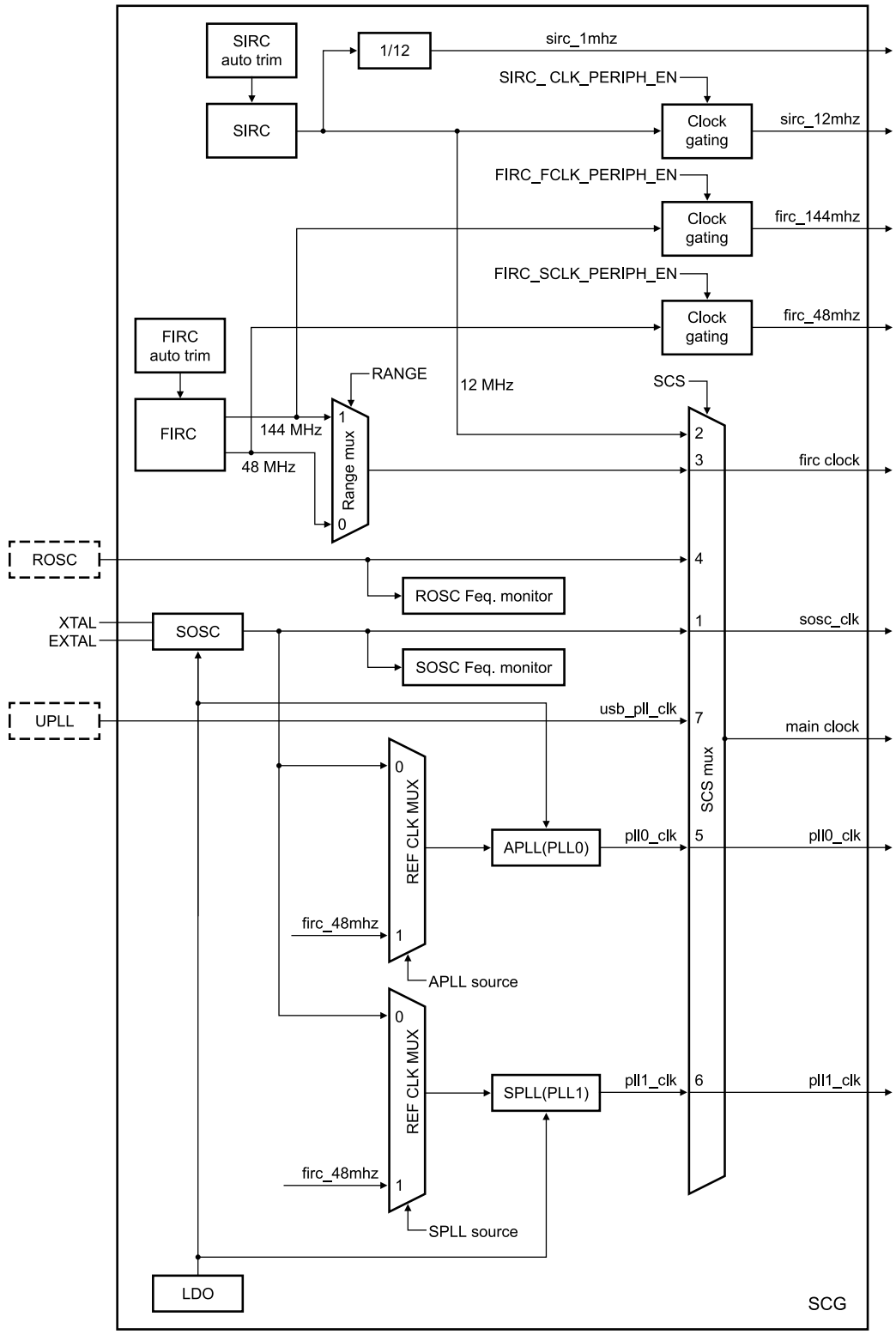

Figure 1. MCXN clocking block diagram

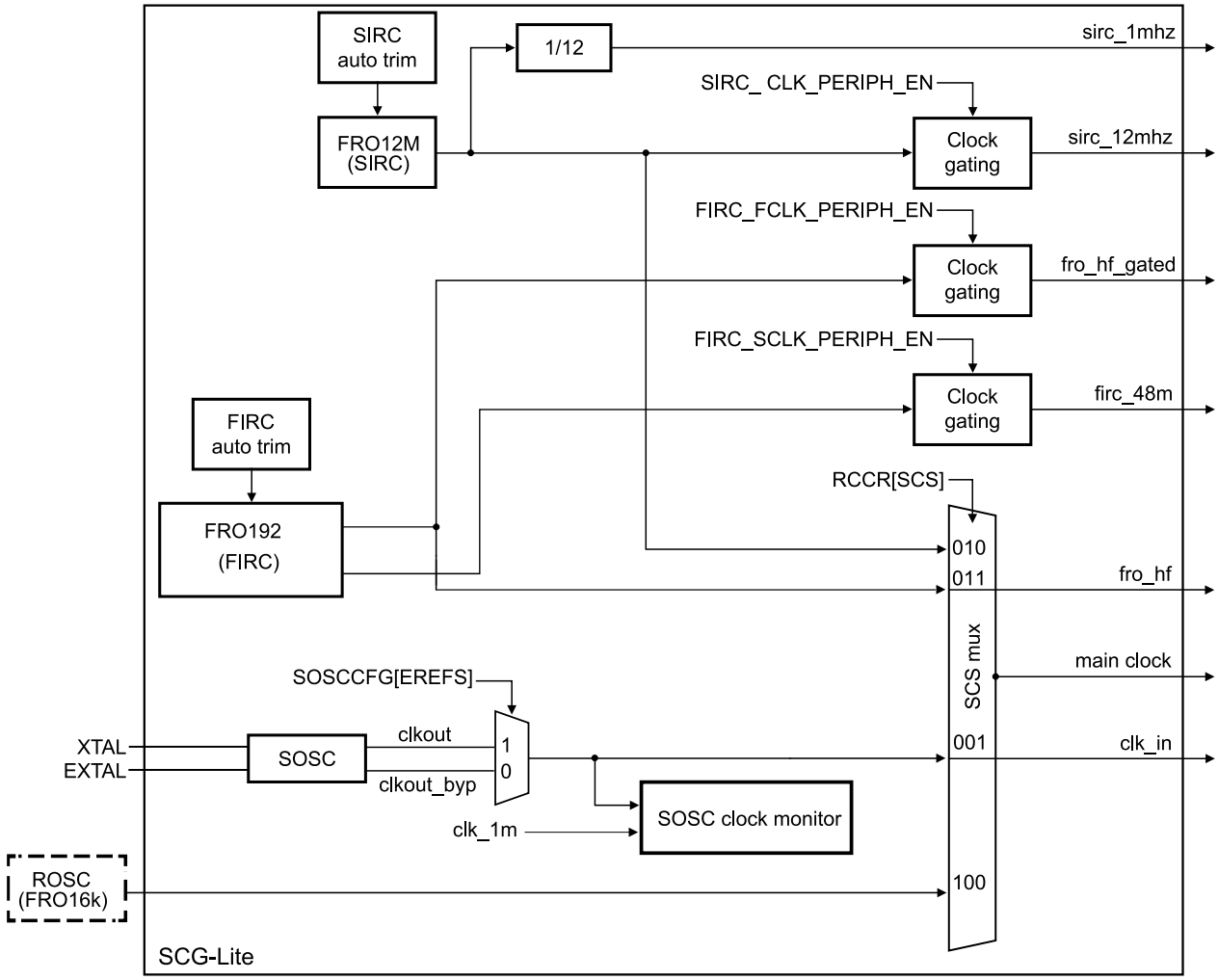

Figure 2. MCXA clocking block diagram

Table 6 outlines the clock module differences at a high level.

Table 6. Clock modules comparison

	MCXN	MCXA
Internal source	FRO144M	FRO192M
	FRO12M	FRO12M
	FRO16K	FRO16K
External clock	System crystal (16 MHz - 40 MHz)	System crystal (8 MHz - 50 MHz)
	32 K crystal	NA
PLL	550 MHz PLL0, PLL1	NA

Table 7 outlines system clock requirements differences.

Table 7. System clock requirement comparison

	MCXN			MCXA	
	Max. clock frequency			Max. clock frequency	
	Over Drive mode (VDD_CORE = 1.2 V)	Standard Drive mode (VDD_CORE = 1.1 V)	Mid Drive mode (VDD_CORE = 1.0 V)	Standard Drive mode (VDD_CORE = 1.1 V)	Mid Drive mode (VDD_CORE = 1.0 V)
CPU_CLK (Core clock)	150 MHz	100 MHz	50 MHz	96 MHz	48 MHz
SYSTEM_CLK (Peripheral Bus Clock 0)	150 MHz	100 MHz	50 MHz	96 MHz	48 MHz
SLOW_CLK (Peripheral Bus Clock 1)	37.5 MHz	25 MHz	12.5 MHz	24 MHz	12 MHz

3.3 Peripheral module comparison

The peripheral modules are classified.

The modules marked by **Unchanged** in the **Software driver comments** column of the peripheral module differences table (see Table 8) are compatible, and use the same SDK driver. Although the designs of these modules were not changed, there is a possibility that they have been integrated differently or that different clock sources are now sourcing these modules. Also, they may have different instances.

The modified modules refer to the modules that have been updated to use newer/different versions or simply have some minor differences. The overall functionality provided is similar. However, changes are required in software and possibly hardware changes are required to utilize updated features. These modules are marked by **Changed** in the **Software driver comments** column of the peripheral modules differences table (see Table 8).

The new modules refer to the new modules that have been added and how they can benefit your design. They are marked with **+** in the **Software driver comments** column of the peripheral module differences table (see Table 8).

Take a note of the removed modules. These modules are marked with **-** in the **Software driver comments** column of the peripheral module differences table (see Table 8). Unpredictable results occur if a module that is present on the MCXN is written on the MCXA. If your application is using a removed module, you should remove the code for this peripheral.

Table 8 presents a comparison of the peripheral modules found on the MCXN device and the MCXA device.

Table 8. Peripheral module comparison

Peripheral	MCXN	MCXA	Software driver comments
Serial communication interfaces	10x LP_FLEXCOMM	2x LPSPI, 3x LPUART, LPI2C	Unchanged. LPSPI / LPUART / LPI2C are compatible with LP_Flexcomm
I3C	2x	1x	Unchanged.
Full-speed USB	1x	1x	Changed. MCXA FS USB does not support USB DCD.
High-speed USB	1x	-	-
High-speed Interface	FlexSPI, SDHC, ENET, eSPI	-	-
CAN	2x FlexCAN	-	-
Audio	2x SAI	-	-

Table 8. Peripheral module comparison*...continued*

Peripheral	MCXN	MCXA	Software driver comments
FlexPWM	2x	1x	Unchanged 3 Sub Modules in FlexPWM of MCXA
Quadrature decoder	2x ENC	1x QDC	Changed. QDC is a new design, but mostly compatible with MCXN ENC
CTimer	5x CTimer	3x CTimer	Unchanged
SCTimer	1x	-	-
Micro-tick timer (UTICK)	1x	1x	Unchanged
OS Timer	1x	1x	Unchanged
Frequency measurement (FREQME)	1x	1x	Unchanged
RTC	1x	-	-
LPTIMER	2x	1x	Unchanged
Multi-rate timer (MRT)	1x	-	-
ADC	2x 16 bit ADC	1x 16 bit ADC	Changed. The ADC on MCXA features a single-ended configuration, with a single sample/hold circuit. Supports up to 3.2 Msps in 16-bit mode. MCXA ADC supports seven CMDs, one 8-entry conversion result FIFO; MCXN ADC supports 15 CMDs, two 16-entry conversion result FIFO.
CMP	3x	2x	Unchanged.
DAC	3x	-	-
OPAMP	3x	-	-
VREF	1x	-	-
TSI	1x	-	-
PORT	6x	4x	Changed. MCXN each port has the independent power supply VDD_Px. MCXA all ports have the same power supply VDD.
GPIO	6x	4x	Changed. MCXA added high drive and 5 V tolerant IOs

4 Hardware comparison

This section outlines the differences and hardware considerations when migrating from the MCXN device to the MCXA device.

4.1 Package / pinout differences

The MCXN device is offered in two package options, which are 100HLQFP and 184MAPBGA. On the other hand, the MCXA device is available in three packages, which are 64LQFP, 48HVQFN, and 32HVQN. These devices are not designed to be pin-to-pin compatible. You can find the package drawing in the Device data sheet.

4.2 Minimum system considerations

There are some additional hardware considerations when migrating from MCXN to MCXA.

Figure 3 shows the MCXA minimum system.

The MCXN and MCXA devices have the similar reset, ISP, and debug circuit for the minimum system. However, MCXA integrates a simple capless LDO to power the core in a power supply circuit, while MCXN offers an additional DCDC converter with better power efficiency. Furthermore, MCXA does not have the external 32 K crystal circuit.

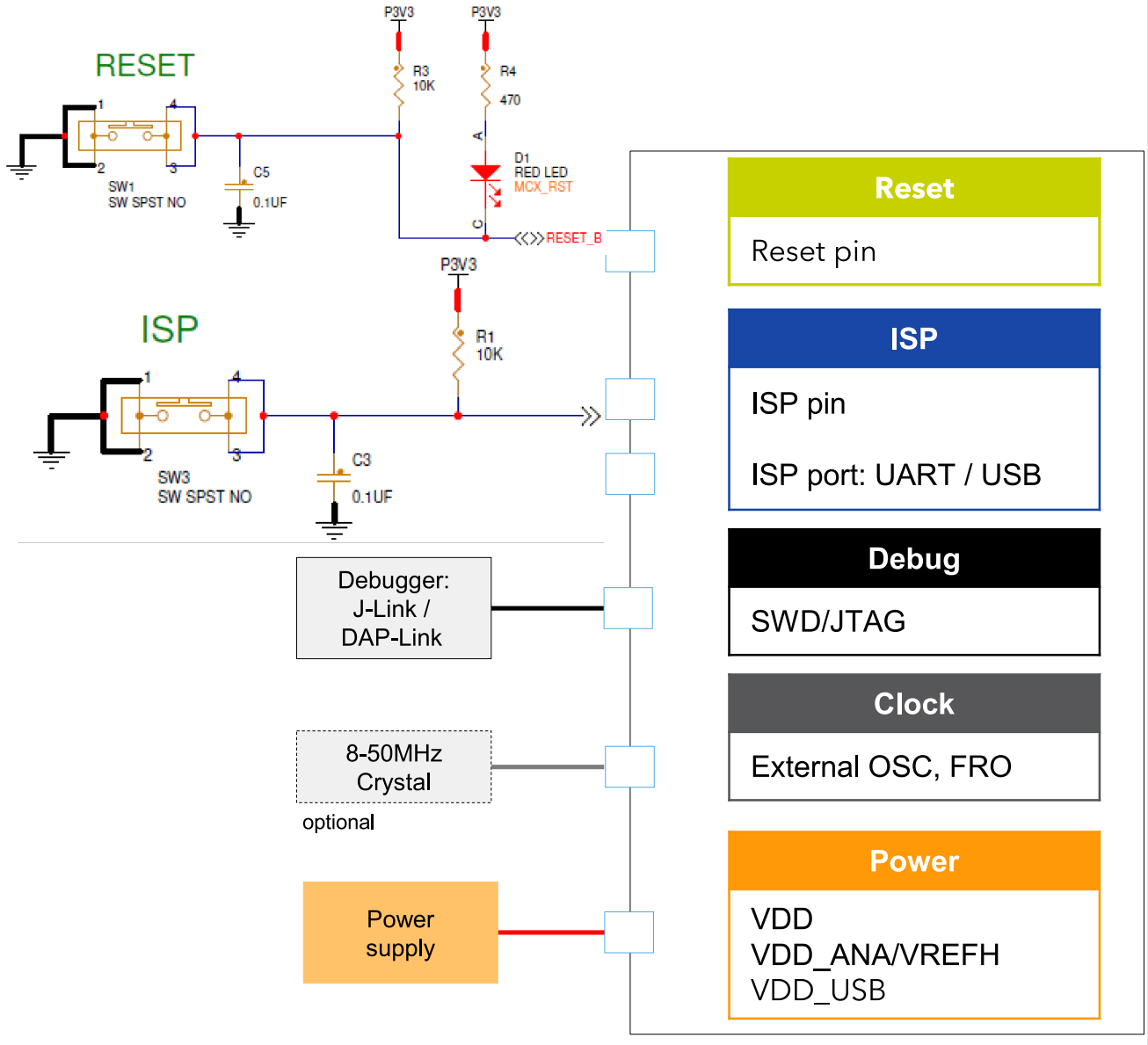

Figure 3. MCXA minimum system block diagram

5 Revision history

Table 9 summarizes revisions to this document.

Table 9. Revision history

Document ID	Release date	Description
AN14208 v.1	18 March 2024	Initial public release

Contents

For more information, please visit: https://www.nxp.com

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