AN13592

Application Hints for i.MX RT1040 and i.MX RT1060X

Rev. 1 — 19 October 2022 Application note

Document information

Information	Content
Keywords	RT1060X, FlexSPI, 125C
Abstract	This document focuses on the differences between i.MX RT1040 and i.MX RT1050, and between i.MX RT1060 and i.MX RT1060X. At the same time, it adds some application key points.

1 Introduction

i.MX RT1040 and i.MX RT1060X are new members of i.MX RT family. They feature advanced implementation of the Arm Cortex-M7 core of NXP by extending industrial qual to Tj 125C. To provide high CPU performance and also best real-time response, it retains operation at the speed up to 600 MHz for commercial qual spec and 528 MHz for extended industrial qual spec.

In addition, the new number provides more package options. For details, see the package section in Datasheet.

This document focuses on the differences between i.MX RT1040 and i.MX RT1050, and between i.MX RT1060 and i.MX RT1060X. At the same time, it adds some application key points.

2 Comparison between i.MX RT1040 and i.MX RT1050

Table 1 lists the key differences between i.MX RT1040 and i.MX RT1050. In conclusion, i.MX RT1040 reduces a few features but provides higher Tj and one more FlexSPI interface.

Table 1. Comparison between i.MX RT1040 and i.MX RT1050

	i.MX RT1040	i.MX RT1050
GPIO number	108	124
CAN-FD	Y	—
CSI	—	Y
KPP	—	Y
CCM_CLK1_P/N	—	Y
ACMP Output pin	—	Y
FlexSPI	2	1
LPSPI	3	4
Tj (industrial)	125℃	105℃
Package	BGA169	BGA196

3 i.MX RT1040 lower cost board design

i.MX RT1040 optimized ball map with MAPBGA169, 0.8 mm pitch and 11 × 11 mm mechanical package. To save board cost by enabling two-layer PCB designs, pay attention to below design points.

1. The signals of first two rows can fan out on the top layer directly. Other signals can fan out using vias on the bottom layer. Power and ground pin is distributed in the third row. It can fan out directly using a via hole on the bottom layer, as shown in Figure 1.

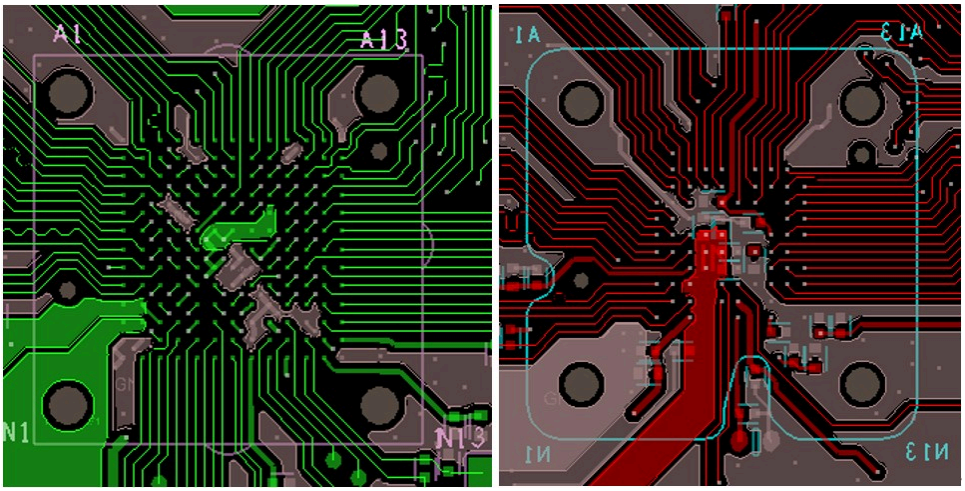

Figure 1. Top and bottom layer of RT1040-EVK

2. USB signal pins are placed in the first row and routed to connector. Keep `USB_P/N` connected directly, no layer changed. The default impedance of the differential pair is 90 Ω.
3. The clock of 24 MHz and 32.768 KHz is placed in the first row, connected to crystal with shorter trace length.
4. The pitch between pins on the package is 0.8 mm, so vias can be a regular plating hole, 18-mil circle pad and 8-mil drill hole, meeting the capabilities/requirements of all PCB manufacturers.
5. The impedance requirement is difficult to control for a two-layer board. To ensure sufficient impedance, place serial resistors and shorter trace stubs for high-speed signals. The resistor values can be adjusted according to the EMC test results. For example, use 47 Ω serial resistors for SDRAM signals.
6. Most devices are placed on the top layer, and the bottom layer is used as ground reference layer. It must be GND copper shape as much as possible. Especially between the chip and power supply, sufficient ground return path is required.
7. Place layer changes for clocks and sensitive signals near to a ground via or decoupling capacitor.

4 Comparison between i.MX RT1060 and i.MX RT1060X

Figure 1 lists the key differences between i.MX RT1060X and i.MX RT1060. In conclusion, compared to i.MX RT1060, i.MX RT1060X has a FlexSPI2 dedicated interface, more GPIO pins, and higher Tj.

Table 2. Comparison between i.MX RT1060 and i.MX RT1060X

	i.MX RT1060	i.MX RT1060X
FlexSPI2 dedicated interface	—	Y
GPIO number	124	146
Tj (industrial)	105 ℃	125 ℃
Package	BGA 196	BGA 225

5 More GPIOs of i.MX RT1060X

i.MX RT1060X has an additional 22 GPIOs when compared to i.MX RT1060 (added to GPIO10), providing more flexibility for system designs. Those added GPIOs can also be configured as FlexSPI function to interface with different memories. These additional GPIO signal locations are show in Figure 2.

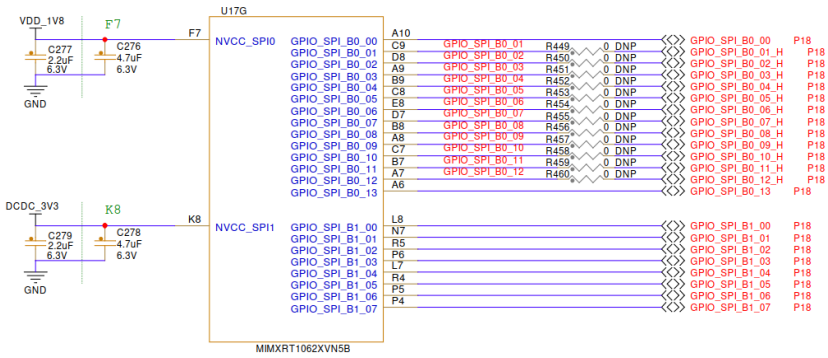

Figure 2. More GPIOs of i.MX RT1062X

6 FlexSPI2 in i.MX RT1060X

The FlexSPI2 module in i.MX RT1060X parts includes two ports, **Port A** and **Port B**. Each port can operate in quad mode up to 133 MHz. To support Octal devices or HyperBus devices, **Port A** and **Port B** can be combined.

Note:

Port A *of FlexSPI2 can work up to 166 MHz but* ***Port B*** *of FlexSPI2 can only work up to 133 MHz.*

To use Octal devices or HyperBus devices at a higher frequency than 133 MHz, use FlexSPI1. Details of the FlexSPI2 ports are shown in Figure 3.

Note: *To boot from FlexSPI2, set* ***fuse0x6d0[20]*** *to* ***1****.*

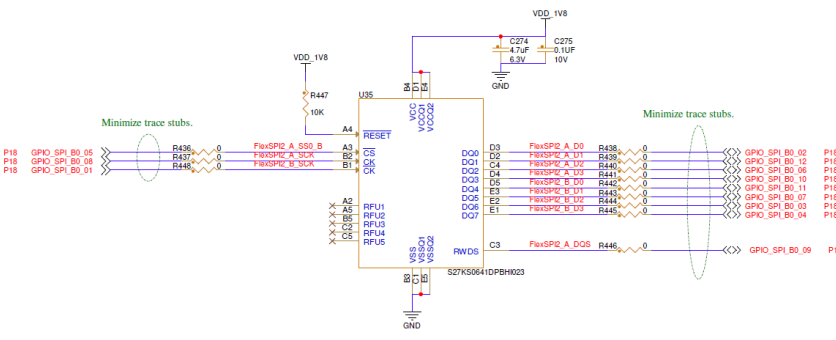

Figure 3. FlexSPI2 extension of i.MX RT1060X

7 Use case comparison between RT1060 and RT1060x

- i.MX RT1060 family expansion – FLEXSPI USE CASE example 1
  - **i.MX RT1060 (BGA196)** is limited to use XIP flash through gpio_sd_xx (FlexSPI1) and **ONLY extend 133 MHz HyperRAM** through gpio_semc_xx (FlexSPI2) because it cannot boot using FlexSPI through gpio_semc_xx.
    Note: *To boot from FlexSPI2, set* ***fuse0x6d0[20]*** *to* ***1****.*

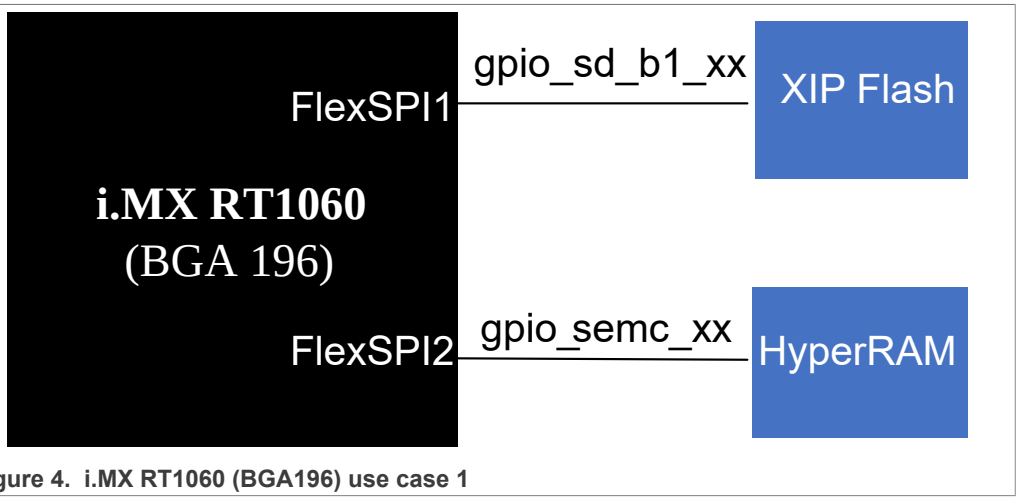

Figure 4. i.MX RT1060 (BGA196) use case 1

  - **i.MX RT1060 (BGA225)** provides option to **use 166 MHz HyperRAM** through gpio_sd_xx (FlexSPI1) and XIP flash through the added gpio_spi_xx (FlexSPI2).

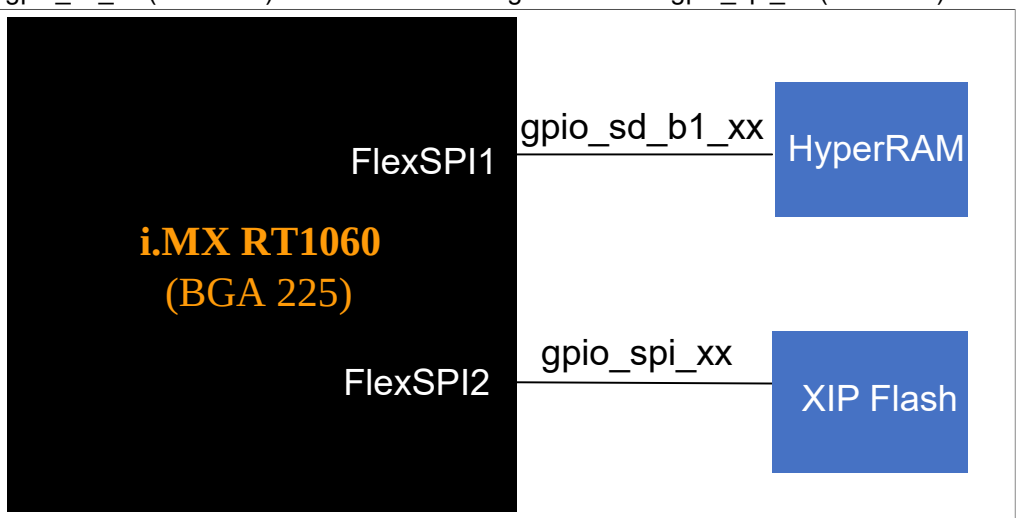

Figure 5. i.MX RT1060 (BGA225) use case 1

- i.MX RT1060 family expansion – flexspi USE CASE example 2
  - **i.MX RT1060 (BGA196)** is limited to use XIP flash through gpio_sd_b1_xx (FlexSPI1) and **can ONLY extend one** SD/SDIO device because SDHC2 PINMUX is multiplexed with FlexSPI1.

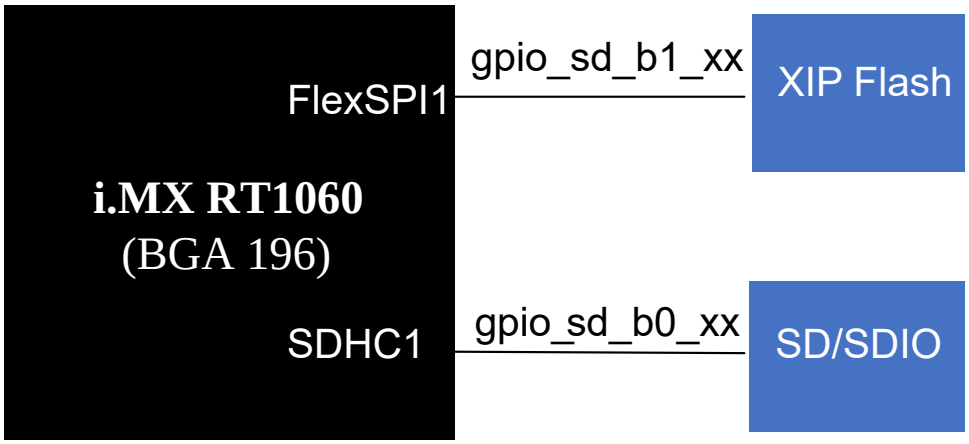

Figure 6. i.MX RT1060 (BGA196) use case 2

– **i.MX RT1060 (BGA225)** provides option to use XIP Flash through added gpio_spi_xx (FlexSPI2) and can **extend two** SD cards/SDIO devices.

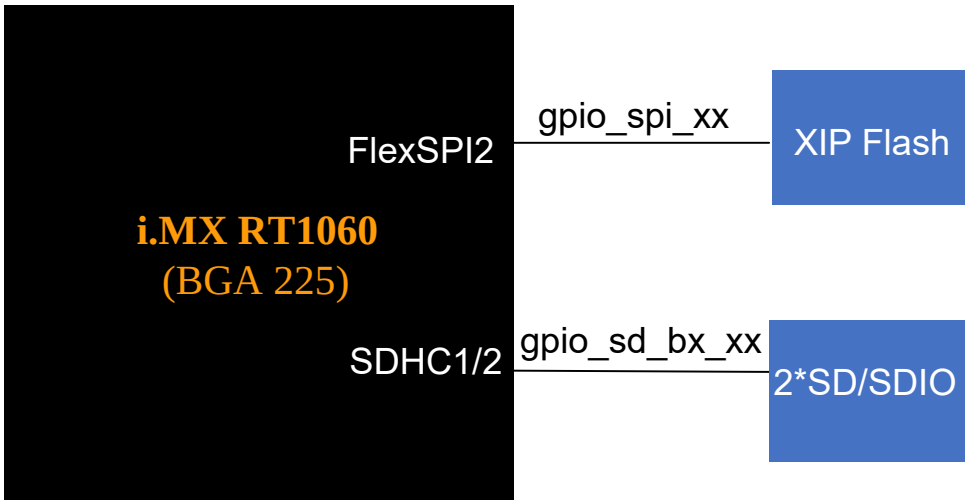

Figure 7. i.MX RT1060 (BGA225) use case 2

8 Revision history

Rev.	Date	Description
1	19 October 2022	• Updated Table 1 • Added a note in Section 6 • Added a note in Section 7
0	11 March 2022	Initial release

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