AN12581

2-layer PCB Layer Design Guide for VFBGA98 Package

Rev. 0 — 10/2019 Application Note

Contents

1 Purpose

The LPC5500 series support VFBGA98 package.

Usually, to route the function pins of LPC5500 in VFBGA98 package, the hardware enginners use a 4-layer for PCB layout. However, to reduce the PCB cost, customers may use a 2-layer PCB to route VFBGA98. This application note introduces two solutions for LPC5500 VFBGA98 layout on 2-layer PCB.

2 LPC5500 VFBGA98 package information

2.1 Overview

VFBGA98(SOT1982-1) is a friendly package with very thin fine-pitch ball grid array. It contains 98 terminals, a pitch of 0.5 mm, and a body of 7 mm × 7mm body. Table 1 describes the package summary.

Table 1. VFBGA98 package summary

Parameter	Min.	Normal	Max.	Unit
Package length	—	7	—	mm
Package width	—	7	—	mm
Package height	—	0.86	—	mm
Nominal pitch	—	0.5	—	mm
Actual quantity of termination	—	98	—	

2.2 Pads diameter information

Figure 1 shows the ouline information of the VFBGA98 package. As shown in Figure 1, the key parameter is the pad's diameter, and for VFBGA98, it is 0.25 - 0.35 mm.

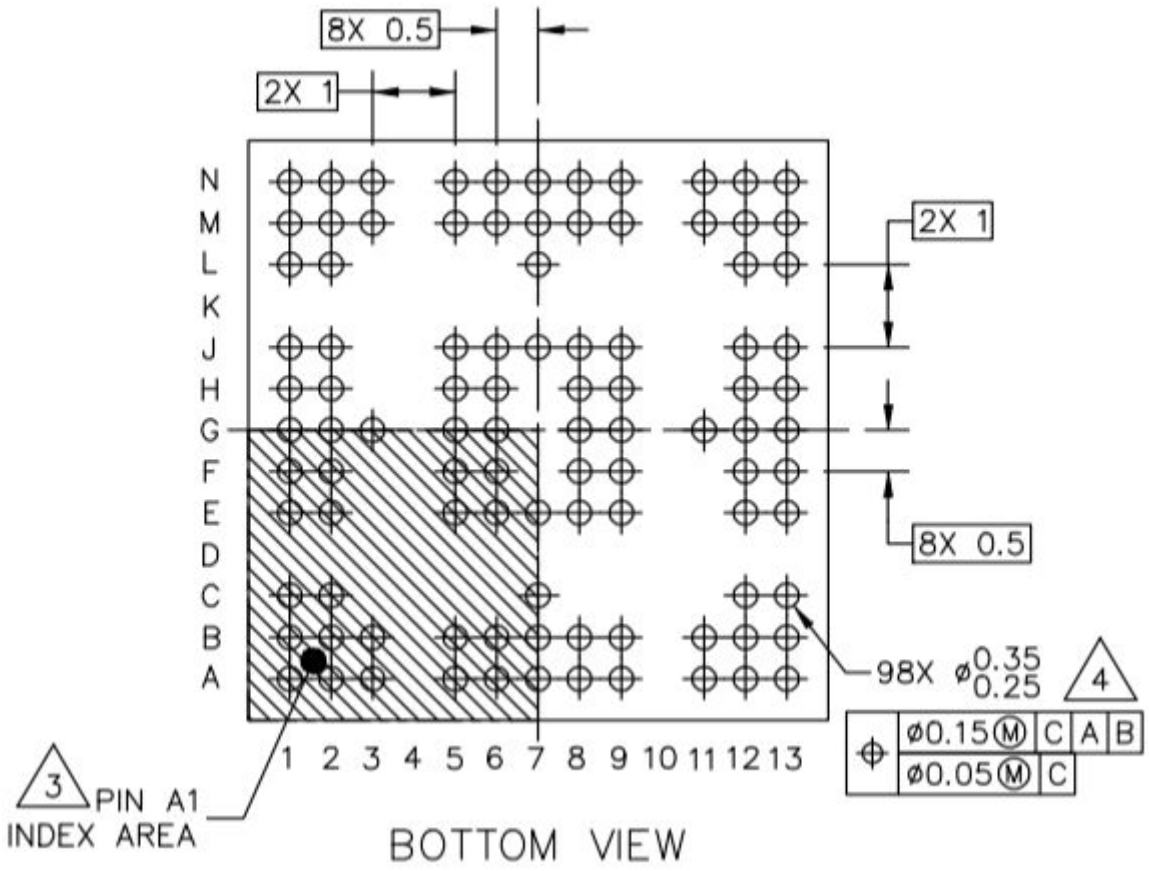

Figure 1. VFBGA98 package outline infomration

2.3 Reflow soldering footprint

In the VFBGA98 (SOT1982-1), two kinds of reflow soldering footprint are provided for the use of 4-layer PCB, as shown in Figure 2 and Figure 3. For details, see *LPC55S6x product data sheet* (document LPC55S6x).

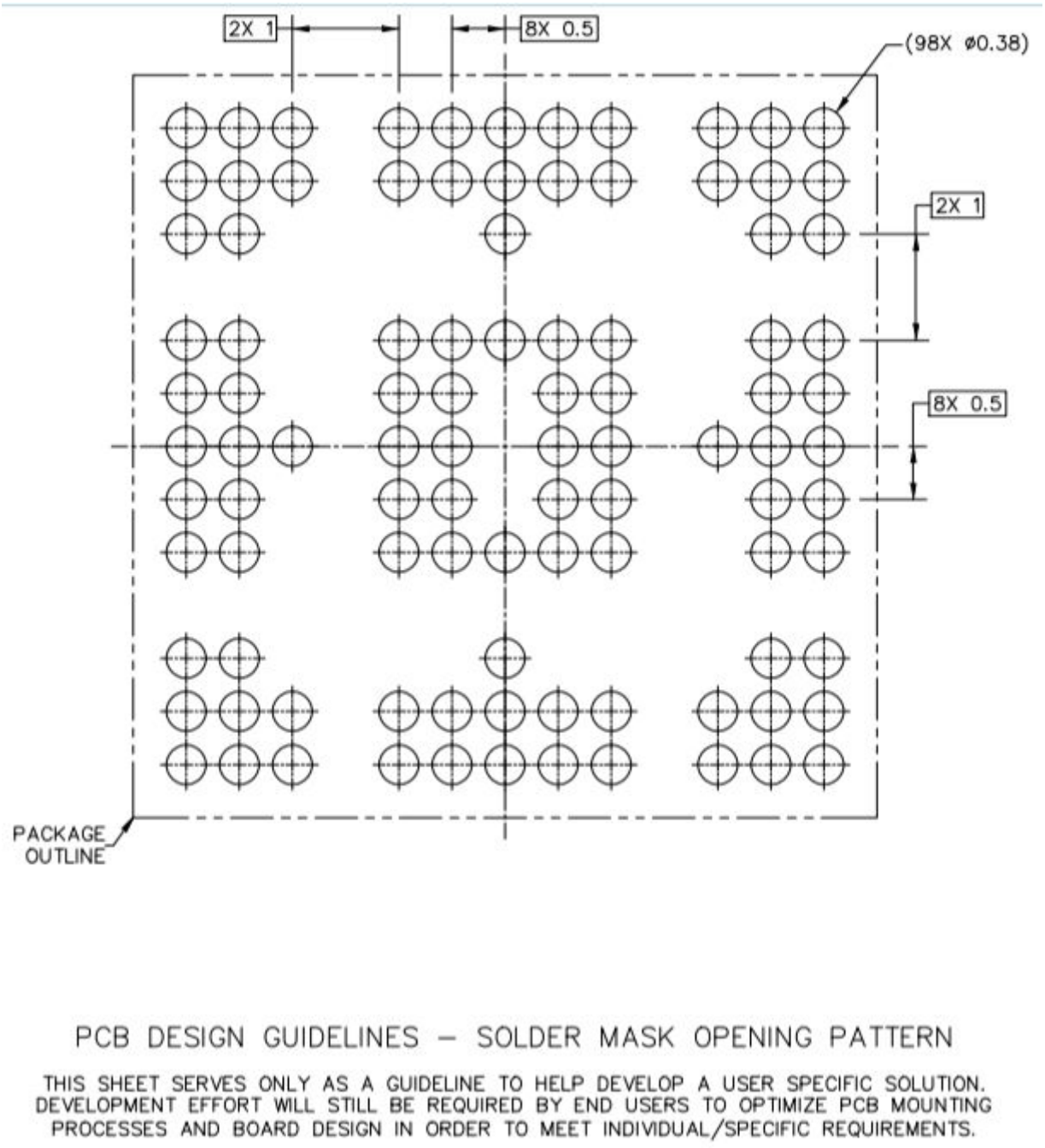

Figure 2. Reflow soldering footprint part1 for VFBGA98 (SOT1982-1)

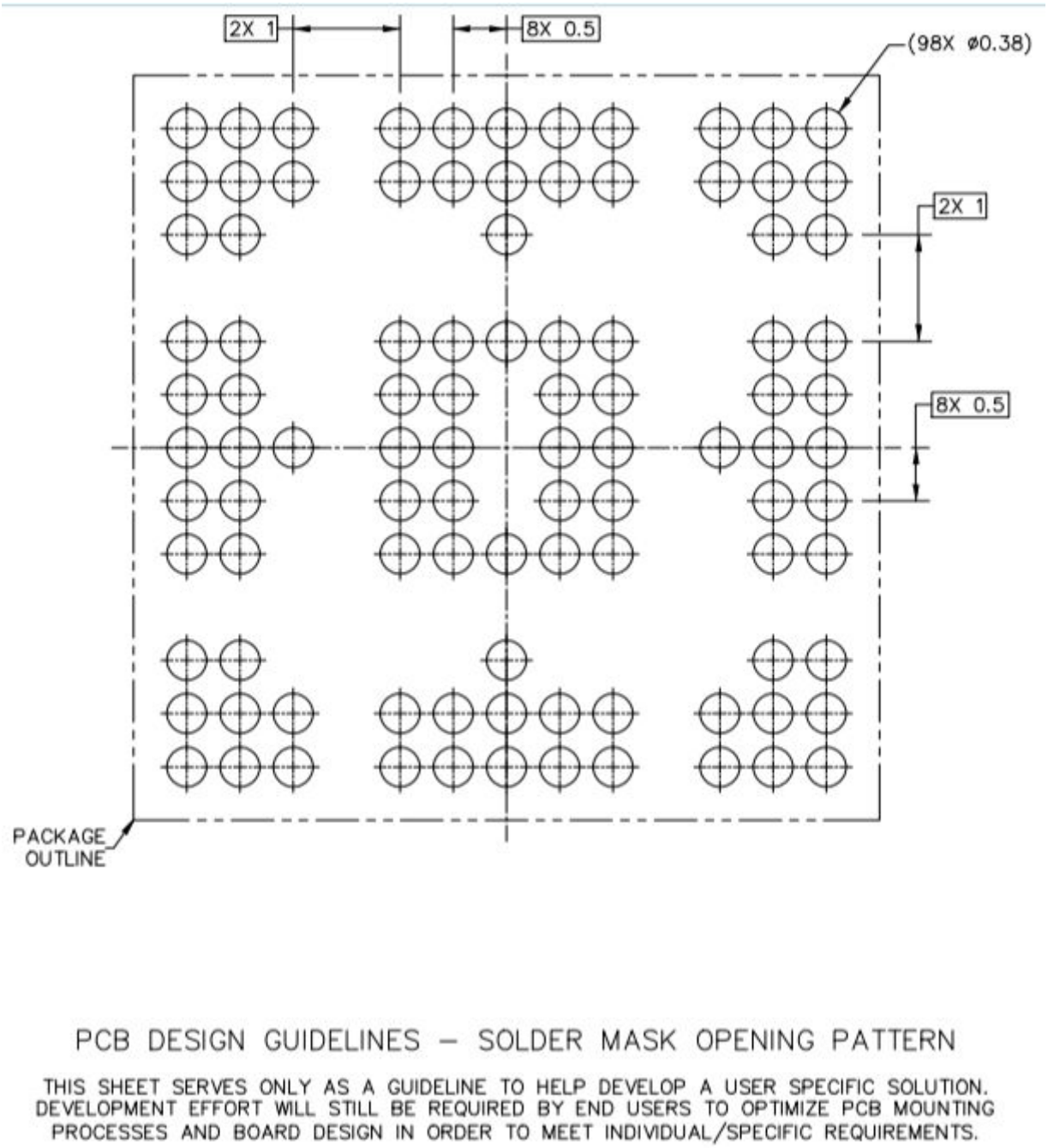

Figure 3. Reflow soldering footprint part2 for VFBGA98 (SOT1982-1)

3 Solutions for 2-layer PCB layout

Usually, the limitation of the PCB vendor's process is 3 mils (0.77 mm) for line/space width. The ultra-low cost PCB process limitation is 5 mils (0.127 mm). This document introduces two kinds of layout rules:

- **3.2 mils version**: It can help to draw out all VFBGA98 functional pins.
- **5 mils version**: It can extract up-to 37-38 function pins (including one high-speed USB pin, two external crystal pins, and two SWD pins).

3.1 3.2 mils line/space limitation

The required trace width of the 3.2 mils layout version is 3.2 mils, and the clearance is also 3.2 mils. Table 2 describes the layout rules.

Table 2. Layout rules for 3.2 mils version

VFBGA98 Pad diameter	10 mils (0.254 mm)	
Net rules	**Default/Neck down**	**Power/GND**
Trace width	4 mils/3.2 mils	8 mils (min.)
Trace to Trace	3.2 mils	3.2 mils (min.)
Trace to Pad	3.2 mils	3.2 mils (min.)
Trace to Via	4 mils	4 mils
Through Via	8 mil drill & 18 mil pad	
Layers	2-layer (Top & Bottom)	

The key rule is the pad diameter. The suggested pad diameter is 15 mils (0.38 mm). For the 3.2 mils version, the pad diameter is 10 mils (0.254 mm, still in spec range 0.25 - 0.35 mm and follow IPC-7351). With the 3.2 mils width/clearance rules, it can easily draw out two or three functional pins through blank area (between pin groups), as shown in Figure 4.

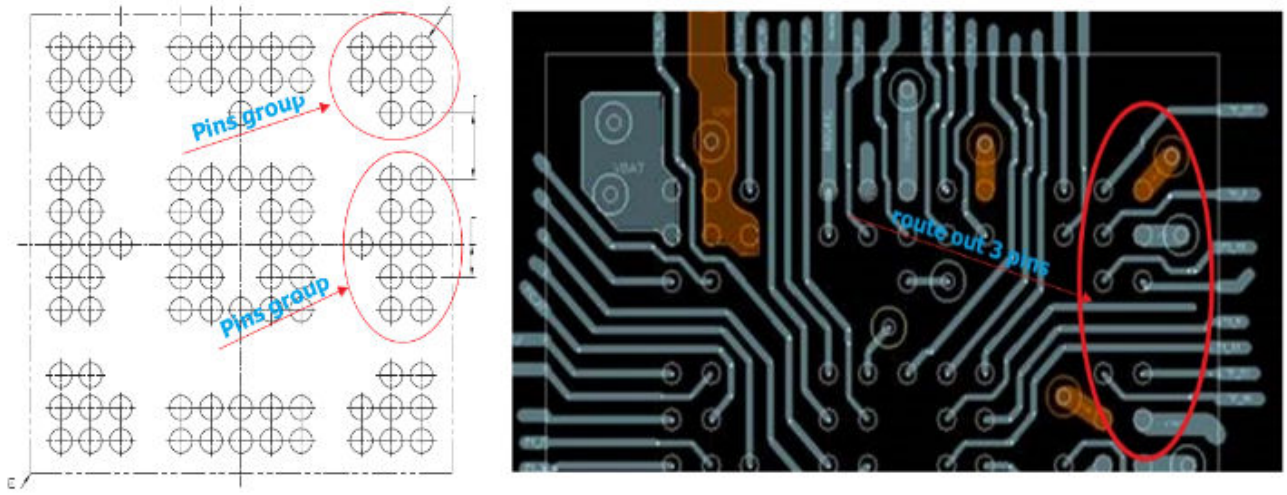

Figure 4. Routing two or three pins through blank area

The package of this application note provides allegro PCB reference source files. For details, see the BMS-00108.brd file. Figure 5 shows the layout reference design.

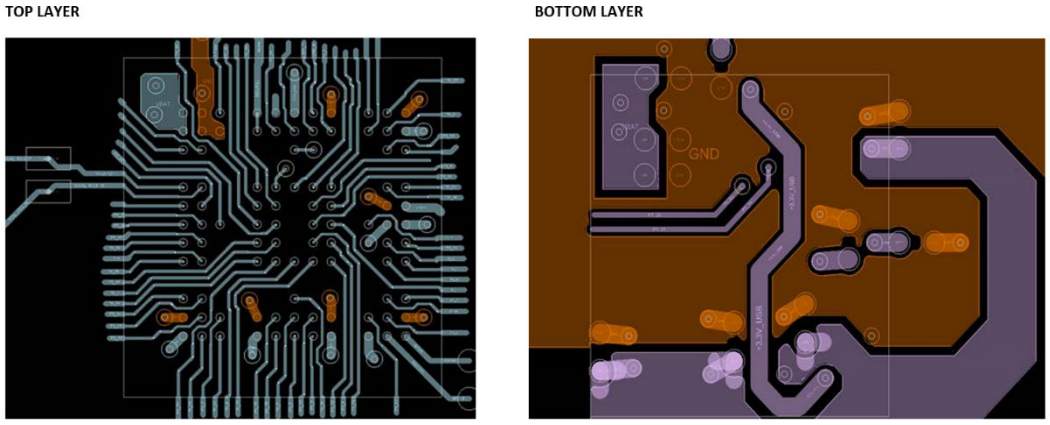

Figure 5. 3.5 mil layout reference design

3.2 5 mils line/space limitation

The required trace width of the ultra-low cost PCB process of the 5 mils layout version is 5 mils, and the clearance is also 5 mils. Table 3 describes the layout rules.

For the 5 mil version, we can not lead all functional pins. Regarding the VFBGA98 as QFN48, the QFN48 package size is 7 mm × 7 mm, which is same as VFBGA98. For most of QFN48 packages, MCU supports 31-37 functional pins (except power/GND). If the rules follow the 5 mil version guideline, user can lead out:

28 GPIO pins, three SWD (w/ RESET) pins, three USB1 (High Speed) pins, and four Crystal pins.

Consider the real application requirement on functional pins. Usually, SWD/USB/Crystal pins can be replaced with GPIOs. So the 5 mils version layout can lead 37-38 GPIO pins.

Table 3. Layout rules for 5 mils version

VFBGA98 Pad diameter	10 mils (0.254 mm)	
Net rules	**Default/Neck down**	**Power/GND**
Trace width	5 mils	8 mils (min.)
Trace to Trace	5 mils	5 mils (min.)
Trace to Pad	5 mils	5 mils (min.)
Trace to Via	5 mils	5 mils
Through Via	12 mil drill & 24 mil pad	
Layers	2-layer (Top & Bottom)	

Due to the wire width and clearance setting of the 5 mils, we can only lead two physical pins through two **Pin group**, as shown in Figure 6.

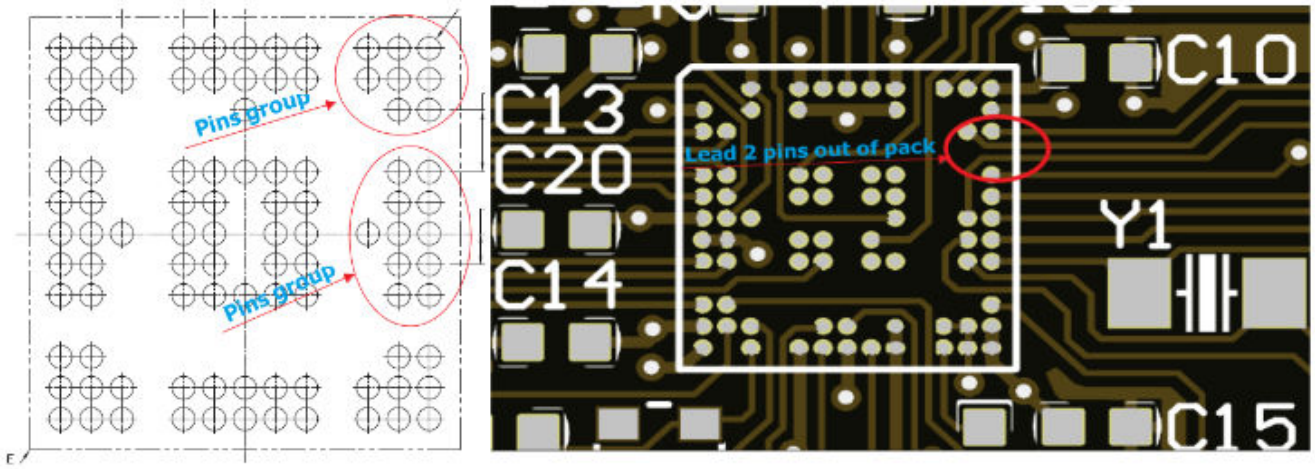

Figure 6. Routing two pins through blank area

NXP has designed basic system board based on 5 mil rules. The PCB files are in the `*.zip` file attached to this document. The drawing tool is Aluminum Design PCB tool. For details, refer to `LPCup.pcb`. Figure 7 shows the layout reference design.

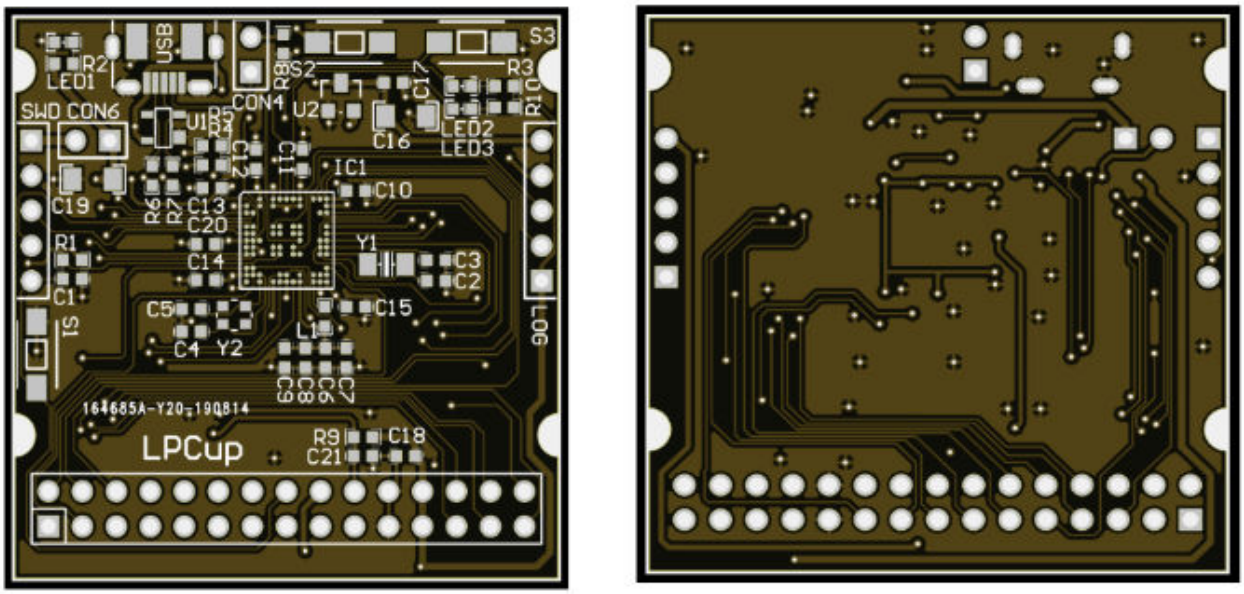

Figure 7. LPC55S69JEV98 basic system PCB board

4 Conclusion

This application note introduces two solutions of 2-layer PCB layout for VFBGA98. The solutions can help to reduce the PCB cost. The cost of a 4-layer PCB is much higher than that of a 2-layer PCB (for additional material, production step, production time, and so on). After consulting with PCB vendors, we also know that the 5 mils process is more effective than 3.5 mils.

The two solutions, 3.5 mil and 5 mils, are provided for different application requirements. Both can help to reduce the PCB cost if need. The original PCB design files are also provided along with this application note.

5 References

- LPC55S6x product data sheet (document LPC55S6x, NXP Semiconductors, 8 April 2019)
- VFBGA package information (document https://www.nxp.com/docs/en/package-information/SOT1982-1.pdf, NXP Semiconductors, 1 October 2018

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