AN12409

i.MX 6/7/8 series USB Certification Guide

Rev. 4 — 8 June 2023 Application note

Document Information

Information	Content
Keywords	i.MX 6/7/8, USB Certification Test, USB Compliance Test
Abstract	The purpose of this document is to describe how to perform USB Certification Test on the i.MX 6/7/8 series family of applications processor. This document constitutes the description of procedures, tools, and criteria for USB Compliance Test.

1 Introduction

The purpose of this document is to describe how to perform USB Certification Test on the i.MX 6/7/8 series family of applications processor. This document constitutes the description of procedures, tools, and criteria for USB Compliance Test.

2 Test preparing

This chapter lists all required materials for running the compliance test, including equipment, documents, software and so on.

2.1 Test board

Tests were performed on the following boards:

- **MCIMX8 Series（Example）**
- **MCIMX7 Series**
- **MCIMX6 Series**

2.2 Test environment

- DUT OS: Linux version 4.9.51 (Example)
- Test Bed Computer OS: WIN 10 and WIN 7

2.3 Test equipment

The following tables list the test equipment and the tests for which they are required. We used Keysight(Agilent) equipment for USB Electrical Test, but customer may use equipment from other vendors instead, such as Tektronix, Lecroy.

Table 1. Digital Oscilloscope, Software, and Accessories

Test Equipment			Tests				
Part Number	Description	Manufacturer	Embedded Host Super-Speed transmitter	Device Super-Speed transmitter	Embedded Host Hi-Speed	Device Hi-Speed	Low/Full Speed
U7243B	USB 3.0 5 Gbps and 10 Gbps Transmitter Compliance Software	Keysight(Agilent)	1	1	N/A	N/A	N/A
N5416A	USB 2.0 Automated Software	Keysight(Agilent)	N/A	N/A	1	1	1
DSAV204A	Infiniium V-Series Oscilloscopes	Keysight(Agilent)	1	1	N/A	N/A	N/A
DSO9254A	Digital real-time Oscilloscope	Keysight(Agilent)	N/A	N/A	1	1	1
1169A	Differential Probe Amplifier	Keysight(Agilent)	N/A	N/A	1	1	N/A
N5381A	Differential solder in Probe head	Keysight(Agilent)	N/A	N/A	1	1	N/A
E2697A	Single-ended Probe	Keysight(Agilent)	N/A	N/A	N/A	N/A	3
N2774A	Current probe	Keysight(Agilent)	N/A	N/A	N/A	N/A	1
54855-67604	Precision BNC male to SMA 3.5 Female Adapter	Agilent	2	2	N/A	N/A	N/A

Table 1. Digital Oscilloscope, Software, and Accessories*...continued*

Test Equipment			Tests				
Part Number	**Description**	**Manufacturer**	**Embedded Host Super-Speed transmitter**	**Device Super-Speed transmitter**	**Embedded Host Hi-Speed**	**Device Hi-Speed**	**Low/Full Speed**
15443A	cable pair consists of two cables SMA (m) to SMA (m)	Keysight(Agilent)	2	2	N/A	N/A	N/A
HSEHET Board	High-Speed Embedded Host Electrical Test Board	Allion	N/A	N/A	1	N/A	N/A
Packet-Master USB-PET	USB Protocol and Electrical Tester	MQP	N/A	N/A	1	N/A	N/A
33401A	Digital Multimeter equivalent.	Keysight(Agilent)	N/A	N/A	1	1	1
P40A-1P2J	DC5V Power Supply	SunPower	N/A	N/A	1	1	1

Table 2. Test Fixtures for USB Electrical Test

Test Fixture			Tests				
Part Number	**Description**	**Manufacturer**	**Embedded Host Super-Speed transmitter**	**Device Super-Speed transmitter**	**Embedded Host Hi-Speed**	**Device Hi-Speed**	**Low/Full Speed**
5M 94V-0 3913-01	USB 3.0 Device Test Fixture-1	Intel	N/A	1	N/A	N/A	N/A
5M 94V-0 3913-01	USB 3.0 Host Test Fixture-1	Intel	1	N/A	N/A	N/A	N/A
5M 94V-0 3913-01	USB 3.0 Device Test Fixture-2	Intel	N/A	1	N/A	N/A	N/A
5M 94V-0 3913-01	USB 3.0 Host Test Fixture-2	Intel	1	N/A	N/A	N/A	N/A
5M 94V-0 4316 16-15	USB 3.0 Device Test Fixture-1C	Intel	N/A	1	N/A	N/A	N/A
5M 94V-0 4316 16-16	USB 3.0 Host Test Fixture-1C	Intel	1	N/A	N/A	N/A	
E2649-66401	Device High-Speed Signal Quality Test Fixture	Keysight(Agilent)	N/A	N/A	N/A	1	N/A
E2649-66402	Host High-Speed Signal Quality Test Fixture	Keysight(Agilent)	N/A	N/A	1	N/A	N/A
E2649-66405	USB 2.0/3.0 Droop/Drop TestFixture	Keysight(Agilent)	N/A	N/A	N/A	N/A	1
E2646A/B	USB Inrush (SQiDD) Test Fixture	Keysight(Agilent)	N/A	N/A	N/A	N/A	1
E2649-66403	Receiver Sensitivity Test Fixture	Keysight(Agilent)	N/A	N/A	1	N/A	N/A

Table 3. Digital Signal Generator for Receive Sensitivity Test

Required Equipment			Tests				
Part Number	**Description**	**Manufacturer**	**Embedded Host Super-Speed transmitter**	**Device Super-Speed transmitter**	**Embedded Host Hi-Speed**	**Device Hi-Speed**	**Low/Full Speed**
82357A	USB/GPIB interface	Keysight(Agilent)	N/A	N/A	N/A	1	N/A
81130A	Pulse/Pattern generator	Keysight(Agilent)	N/A	N/A	N/A	N/A	N/A
8493C	6 dB attenuators	Keysight(Agilent)	N/A	N/A	N/A	1	N/A
8120-4948 or equivalent	50 ohm coaxial cable with male SMA connectors at both ends	Keysight(Agilent)	N/A	N/A	N/A	2	N/A

Table 4. Miscellaneous cables and devices

Required Equipment	Tests				
Description	Embedded Host Super-Speed transmitter	Device Super-Speed transmitter	Embedded Host Hi-Speed	Device Hi-Speed	Low/Full Speed
5 m USB cable (any listed on USB-IF website)	N/A	N/A	1	1	6
1.5 m USB cable (any listed on USB-IF website)	N/A	N/A	1	N/A	N/A
1 m USB cable (any listed on USB-IF website)	N/A	N/A	N/A	N/A	1
4'' USB cable(any listed on USB-IF website)	N/A	N/A	1	1	1
Hi-Speed USB Hub (any listed on USB-IF website)	N/A	N/A	4	N/A	4
Full-Speed USB Hub (any listed on USB-IF website)	N/A	N/A	1	N/A	1
Super-Speed USB Hub (any listed on USB-IF website)	1	1	N/A	N/A	N/A
High-Speed USB Device (any listed on USB-IF website)	N/A	N/A	1	1	N/A
Full-Speed USB Device (any listed on USB-IF website)	N/A	N/A	N/A	N/A	1
Low-Speed USB Device (any listed on USB-IF website)	N/A	N/A	N/A	N/A	1

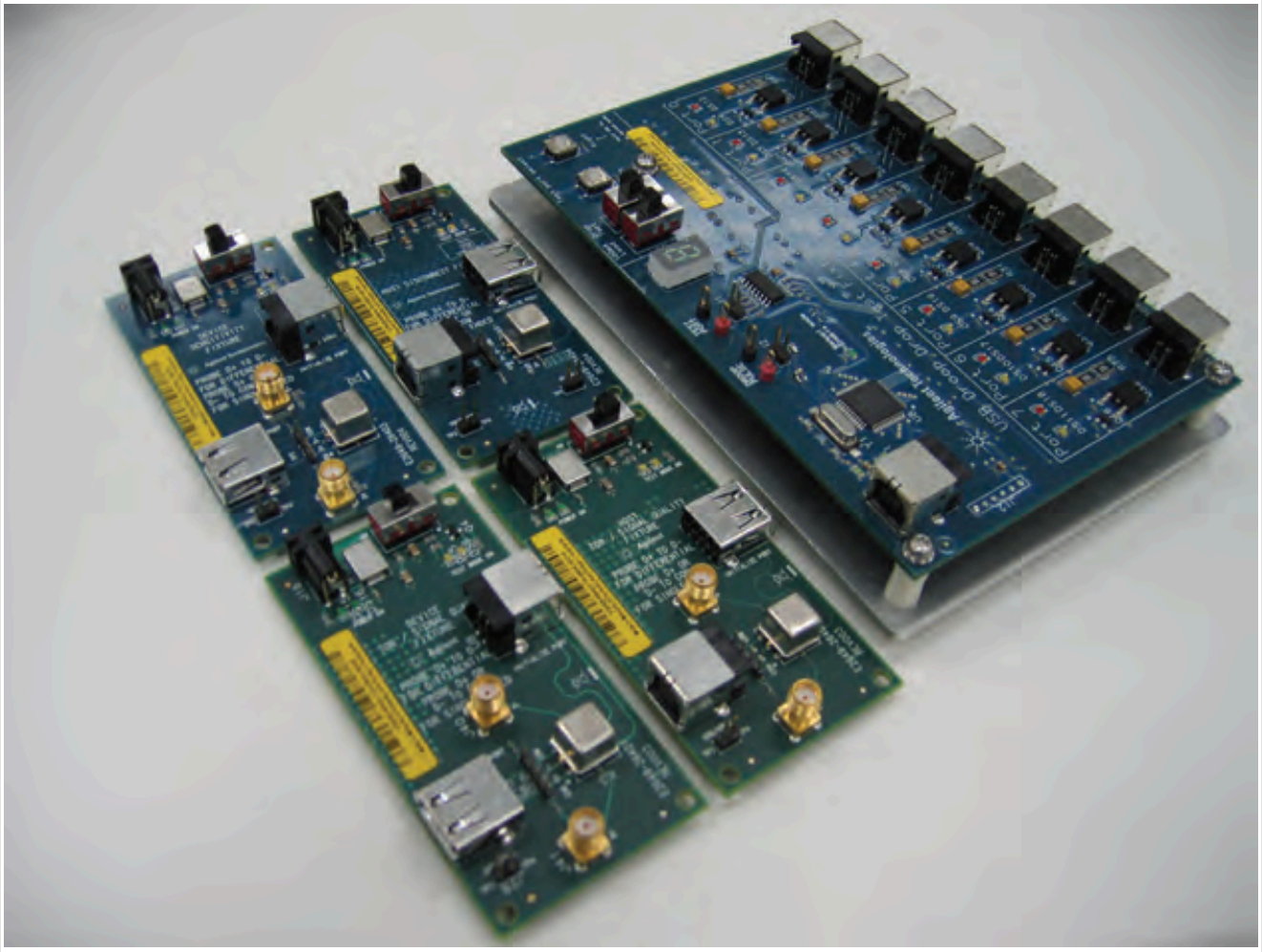

Figure 1. E2649 High-Speed Test Fixture Set

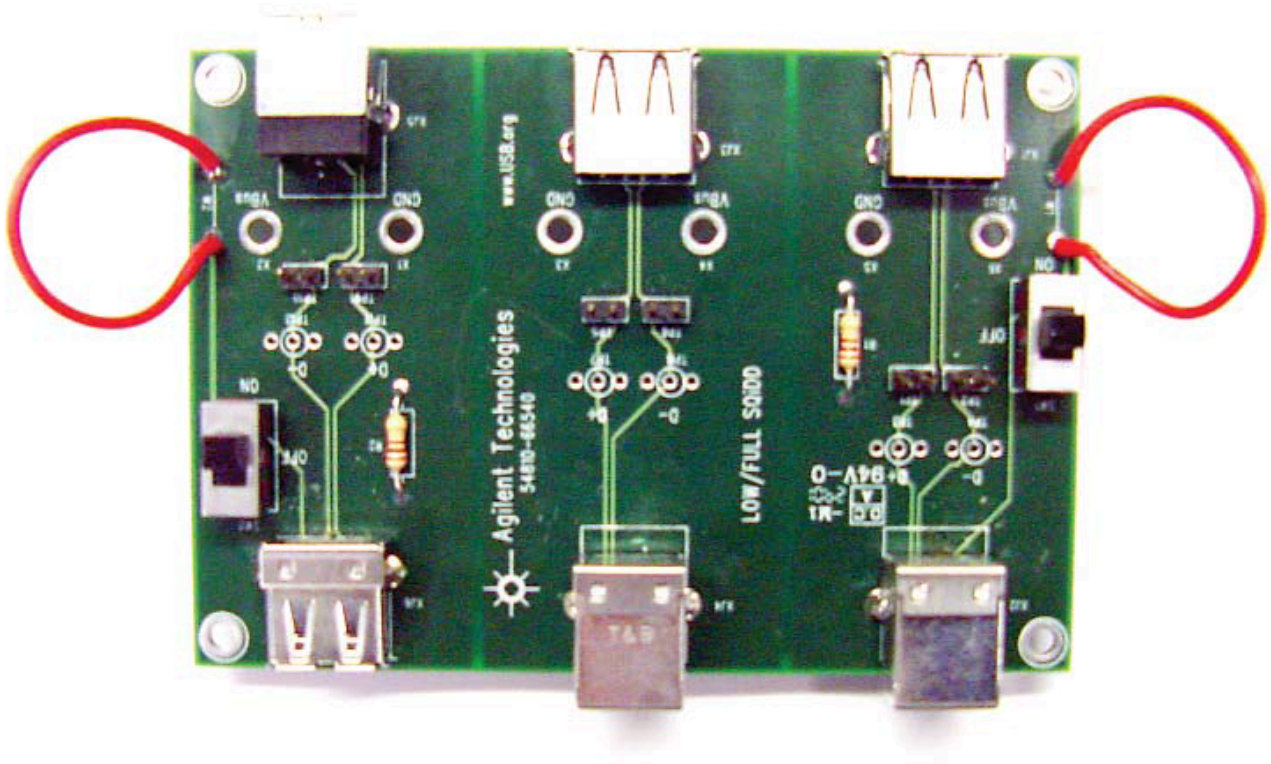

Figure 2. E2646A/B SQiDD Test Fixture

Figure 3. 5M 94V-0 Super Speed Test Fixture Set

2.4 Test software

Table 5. Test software used for USB Certification Test

Name	Version	Description
USBET20	1.20	USB Electrical Analysis Tool

Table 5. Test software used for USB Certification Test*...continued*

Name	Version	Description
USBHSET	1.2.2.1	Window-based utility Tool used to initiate test modes
USB20CV	1.4.11.0	USB 2.0 Command Verifier for USB 2.0 Device Framework testing
USB30CV	1.1.2.0	USB 3.0 Command Verifier for USB 3.0 Device Framework testing
GraphicUSB	4.47	Test software for PET Test

Note: *Download the latest software from the websites of USB-IF and MQP.*

2.5 USB-IF required tests

Devices which support features of [USB 3.0] and [USBOTG&EHv2.0] shall undergo additional testing beyond the tests described in this document. This additional testing is a subset of existing tests for USB peripherals and USB host controllers.

Table 6 describes which tests are required for full USB-IF certification by an EH with a Standard-A, Type C, or Micro-AB connector.

Table 7 describes which tests are required for full USB-IF certification by a Device with a Micro-AB, Micro-B connector, or Type C.

Table 6. Embedded Host test requirements

USB-IF test ► USB speed ▼	Enhanced SS Electrical	Automated Test Ch6	Manual Test Ch7	Drop/Droop	DS LS SQT	DS FS SQT	DSHS Electrical
Super-Speed Host	/*						
High-Speed Host		✓	✓	✓ / **	*	*	✓
Full-SpeedHost		✓	✓	✓ / **	*	*	
Low-Speed Host		✓	✓	✓ / **	✓		

Table 7. Device test requirements

USB-IFtest ► USB speed ▼	Enhanced SS Electrical	IOP Goldtree	Avg Current	Automated Test Ch6	Manual Test Ch7	USBCV	Back-Voltage	Inrush Current	US LS SQT	US FS SQT	USHS Electrical
SS Device	✓ / *										
FS Device		✓	✓	*	✓	✓	✓	✓	*	*	
HS Device		✓	✓	*	✓	✓	✓	✓	*	*	✓

Note:

- *USB-IF allows Embedded Host to use the Micro-AB receptacle in 2012.*
- *For peripheral, if the silicon is only compliant with the general USB 2.0 spec, it is recognized as standard USB2.0 peripheral, Automated Test Ch6 must not be launched. If the silicon is compliant to the supplement of OTG and EH Rev. 2.0 (with OTG descriptor in the declaration), the device is recognized as B-device, so Automated Test Ch6 must be launched.*

The following symbols are used in these tables: ✓ Always required * Required if feature is supported ** Required if there are multiple downstream ports.

2.6 Five avenues to certify

There are five avenues for certifying a product with the USB-IF.

1. Participate in a USB-IF Sponsored Compliance workshop (USB-IF Member Company Benefit Only)
2. Attend an Authorized Independent Test Lab

3. Participate in the USB-IF Qualification by Similarity program
4. Attend the USB-IF Platform Interoperability Lab (USB-IF Member Company Benefit Only)

OEM Arrangements

Note: *All companies seeking to use the USB-IF logos on their product must have a valid USB-IF Trademark License Agreement on file with the USB-IF and the product must be certified.*

2.7 Register the product in USB-IF

To attend a test lab, a vendor must first Register their product with the USB-IF. The USB-IF collects a variety of registration data to categorize the product and ensure that the appropriate testing is performed. Once all registration questions are answered and appropriate documentation submitted, a vendor is able to select an ITL that is capable of testing the product type categorized by the registration information. An email will be sent to you, the ITL and USB-IF Administration confirming the selection of ITL and registration. Once the Product has been accepted for testing by an ITL a Test ID (TID) will be assigned.

1. Register and login your account at https://cms.usb.org/register-product, before that make sure your company is a member of USB-IF;
2. Click **My Account** and then click **Add a Product** to enter the Product Register page, select a product type for your product, as shown in Figure 4. If you do not know what kind of Product Type you should choose, consult your Test Lab;

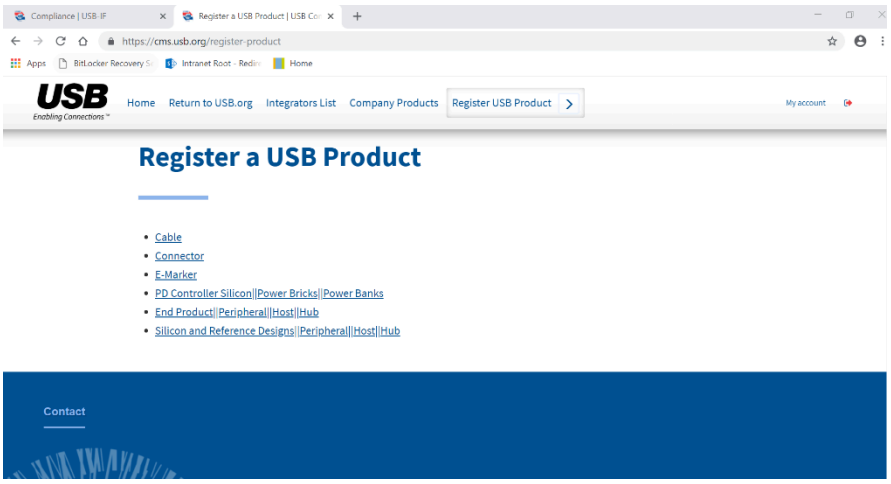

Figure 4. USB Product Type

3. Fill in the detailed information of your product, including Marketing Name, Revision, Product Category, contact window and so on.
4. Wait for USB-IF to approve it.

Note: *Make sure that the Marketing Name is the same as the product name in checklists. Use the VID of your company registered on USB-IF and not the one of your USB silicon providers.* ***The VID of NXP product on USB-IF is 1fc9 in hex or 8137 in decimal.*** *The current membership list will be available here soon. You can download the whole Company List using the following link: https://usb.org/members*

2.8 Compliance test reference documents

Get to know the whole environment settings and detailed test steps of USB Compliance Test, study the following documents:

- Universal Serial Bus 3.0 Specification, revision 1.0(USB-IF, 2008)

- Universal Serial Bus 3.1 Specification, revision 1.0(USB-IF, 2013)
- Universal Serial Bus Implementers Forum Full and Low Speed Electrical and Interoperability Compliance Test Procedure Version 1.3 (USB-IF, 2004)
- USB On-The-Go and Embedded Host Automated Compliance Plan for the On-The-Goand Embedded Host Supplement Revision 2.0 Version 1.2 (USB-IF, 2012)
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification Revision 2.0 Version 1.1A (USB-IF, 2012)
- USB-IF USB 2.0 Certification Mandatory Test Matrix (USB-IF, 2019)
- Universal Serial Bus Specification Revision 2.0 (USB-IF, 2000)
- USB 2.0 Electrical Compliance Test Specification Version 1.07(USB-IF, 2019)
- Embedded High-speed Host Electrical Test Procedure Revision 1.01 (USB-IF, 2006)
- Universal Serial Bus Implementers Forum Device Hi-Speed Electrical Test Procedure For Agilent Infiniium Revision1.2 (USB-IF, 2003)
- Universal Serial Bus Implementers Forum Host Hi-Speed Electrical Test Procedure For Agilent Infiniium Revision1.3 (USB-IF, 2004)
- Agilent N5416A USB 2.0 Compliance Test Option (Agilent, 2013)
- Gold Suite Summary Test Procedure V1.35 Draft (USB-IF)
- Allion HSEHET User Manual (Allion, 2012)
- Universal Serial Bus Revision 2.0 USB Command Verifier Compliance Test Specification Revision 1.2 (USB-IF, 2003)
- Universal Serial Bus Revision 3.1 USB Command Verifier Compliance Test Specification Revision 0.7 (USB-IF, 2015)
- Universal Serial Bus Mass Storage Class Compliance Test Specification Revision 1.1 (USB-IF, 2014)
- i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Industrial Products REV 0 (NXP, 2018)
- i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Consumer Products REV 0 (NXP, 2018)
- i.MX 8M Dual / 8M QuadLite / 8M Quad Product Lifetime Usage REV 0 (NXP, 2018)
- Quick Start Guide i.MX 8M Quad Evaluation Kit REV 0 (NXP, 2018)
- i.MX 8X Family of Applications Processors REV 0 (NXP, 2018)
- i.MX 7ULP Applications Processors REV 0 (NXP, 2018)
- i.MX 8M Mini Family of Applications Processors REV 0 (NXP, 2018)

3 Electrical test procedure

3.1 Legacy USB compliance tests

- Upstream Full Speed Signal Quality Test
- Back-Voltage Test
- Device Inrush Current Test
- Downstream Full Speed Signal Quality Test
- Downstream Low Speed Signal Quality Test
- Host Drop Test

3.1.1 Upstream full speed signal quality test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 5, and make sure you set the Test Type configuration option to “Full-Speed Far End” before running the test. Connect the equipment and test fixture as shown in Figure 6 below.
2. Invoke the HS Electrical Test Tool software on the Computer, select **Device**, and click the **TEST** button to enter the Device Test menu, see Figure 7.
3. On the Device Test Menu of the HS Electrical Test Tool software, click **Enumerate Bus** once. All devices attached to the host controller should appear in the device enumeration list.
4. Highlight the device under test and select **LOOP DEVICE DESCRIPTOR** from the Device Command drop down menu. Click **[EXECUTE]** once.
5. Click **Run Tests** in the USB Automated Test Software on Oscilloscope. After the test is finished, you can view the report in **HTML Report** page.

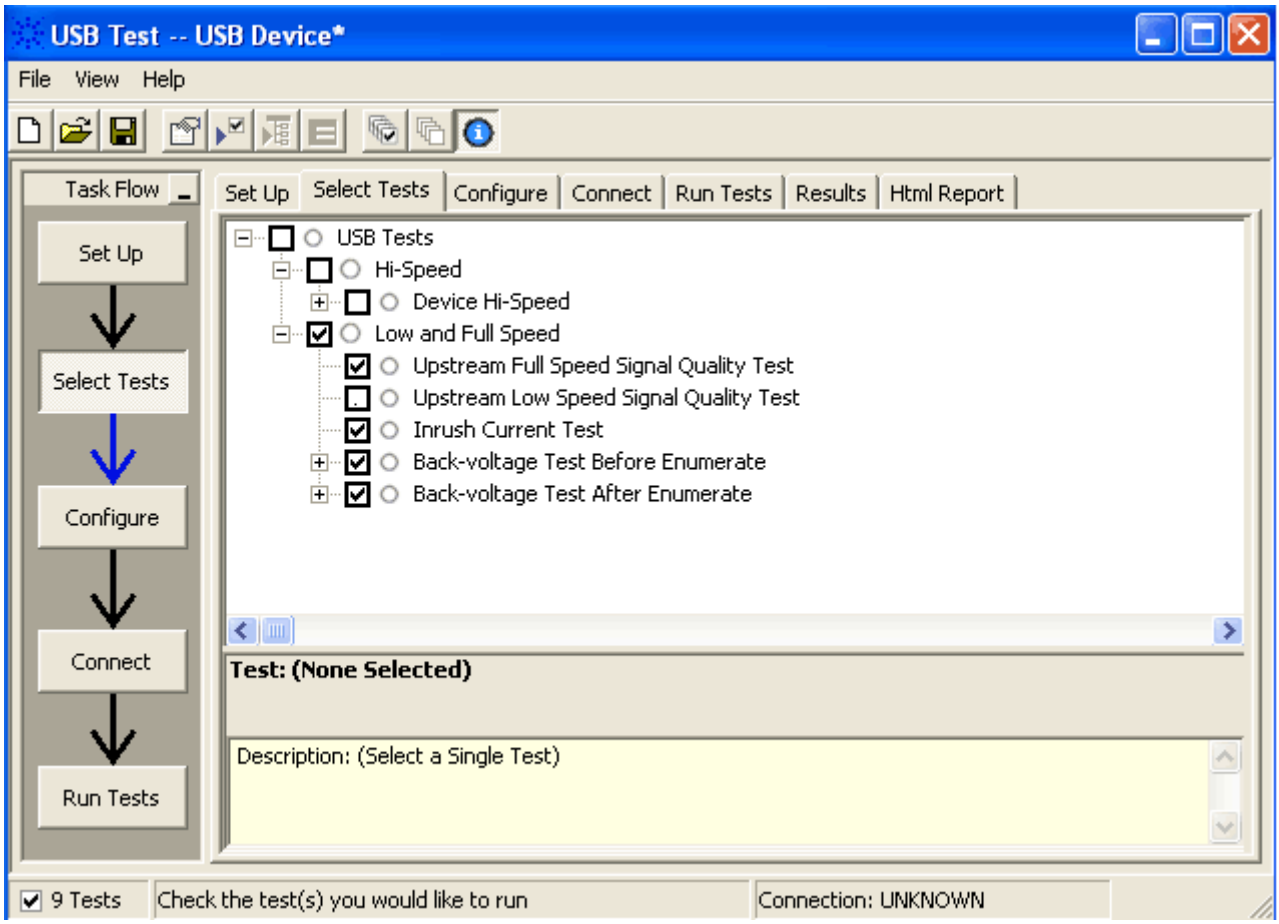

Figure 5. Automated Test Software setting for Upstream FS Signal Test

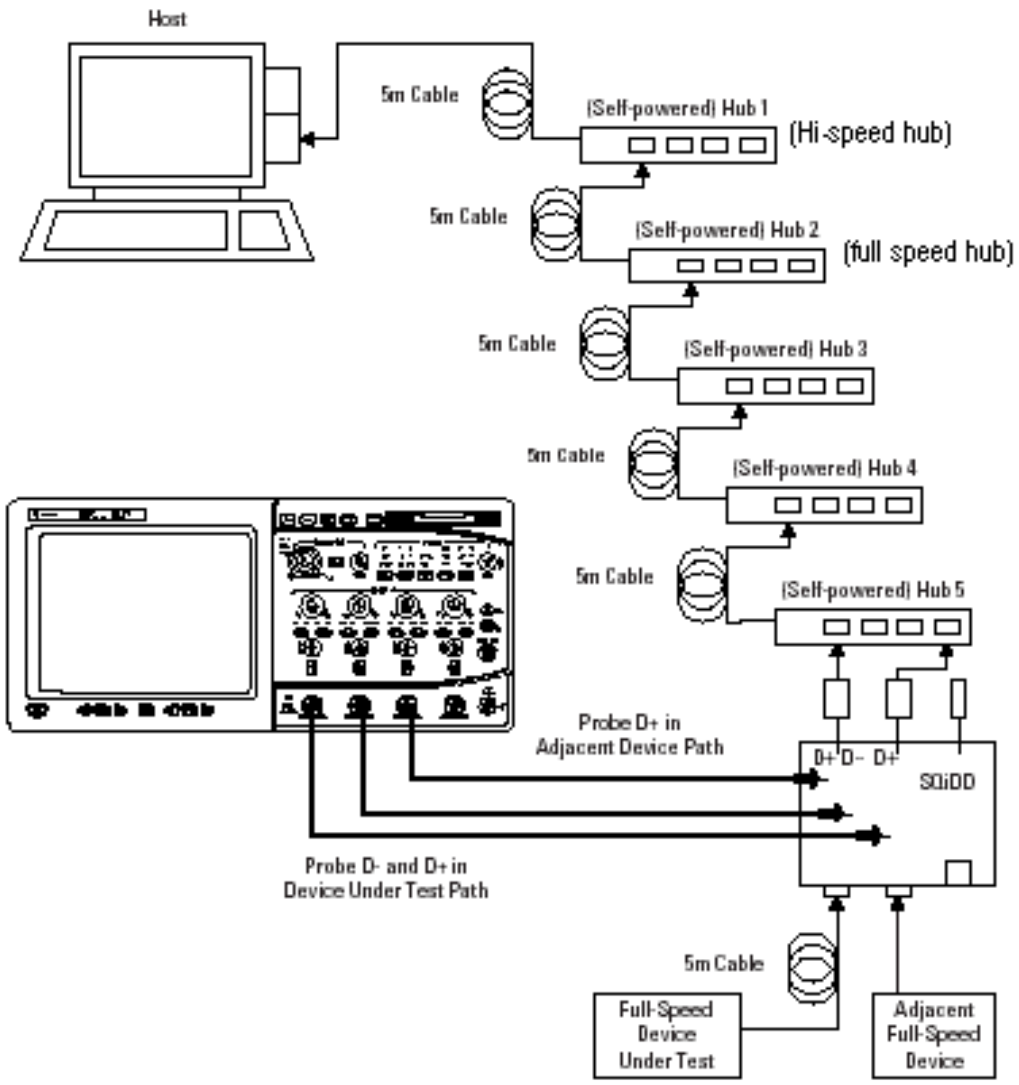

Figure 6. Upstream FS Signal Test Environment

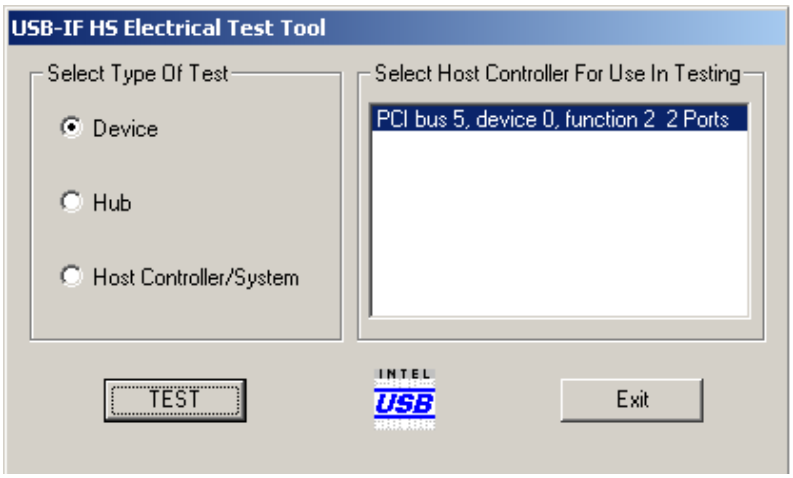

Figure 7. Electrical Test Tool Main Menu

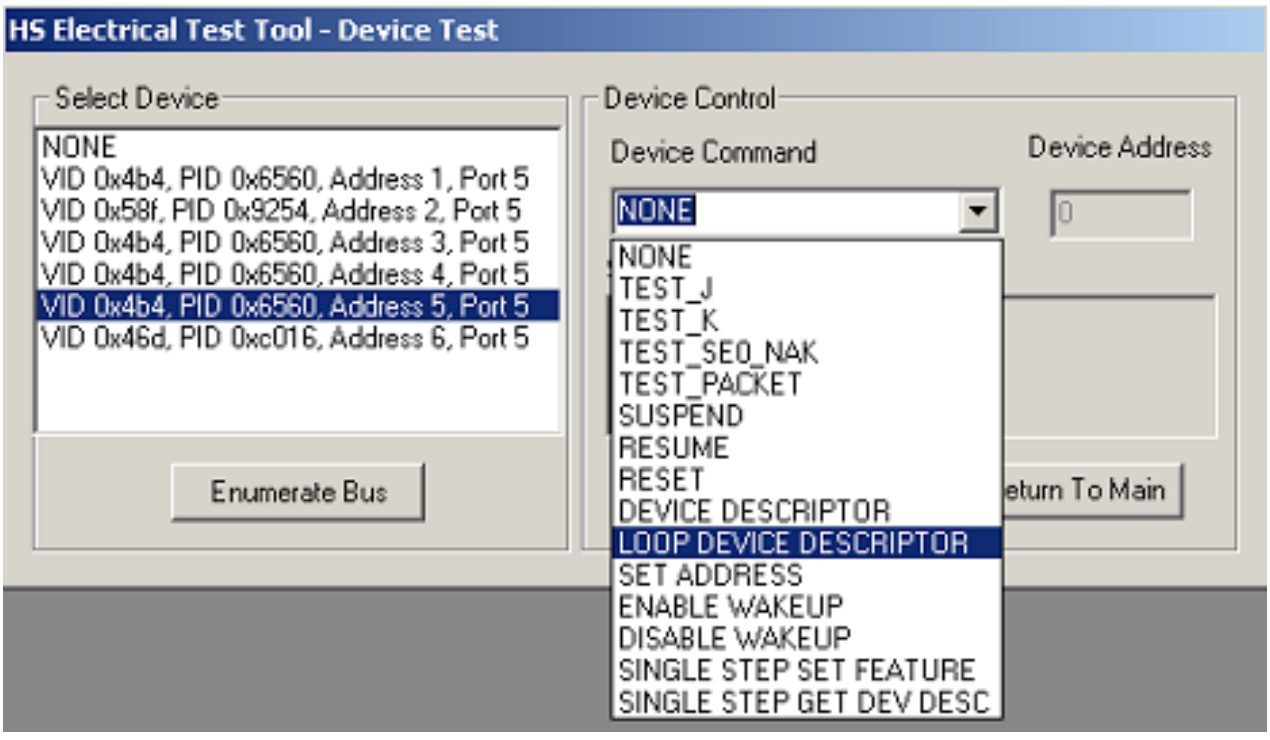

Figure 8. Device Control Command

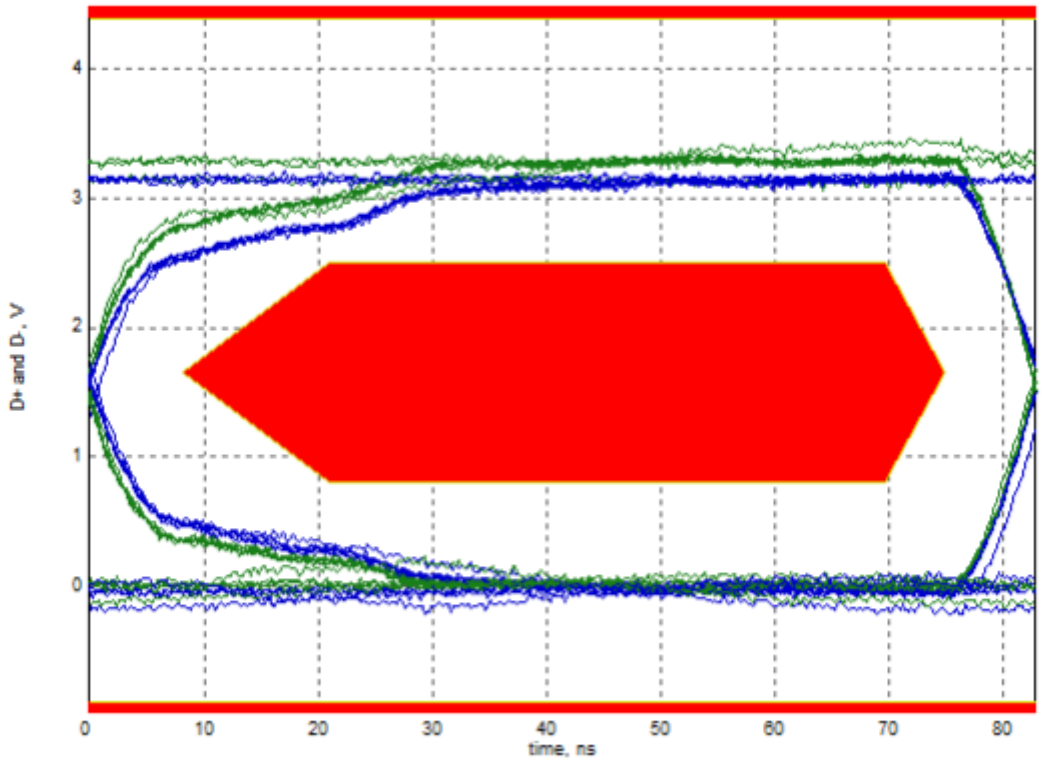

Figure 9. Upstream Full Speed Eye Diagram

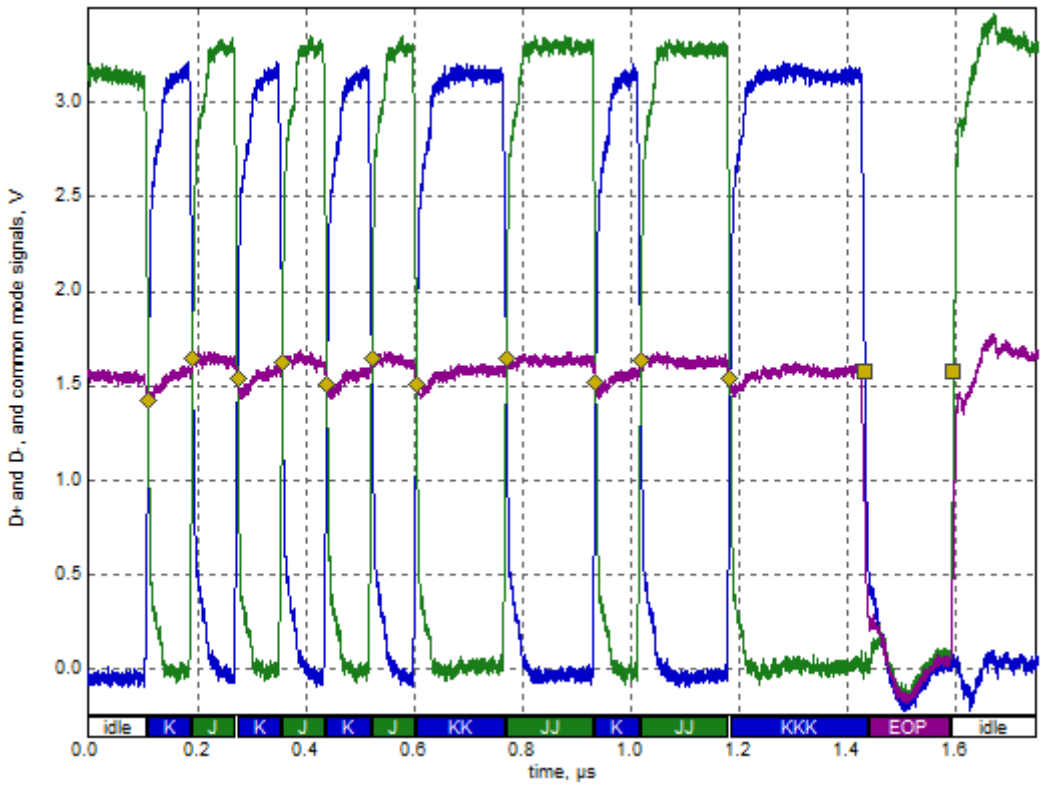

Figure 10. Upstream Full Speed Waveform

Note:

1. *i.MX is enumerated as an MSC device, Low Speed upstream is not supported. And it is ok to measure the upstream full speed EYE without the 5 tiers of hubs since it has no effect on the signal integrity itself.*
2. *High-speed electrical tests are performed either near-end or far-end depending on the configuration of the product. The terms "near-end" and "far-end" are based on which end of the cable the test fixture is attached in relation to the device being tested.*
   All HS peripherals with a B-receptacle are tested near-end (at the peripheral's receptacle). HS devices that have a captive cable are tested far-end (at the end of the captive cable). Unlike full-speed electrical tests, which are always performed far-end, the length of the cable used in HS electrical tests is not important. High-speed electrical tests of downstream ports on hosts and hubs are always performed near-end.
   - *See the detailed explanation of Far End and Near End in USB-IF Compliance Updates, http://compliance.usb.org/index.asp?UpdateFile=Electrical&Format=Standard#8*
3. *The VID of NXP product in USB-IF is 1fc9 in hex or 8137 in decimal.*
4. *A Full-Speed Hub here can force the downstream devices operating in Full-Speed Mode.*

3.1.2 Back-voltage test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 11.
2. Connect power supply to DUT and connect the device upstream port to the back-voltage test fixture using a known good USB cable as shown in Figure 12. Measure and record DC voltages on **VBUS**, **D+** and **D-**. Voltages should all be less than or equal to 400 mV. Any voltages greater than 400 mV will be recorded as a failure.

3. Plug DUT into a known good host, and verify proper enumeration. Unplug USB cable from the host and reconnect the USB cable to the back-voltage test fixture. Measure and record the DC voltages of **VBUS,D+** and **D-.** All voltages must be less than or equal to 400 mV. Any voltages greater than 400 mV will be recorded as a failure.
4. After the test is finished, you can view the report in **HTML Report** page.

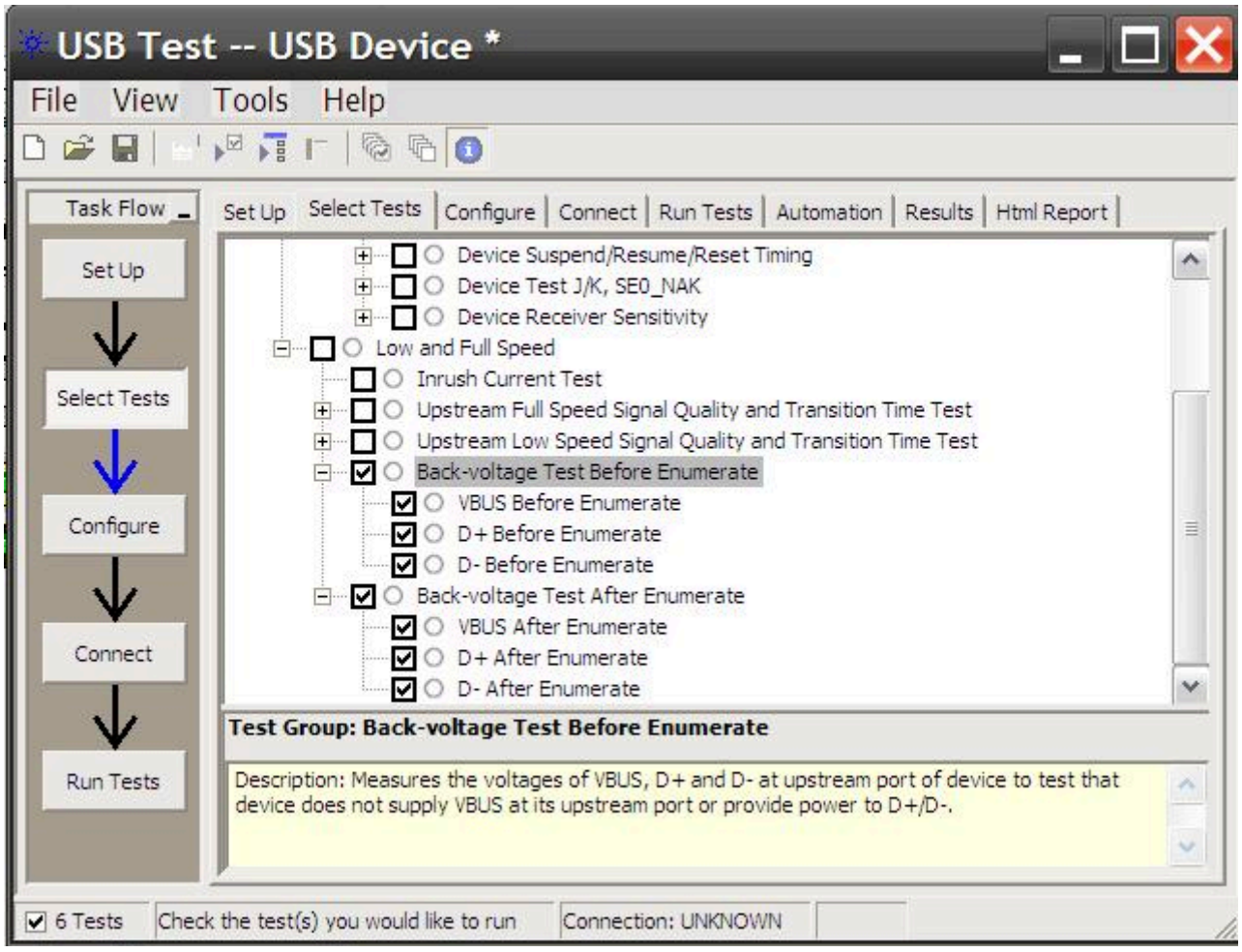

Figure 11. Automated Test Software setting for Back-Voltage Test

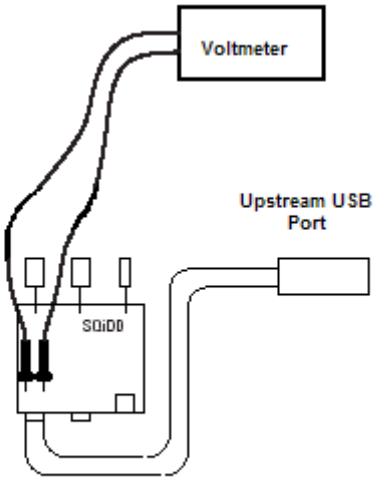

Figure 12. Back-Voltage Test Environment

Table 8. Back-Voltage Test Record

Test Point	DC Voltage Before enumeration(mV)	DC Voltage after enumeration and removal(mV)	Expected Value (VDC)
VBUS	72	72	≤ 400 mV
D+	0	0	≤ 400 mV
D-	0	0	≤ 400 mV

3.1.3 Device inrush current test

The USB 2.0 Spec allows a maximum capacity of 10uF and therefore a maximum Inrush of 50uC. It is required to have at least a 1uF of capacity in order to make ADP detection possible. The DUT cannot consume more that 100 mA during this 100 ms of the starting up. Inrush current should be measured for a minimum of 100 milliseconds after attach.

Test Instructions:

1. Connect the equipment and test fixture as shown in Figure 13, use the current probe to capture the **VBUS** current waveform, make sure that the probe direction is the same.
2. Attach the DUT to SQiDD board, then place the switch on SQiDD board to the discharge position (opposite the ON position).
3. Disconnect the DUT from SQiDD board, then place the switch on SQiDD board to the ON position.
4. Adjust the oscilloscope settings to match the current test requirement: time base 50 ms/div, Vertical resolution 500 mA/div, sample rate >1MS/s.
5. Reconnect the DUT to SQiDD board in order to capture the inrush current waveform, then save the waveform as a *.wfm or *.csv.
6. Use the analysis software "USBET20" on Computer to analyze the waveform file, then a page shows the test result as shown in Figure 15 below. The failures for Inrush mostly occur due to a too large capacity between **VBUS** and **GND.**

Note:

Note: *When doing the measurement make sure that you calibrate the current probe to 0 mA before doing the measurement since a current probe will get quickly a DC offset that will result in a wrong measurement.*

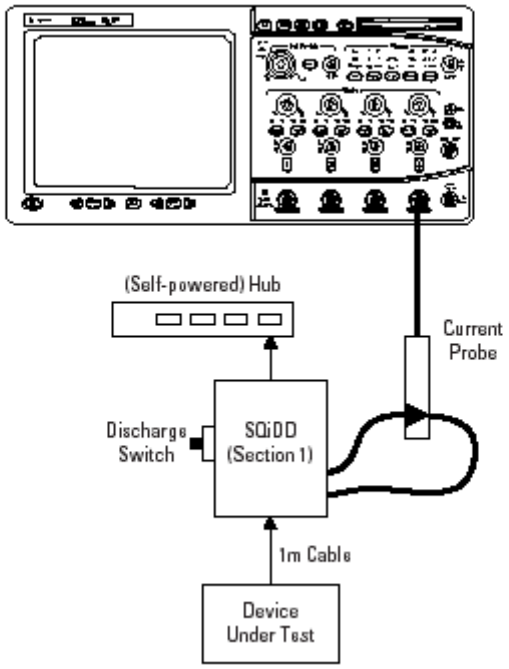

Figure 13. Device Inrush Current Test Environment

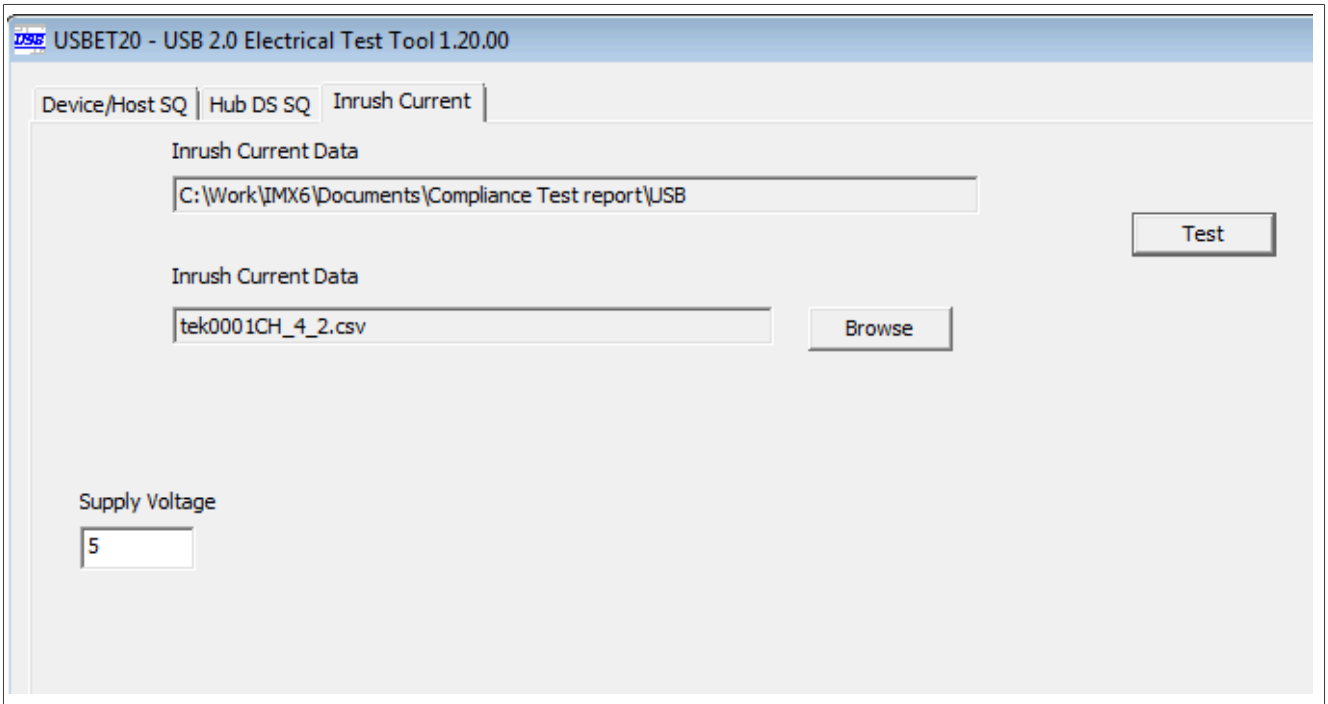

Figure 14. USBET20 operation interface

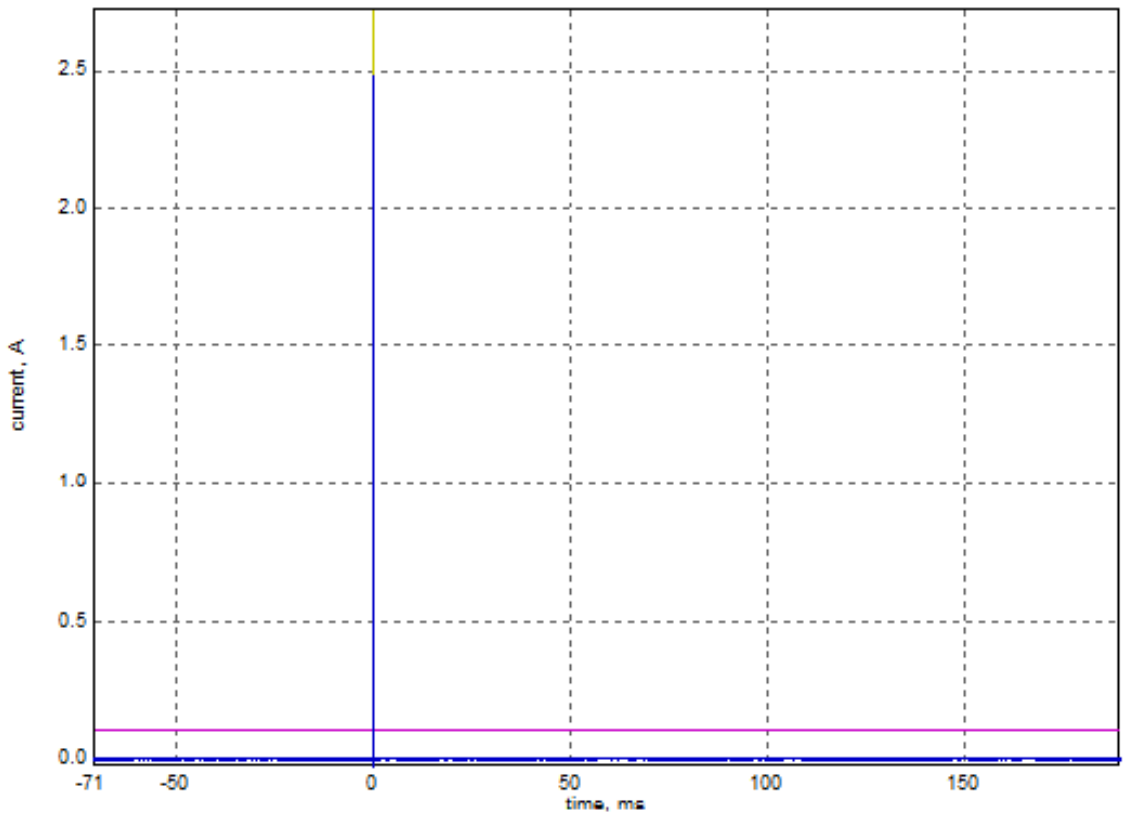

Figure 15. Device Inrush Current Test Result

3.1.4 Downstream full speed signal quality test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 16, and make sure you set the Test Type configuration option to “Full-Speed Far End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 17.
3. Click **Run Tests,** after the test is finished, you can view the report in **HTML Report** page.

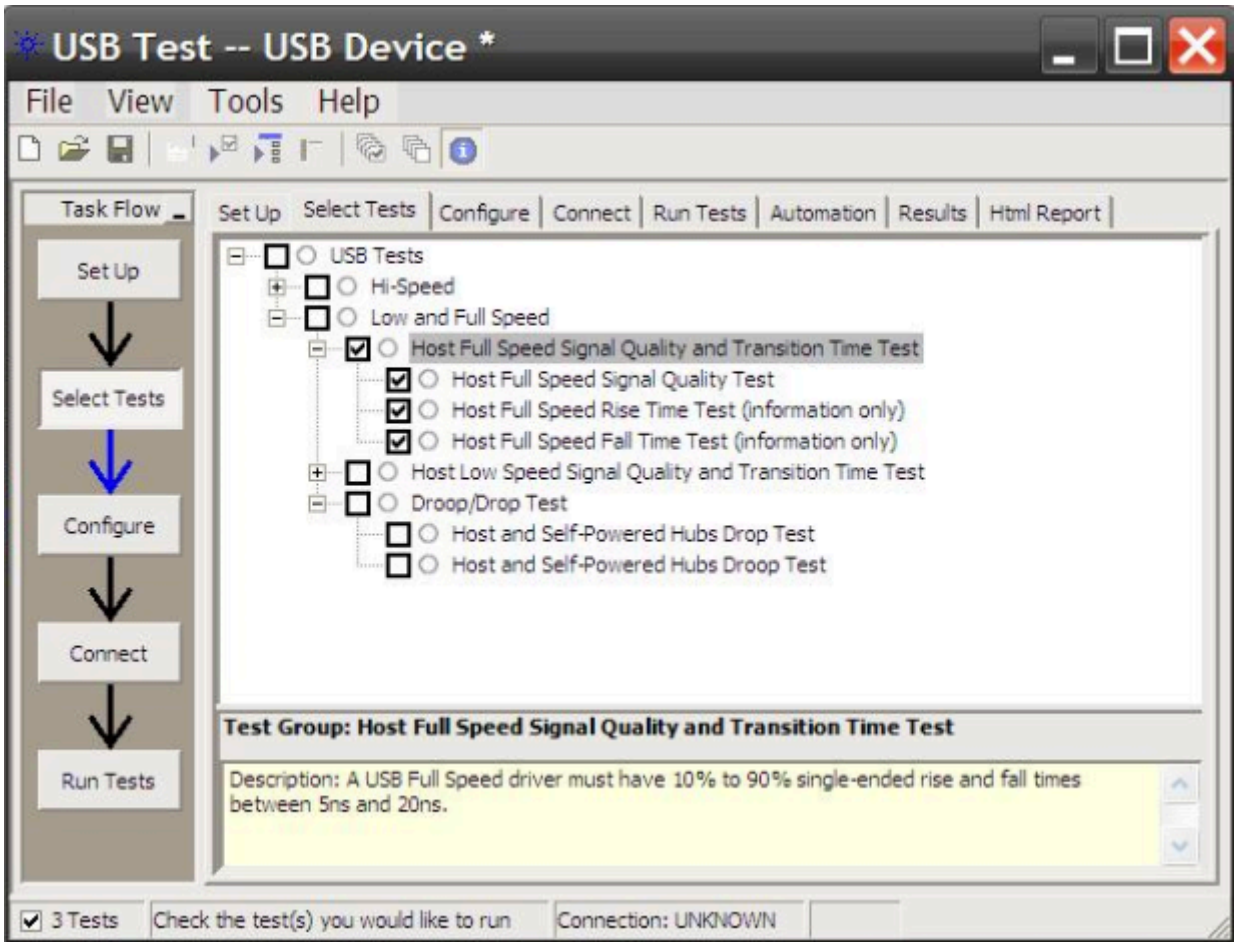

Figure 16. Automated Test Software setting for Downstream FS Signal Test

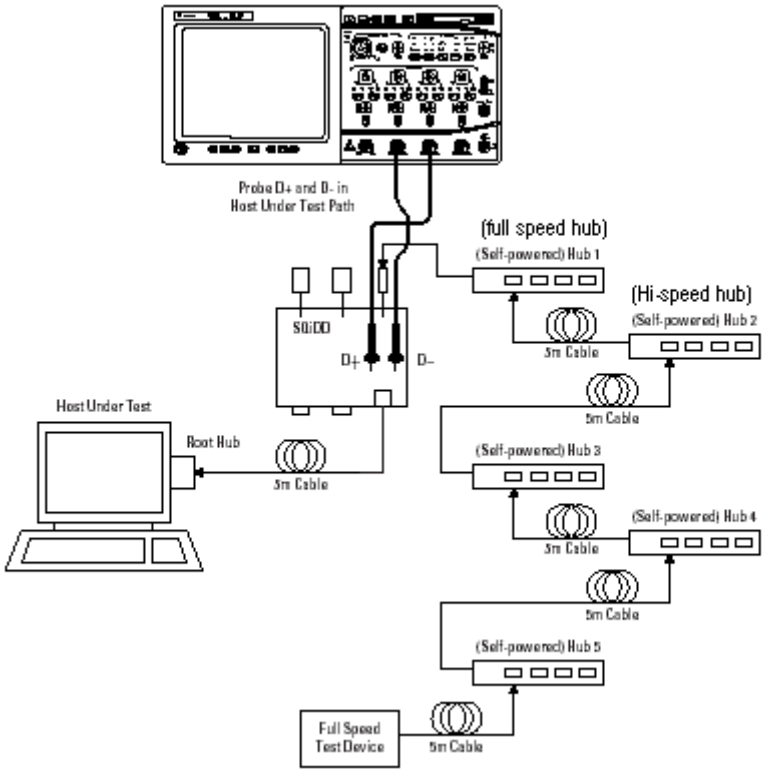

Figure 17. Downstream FS Signal Test Environment

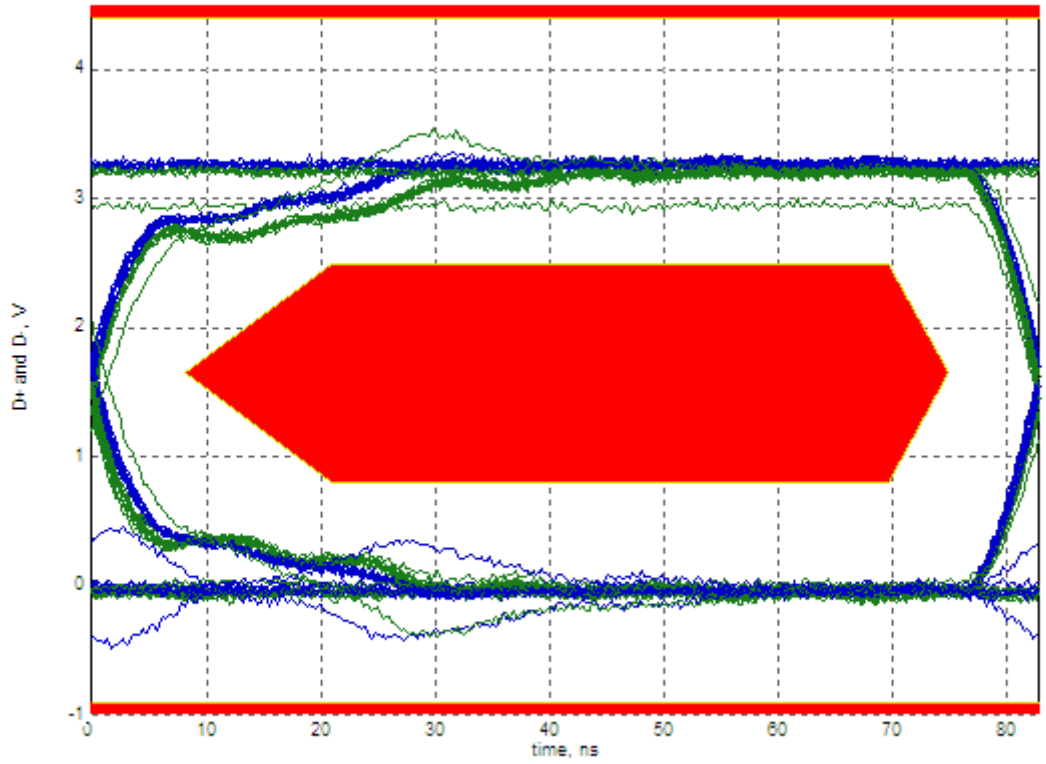

Figure 18. Downstream full-speed Eye Diagram

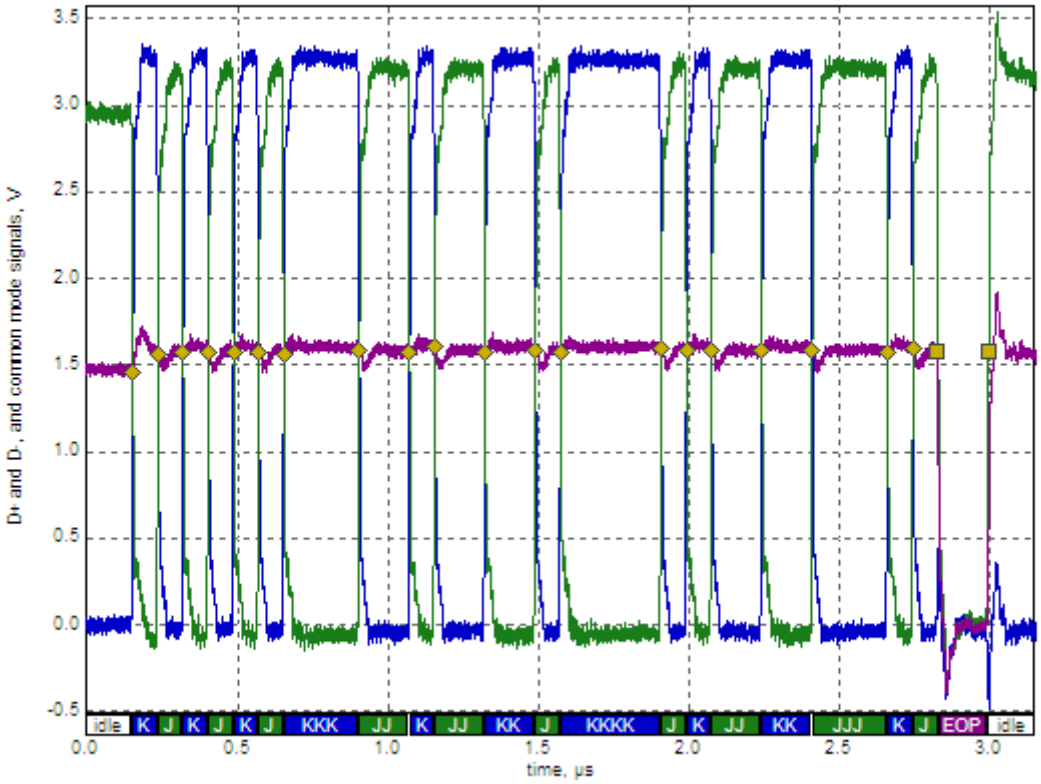

Figure 19. Downstream full-speed waveform

3.1.5 Downstream low-speed signal quality test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 20, and make sure you set the Test Type configuration option to “Low-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 21.
3. Click **Run Tests,** after the test is finished, you can view the report in **HTML Report** page.

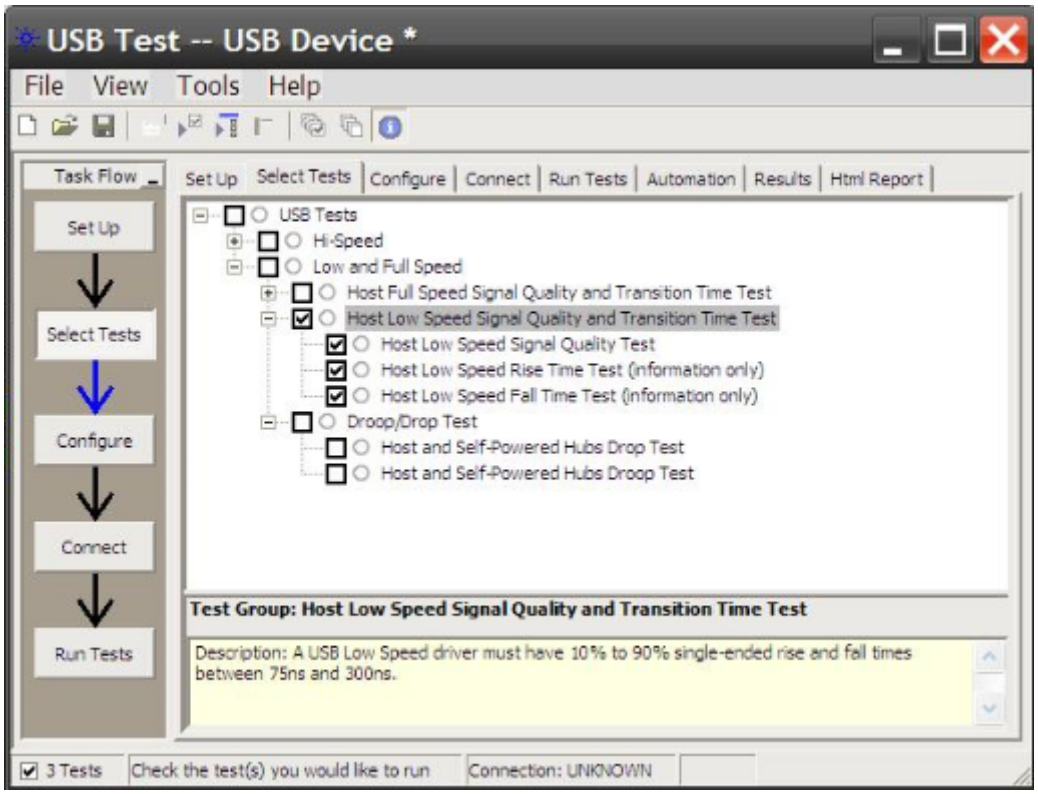

Figure 20. Automated Test Software setting for Downstream LS Signal Test

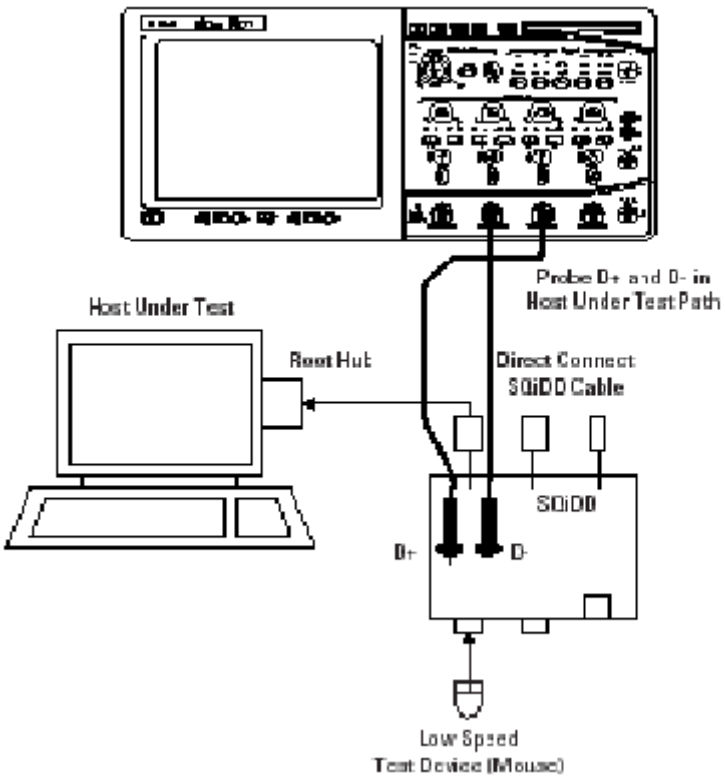

Figure 21. Downstream LS Signal Test Environment

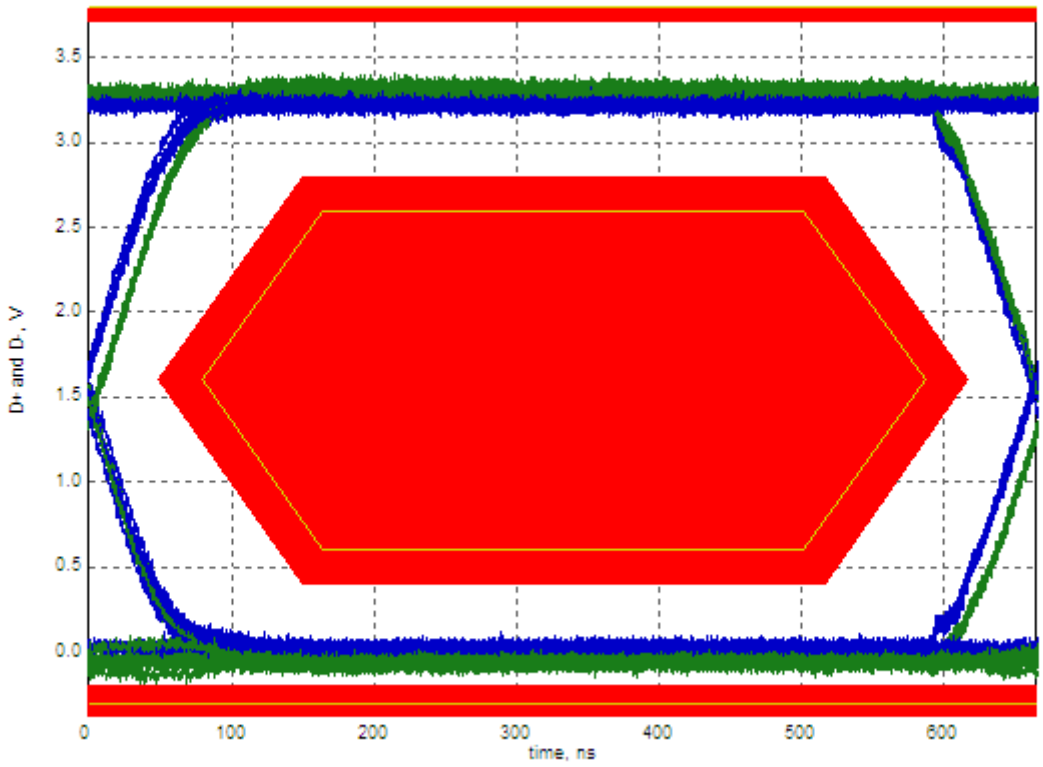

Figure 22. Downstream low-speed Eye Diagram

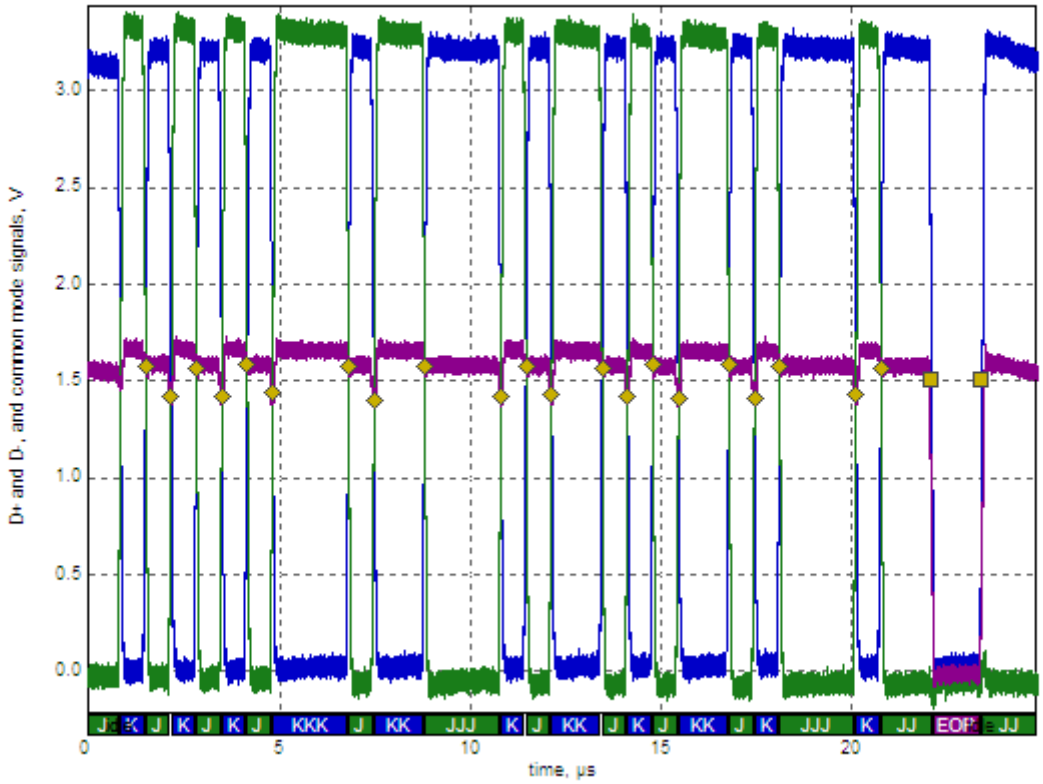

Figure 23. Downstream low-speed waveform

3.1.6 Host drop test

The Drop test is a measure of a Host/Hub's ability to host full load current while keeping the output voltage above spec. To perform this test, **VBUS** is measured with all downstream ports loaded with 500 mA loads (for host and self-powered hubs). The lowest value measured across all ports must be between 4.75 V and 5.5 V for host and self-powered hubs.

The Droop test is a transient test on adjacent ports. When a device is hot plugged into another port, the droop in VBUS supplied to a port must be less than or equal to 330 mV for host, self-powered, and bus powered hubs. If there is only one Host Port on board, this test is not needed.

Test Instructions:

1. First, power the test fixture from your Computer or a USB charger. The DS1 LED should illuminate (green LED).
2. There are several switches/buttons used for general control of the test fixture. They include:
   - Switch S5 allows you to select either the Droop or Drop test.
   - Switch S4 allows you to select either the 100 mA or 500 mA load.
   - Press and hold S1 for at least 3 seconds to turn on the test fixture.
   - While pressing and holding S2, press S1 to turn off the test fixture .
   - When the fixture is on, press S2 enables the left port.
   - When the fixture is on, press S1 enables the right port.

3. Measure VBUS at downstream USB connector with no cable or device inserted (no load), then record it as V_{NL}.
4. Measure VBUS at downstream USB connector with 500 mA load, then record it as V_{LOAD}.

Table 9. Host Drop Test Record

Item	Port01_Voltage	Expected Value (VDC)
$V_{non\text{-}load}$	5.19 V	4.75 V <= **VBUS**<= 5.5 V
V_{Load}	5.083 V	4.75 V <= **VBUS**<= 5.5 V
V_{drop}	107 mV	≤ 750 mV
V_{droop}	**NA**	≤ 330 mV

Note: *USB-IF has published an ECN to increase the maximum voltage on VBUS from 5.25 V to 5.5 V in August 2014. So the maximum voltage is 5.5 V now.*

Keep the following items in mind for drop test:

a) When doing the measurement take the cable resistance/voltage drop into account what can be significant with high currents. For example, if you have 0.25 Ohm resistance for cable and connectors and a current of 500 mA you will have a voltage drop of 0.125 V. Therefore the measurement should be done as near to the A-Receptacle as possible and if accessible you can measure at the A-receptacle **VBUS/GND** soldering pad. Measuring at the A-receptacle is the location that the USB specifications define to measure but since it is often too difficult to access you probably use a fixture and maybe also a cable in between, be aware that these will give some additional voltage drop.

b) During testing use the power supply that is used in the market and when changing the power supply re-test **VBUS** drop.

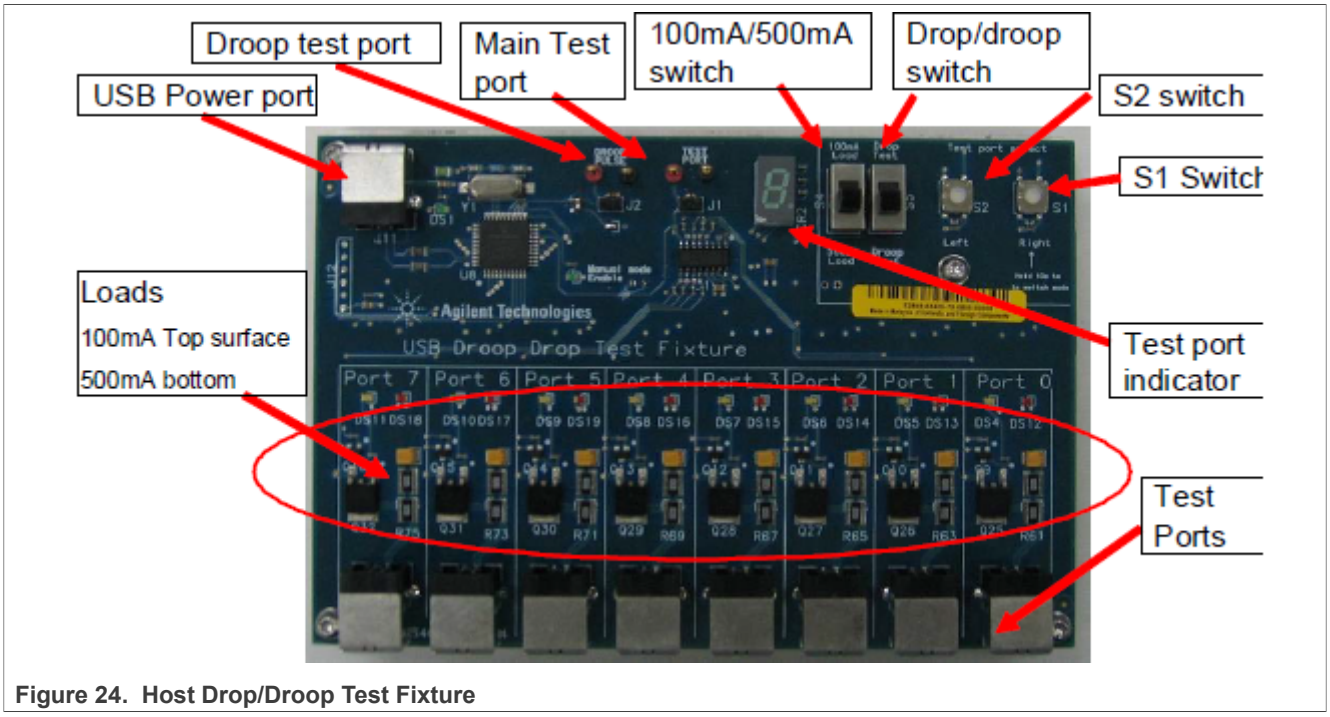

Figure 24. Host Drop/Droop Test Fixture

3.2 Device high-speed signal test

- Device High-Speed Signal Quality Test
  - **EL_2:** Data Rate Test
  - **EL_4, EL_5:** Eye Pattern Test

  - **EL_6:** Rise and Fall Time Test
  - **EL_7:** Non-Monotonic Edge Test
- Device Packet Parameters Test
  - **EL_21:** Sync Field Length Test
  - **EL_25:** EOP Length Test
  - **EL_22:** Measure Inter-packet Gap Between First and Second Packets
  - **EL_22:** Measure Inter-packet Gap Between Second and Third Packets
- Device CHIRP Timing Test
  - **EL_28:** Measure Device CHIRP-K Latency
  - **EL_29:** Measure Device CHIRP-K Duration
  - **EL_31:** Device Hi-Speed Terminations Enable and D+ Disconnect Time
- Device Suspend/Reset/Resume Timing Test
  - **EL_38, EL_39:** Device Suspend Timing Response
  - **EL_40:** Device Resume Timing Response
  - **EL_27:** Device CHIRP Response to Reset from Hi-Speed Operation
  - **EL_28:** Device CHIRP Response to Reset from Suspend
- Device Test J/K, SE0_NAK Test
  - **EL_8:** Device J Test
  - **EL_8:** Device K Test
  - **EL_9:** Device SE0_NAK Test
- Device Receiver Sensitivity Test 14
  - **EL_18:** Minimum SYNC Field
  - **EL_17:** Receiver Sensitivity Test
  - **EL_16:** Squelch

Note:

- *For High-Speed Device Test, install HS Electrical Test Tool software on Computer, which can set DUT into specific test pattern.*
- *To study the detailed description of the test items, you can read this document "USB 2.0 Electrical Test Specification" on https://usb.org/document-library/usb-20-electrical-test-specification.*
- *Device Receiver Sensitivity Test need additional equipment: Digital signal generator (for example Agilent 81130A) and related accessories.*

3.2.1 HS device electrical test limits

Table 10. HS device electrical test limits

Test Name	Pass Limits
EL_2 Data Rate	Within 480 Mb/s +/-0.05%
EL_4 Eye Pattern(Without captive cable)	Must meet Template 1 transform waveform requirements at TP3
EL_5 Eye Pattern15 (With captive cable)	Must meet Template 2 transform waveform requirements at TP2
EL_6 Device Rise/Fall Time	>500 ps
EL_7 Device Non-Monotonic Edge Test	Must have monotonic data transitions over the vertical openings
EL_21 Device Sync Field Length Test	32 bits, 65.62 ns <= VALUE <= 67.700 ns
EL_25 Device EOP Length Test	8 bits, 15.600 ns <= VALUE <= 17.700 ns
EL_22 Measure Interpacket Gap Between Second and Third Packets	16.640 ns <= VALUE <= 399.400 ns
EL_22 Measure Interpacket Gap Between First and Second Packets	16.640 ns <= VALUE <= 399.400 ns
EL_28 Measure Device CHIRP-K Latency	2.500 µs <= VALUE <= 6.000000 ms
EL_29 Measure Device CHIRP-K Duration	1.000 ms <= VALUE <= 7.000 ms

Table 10. HS device electrical test limits ***...continued***

Test Name	Pass Limits
EL_31 Device Hi-Speed Terminations Enable and D+ Disconnect Time	1 ns <= VALUE <= 500.000 µs
EL_40 Device Resume Timing Response	Must transition back to high-speed operation within two-bit times from the end of resume time signaling
EL_27 Device CHIRP Response to Reset from Hi-Speed Operation	3.100 ms <= VALUE <= 6.000 ms
EL_28 Device CHIRP Response to Reset from Suspend	2.500 µs <= VALUE <= 6.000000 ms
EL_38 EL_39 Device Suspend Timing Response	3.000 ms <= VALUE <= 3.125 ms
EL_8 Device J Test	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV
EL_8 Device K Test	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
EL_9 Device SE0_NAK Test	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV
EL_18 Minimum SYNC Field	Detect the end of the SYNC field within 12-bit times
EL_17 Receiver sensitivity	VALUE <= +/- 200 mV
EL_16 Squelch	VALUE >= +/- 100 mV

Note: *If the product used for Certification only has a standard Micro B receptacle, no captive cable, EL_5 must not be chosen.*

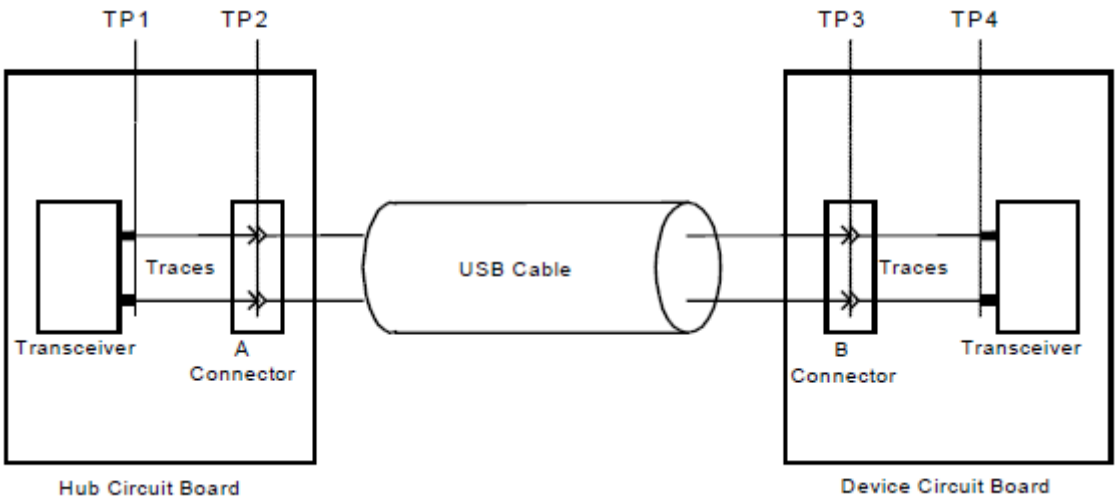

Figure 25. HS Signal Measurement Planes

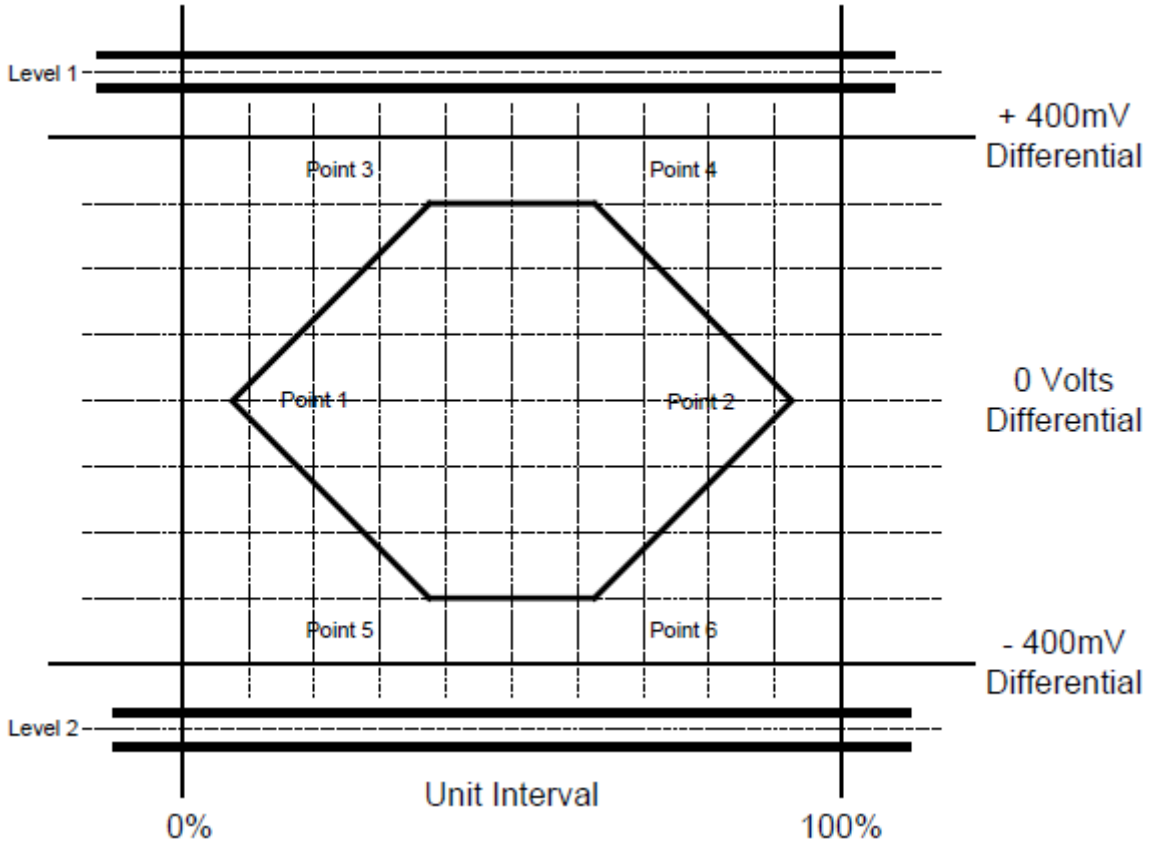

Figure 26. Template 1 for Device without a captive cable

3.2.2 Device high-speed signal quality test

These tests measure the ability of transmitters to do valid high-speed signaling. High-speed signal quality is measured on upstream ports. A high-speed scope with differential probes is used. Signaling data is captured with the scope and then translated to an eye pattern. The signal quality eye patterns obtained from the measurements must agree with the transmit eye patterns in the USB 2.0 Specification.

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 27, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 28.
   - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the Device Hi-speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
   - Connect the [**INIT PORT**] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
   - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
3. Invoke the HS Electrical Test Tool software on the Hi-Speed Electrical Test Bed Computer. Select Device and click the **TEST** button to enter the Device Test menu. The DUT should be enumerated with the device's VID shown together with the root port in which it is connected.

4. Select **TEST_PACKET** from the Device Command drop down menu and click **EXECUTE**. It forces the DUT to transmit test packets continuously.
5. Click **Run Tests** button of Automated Test Software on Oscilloscope.
6. Place the Test Switch (S1) in the **TEST** position according to the requirement of Automated Test Software. Verify that the yellow TEST LED is lit. You should see the transmitted test packet on the oscilloscope as Figure 31.
7. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

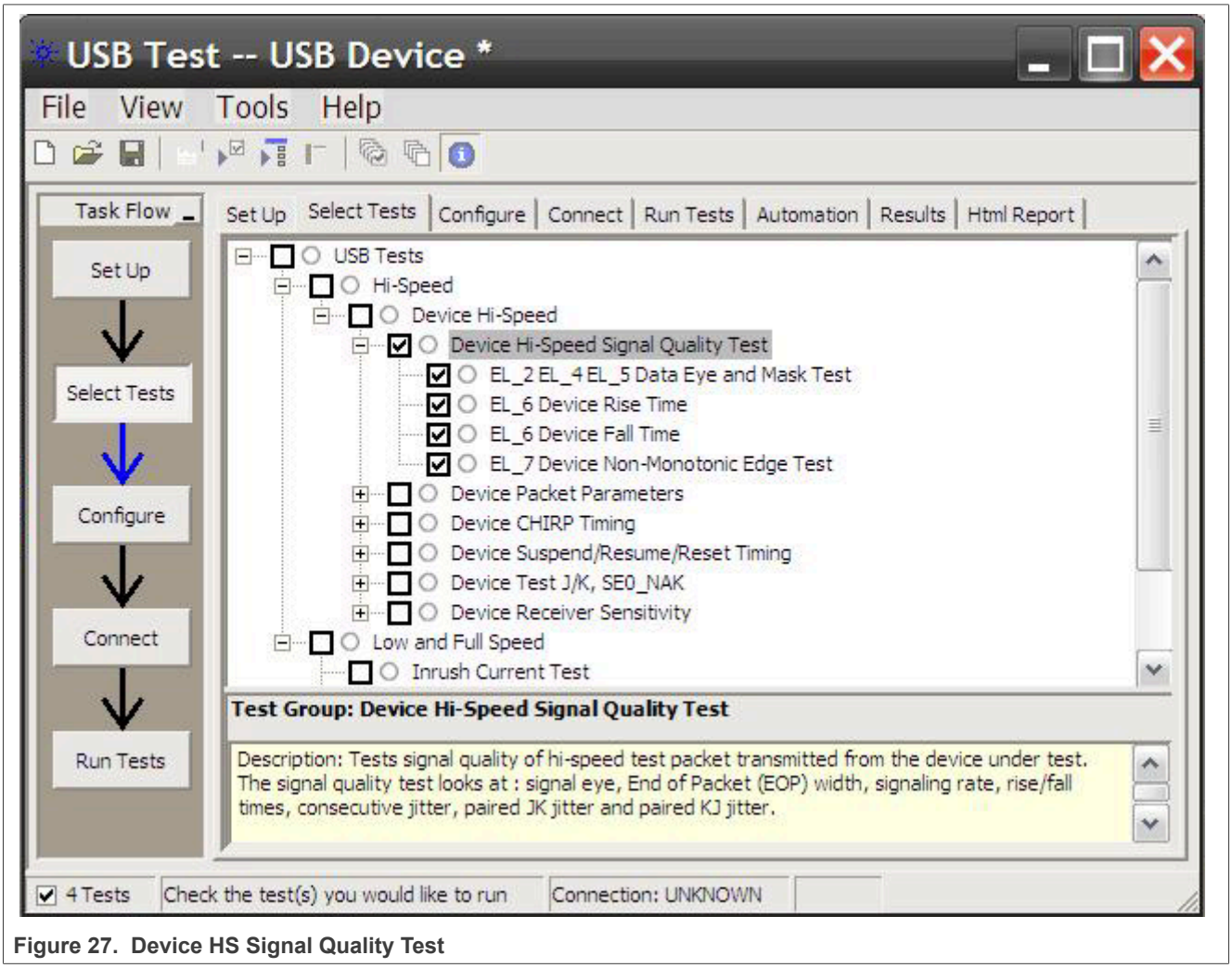

Figure 27. Device HS Signal Quality Test

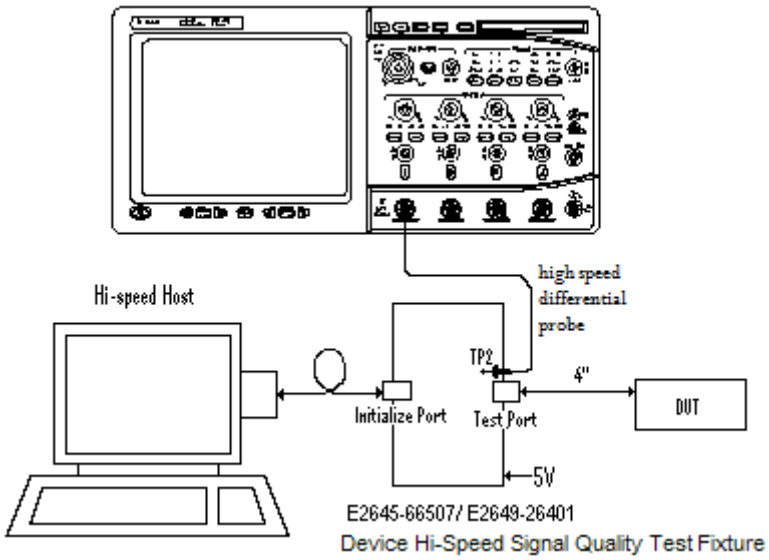

Figure 28. Device HS Signal Quality Test Environment

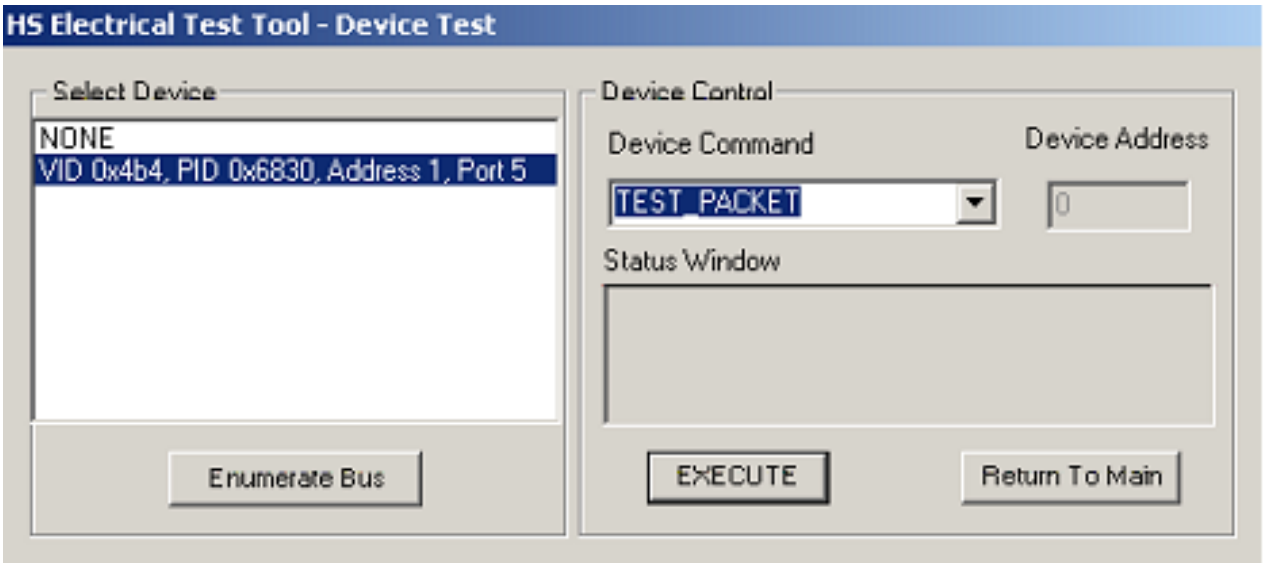

Figure 29. Electrical Test Tool Main Menu

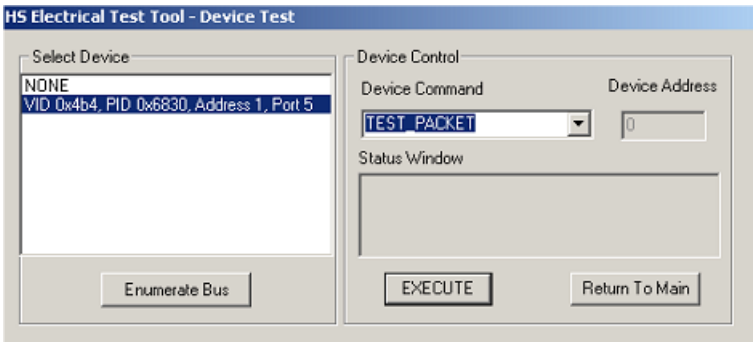

Figure 30. Test_Packet For Eye Diagram Test

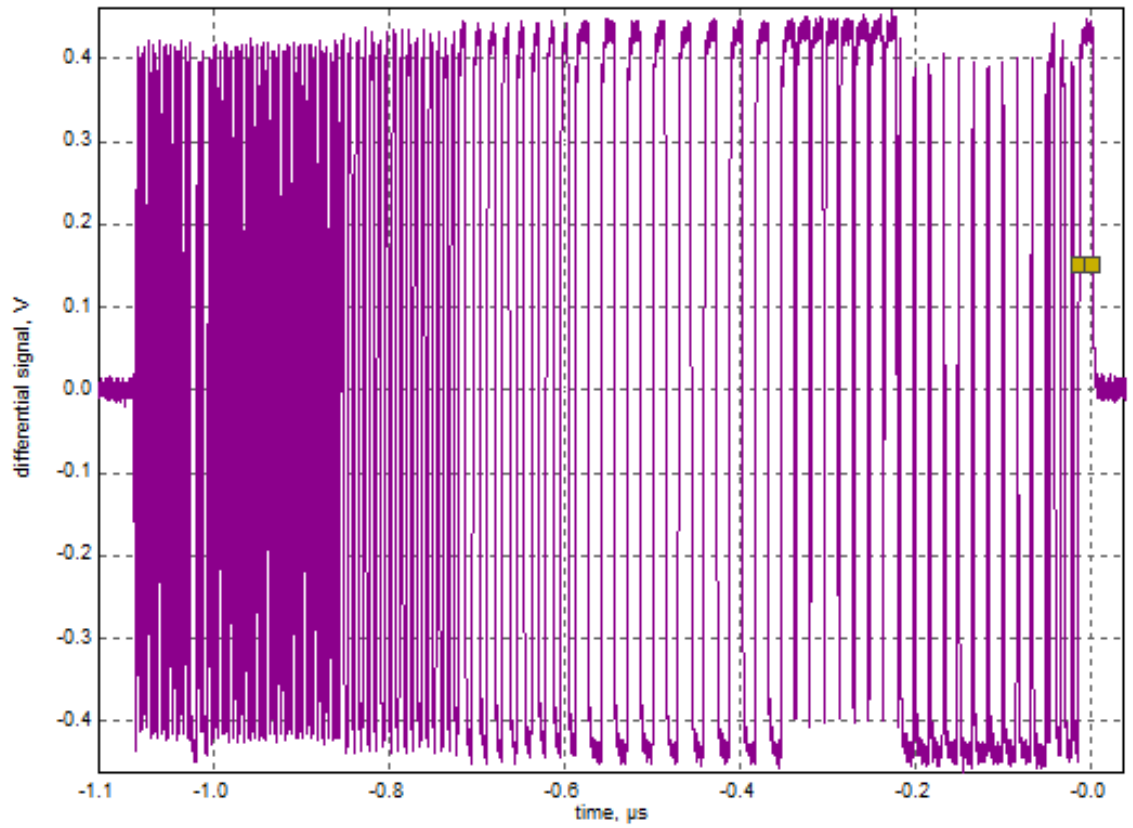

Figure 31. Device HS Test Packet

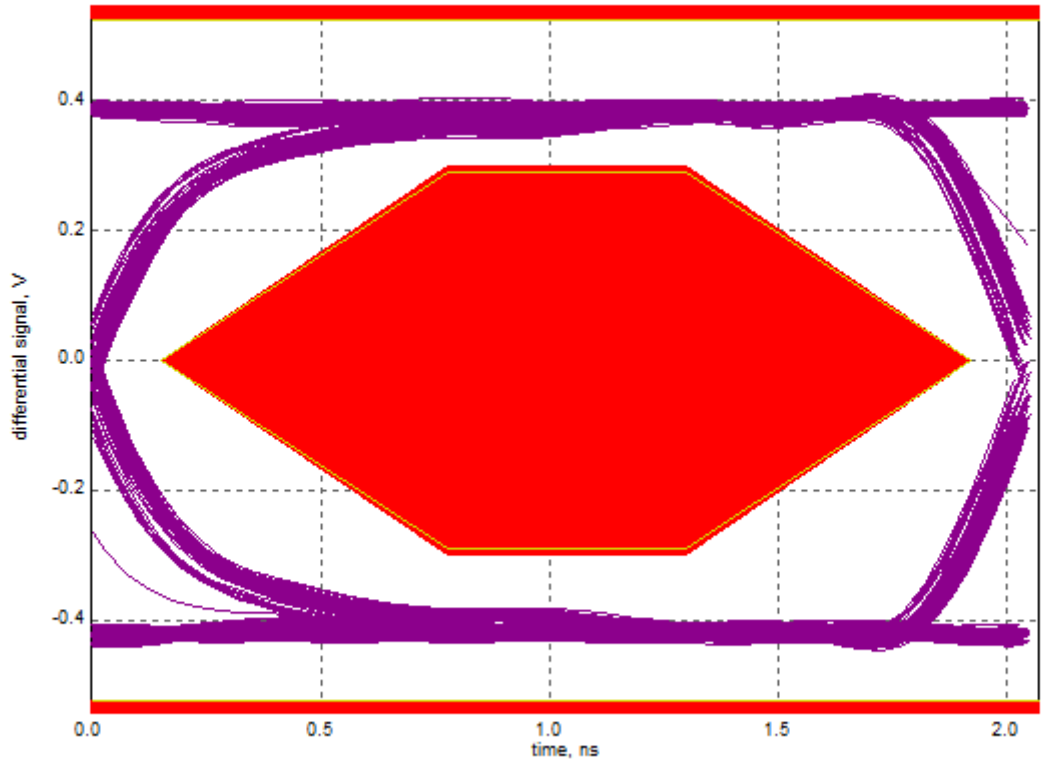

Figure 32. Device HS Eye Diagram

3.2.3 Device packet parameters test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 33, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 28.
   - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the Device Hi-speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
   - Connect the [**INIT PORT**] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
   - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
3. Reboot the device to restore the USB device to normal operation.
4. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Using the oscilloscope, verify the **SOF** (Start of Frame) packets are being transmitted on the port under test. You may need to lower the trigger level to somewhat below 400 mV.

5. Select **Single Step Set Feature** from the Device Command window. Click **EXECUTE** once. Oscilloscope will measure the sync field length (number of bits) of the third (from device) packet (**EL_21**), **EOP** (End of Packet) width (number of bits) of the third packet (**EL_25**), inter-packet gap between the second (from host) and the third (from device in respond to the host's) packets (**EL_22**), as shown in Figure 35 to Figure 37.
6. In the Device Test menu of the HS Electrical Test Tool, click **STEP** once again. This is the second step of the two-step **Single Step Set Feature** command. Oscilloscope will measure the inter-packet gap between the first (from host) and the second (from device in respond to the host's) packets (**EL_22**), as shown in Figure 38.
7. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

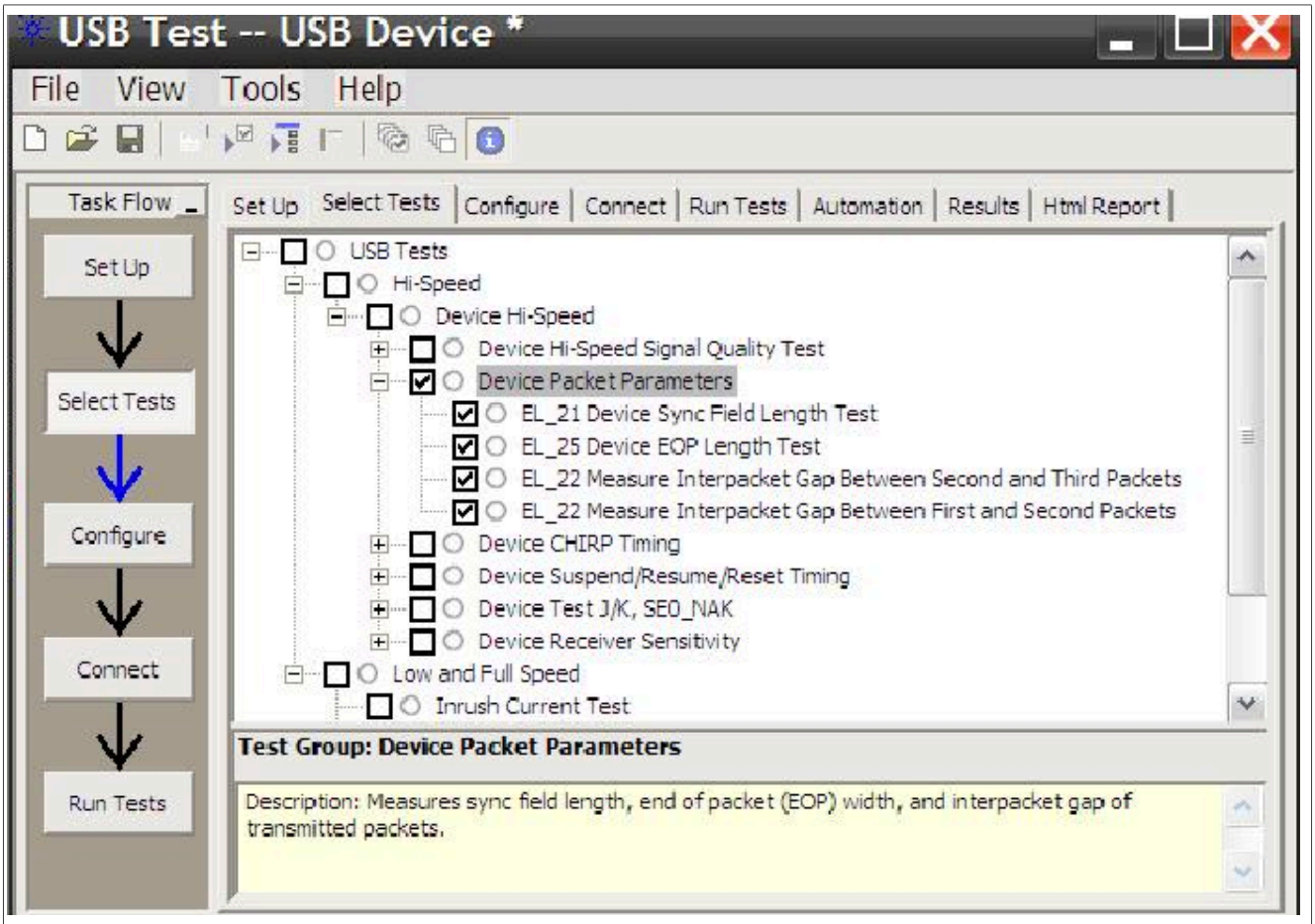

Figure 33. Device HS Packet Parameters Test

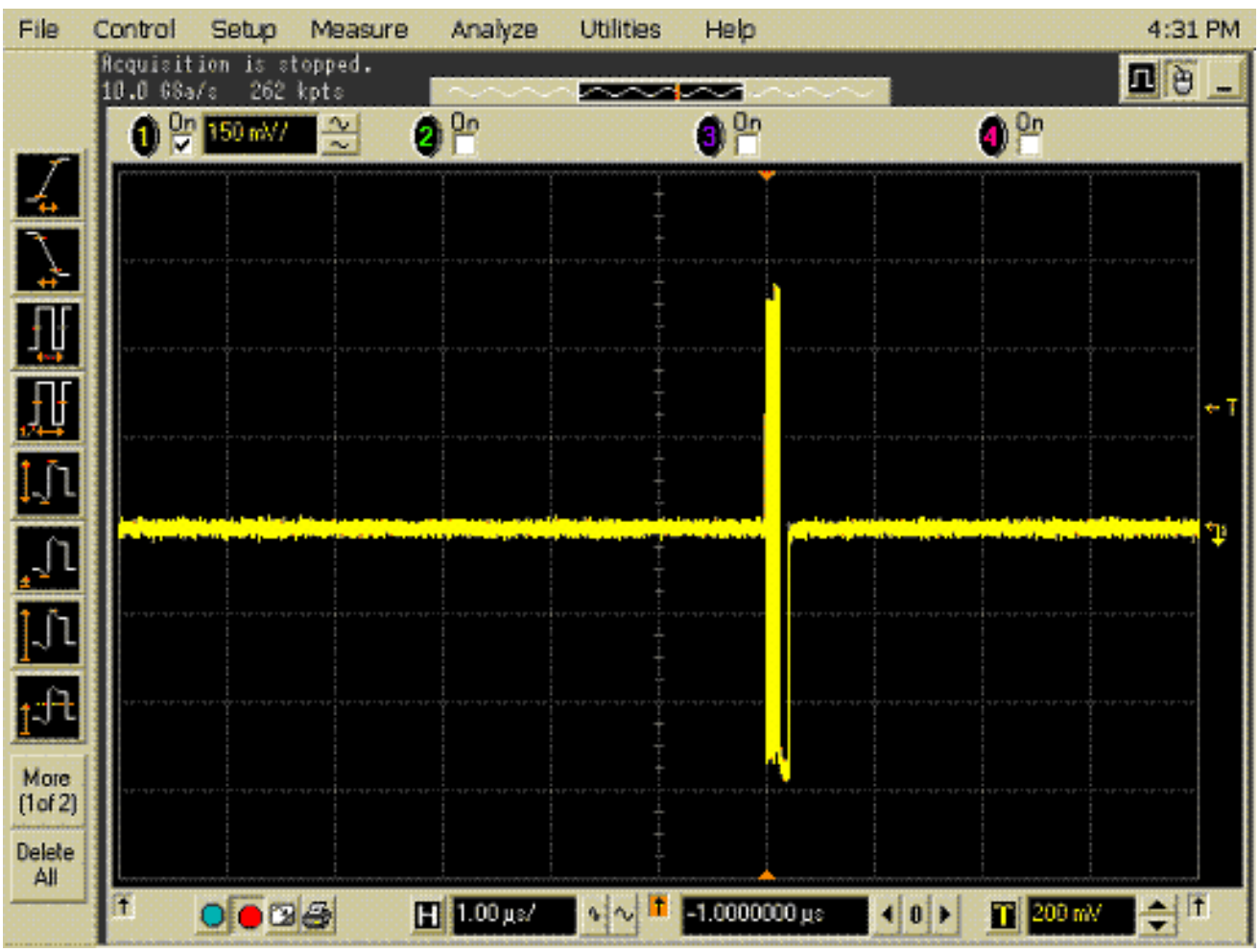

Figure 34. SOF Waveform

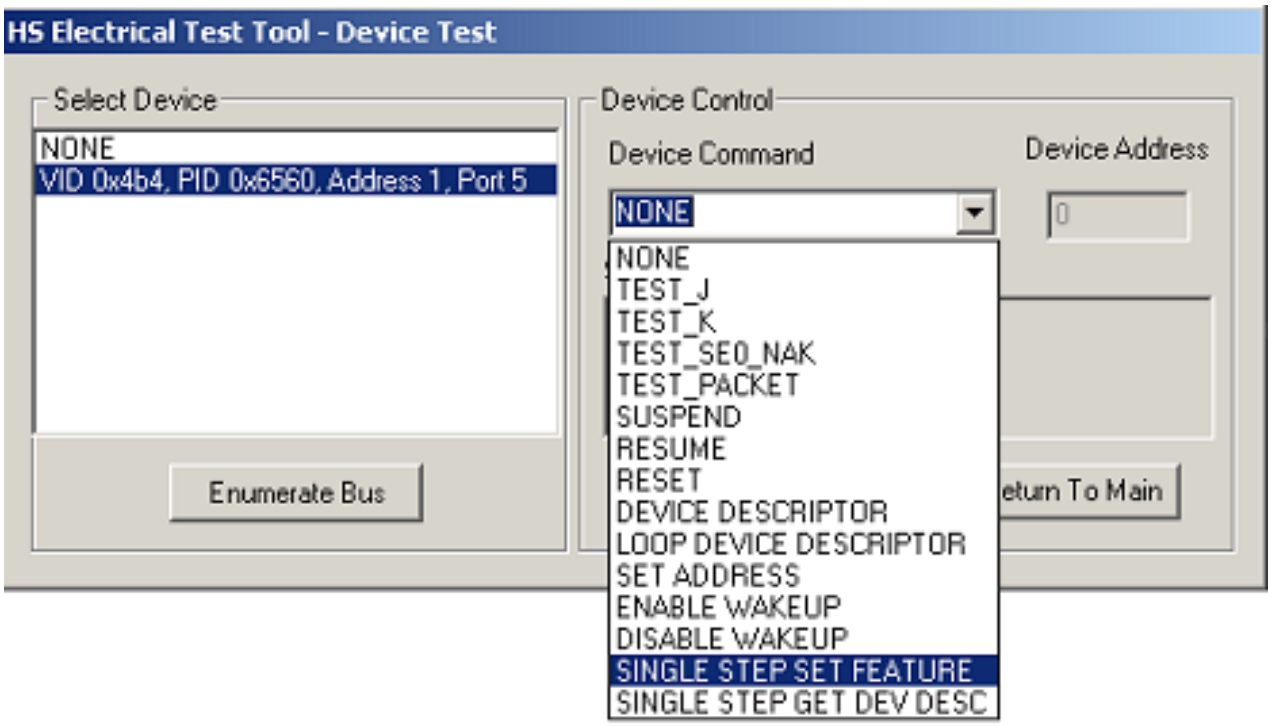

Figure 35. Single Step Set Feature for Packet Parameters Test

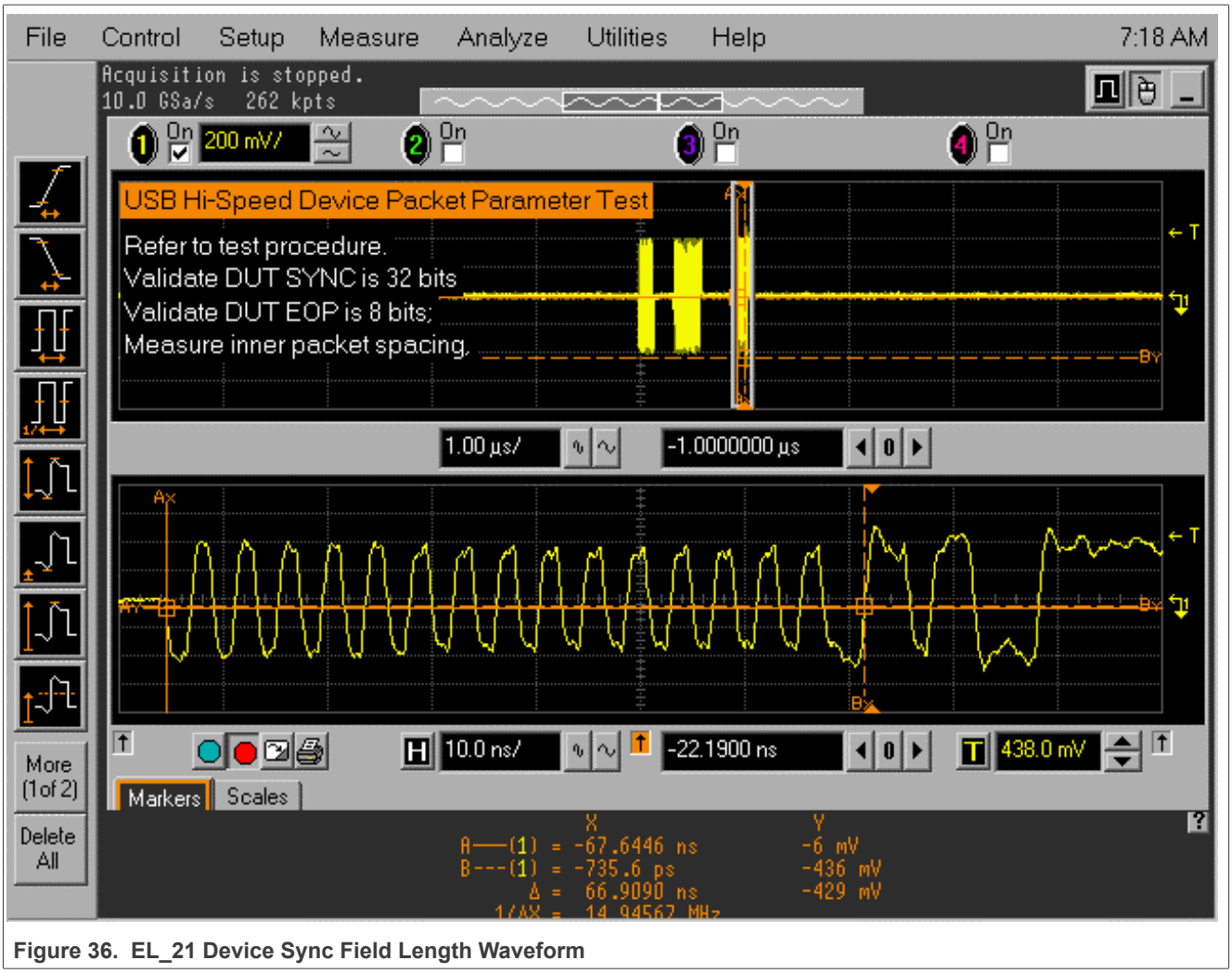

Figure 36. EL_21 Device Sync Field Length Waveform

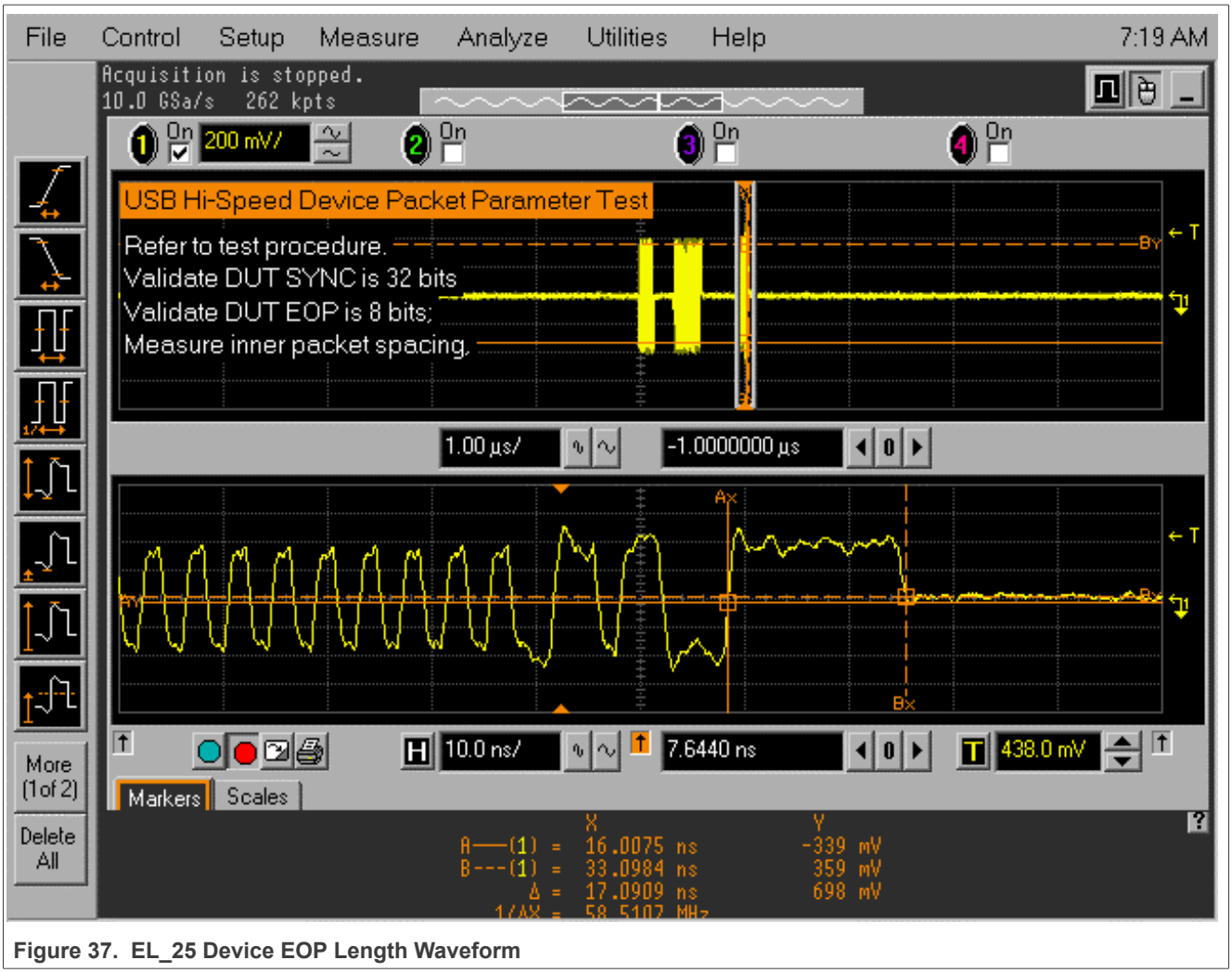

Figure 37. EL_25 Device EOP Length Waveform

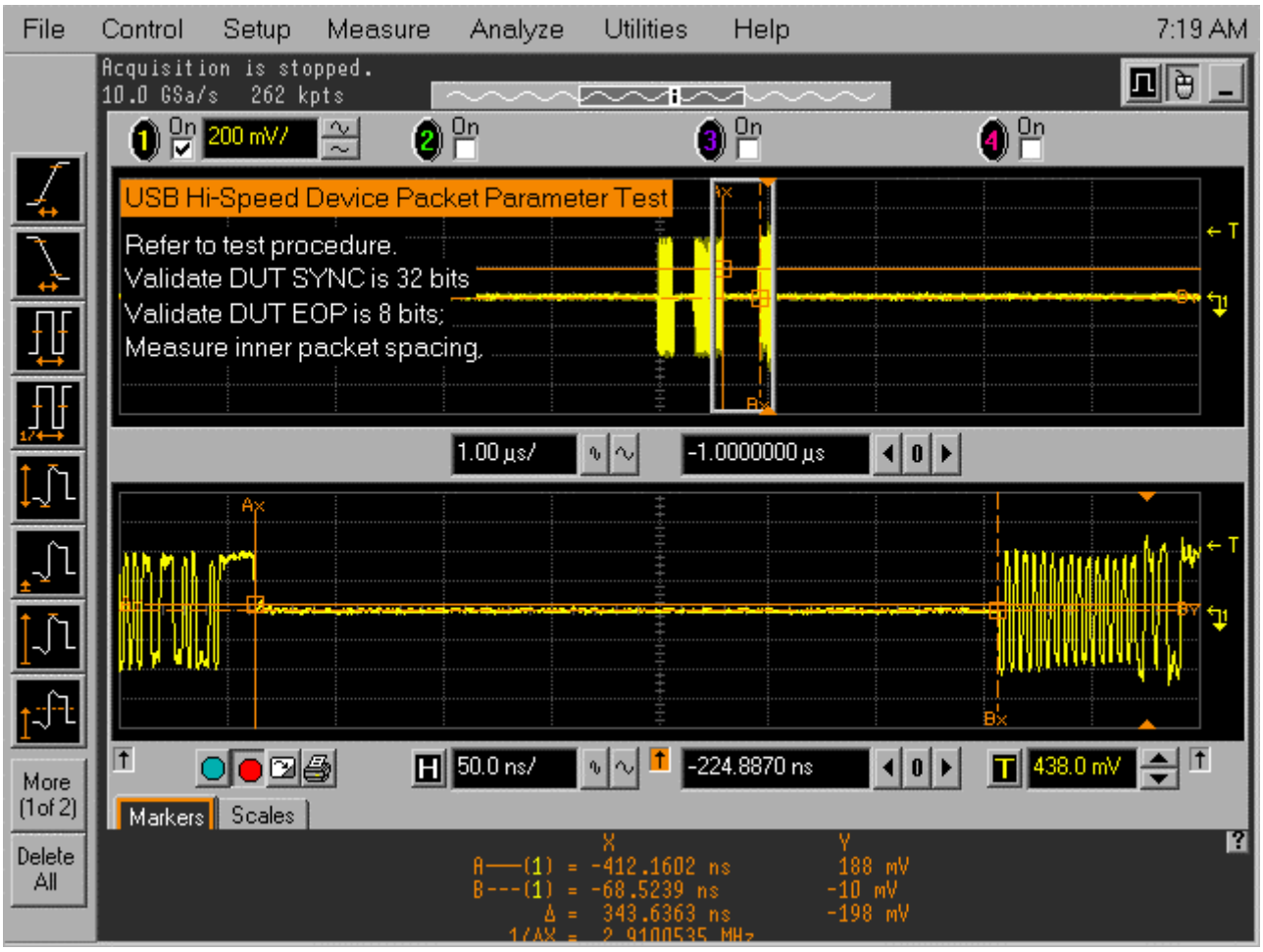

Figure 38. EL_22 Device Inter-packet Gap (Between Second and Third Packets) Waveform

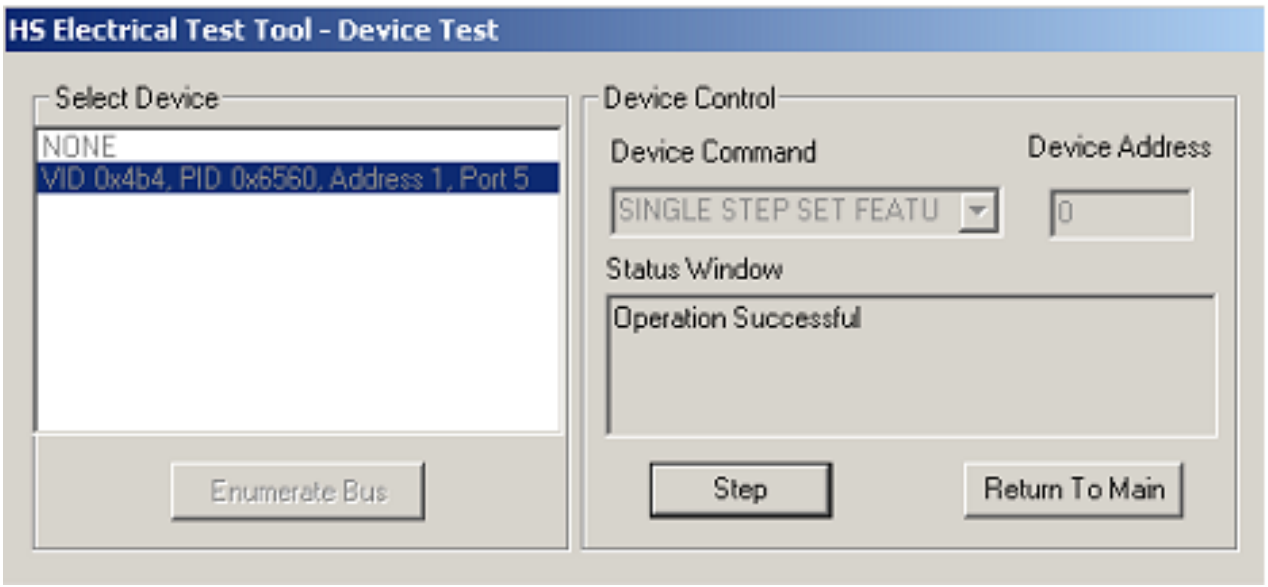

Figure 39. Single Step Set Feature - Second Step

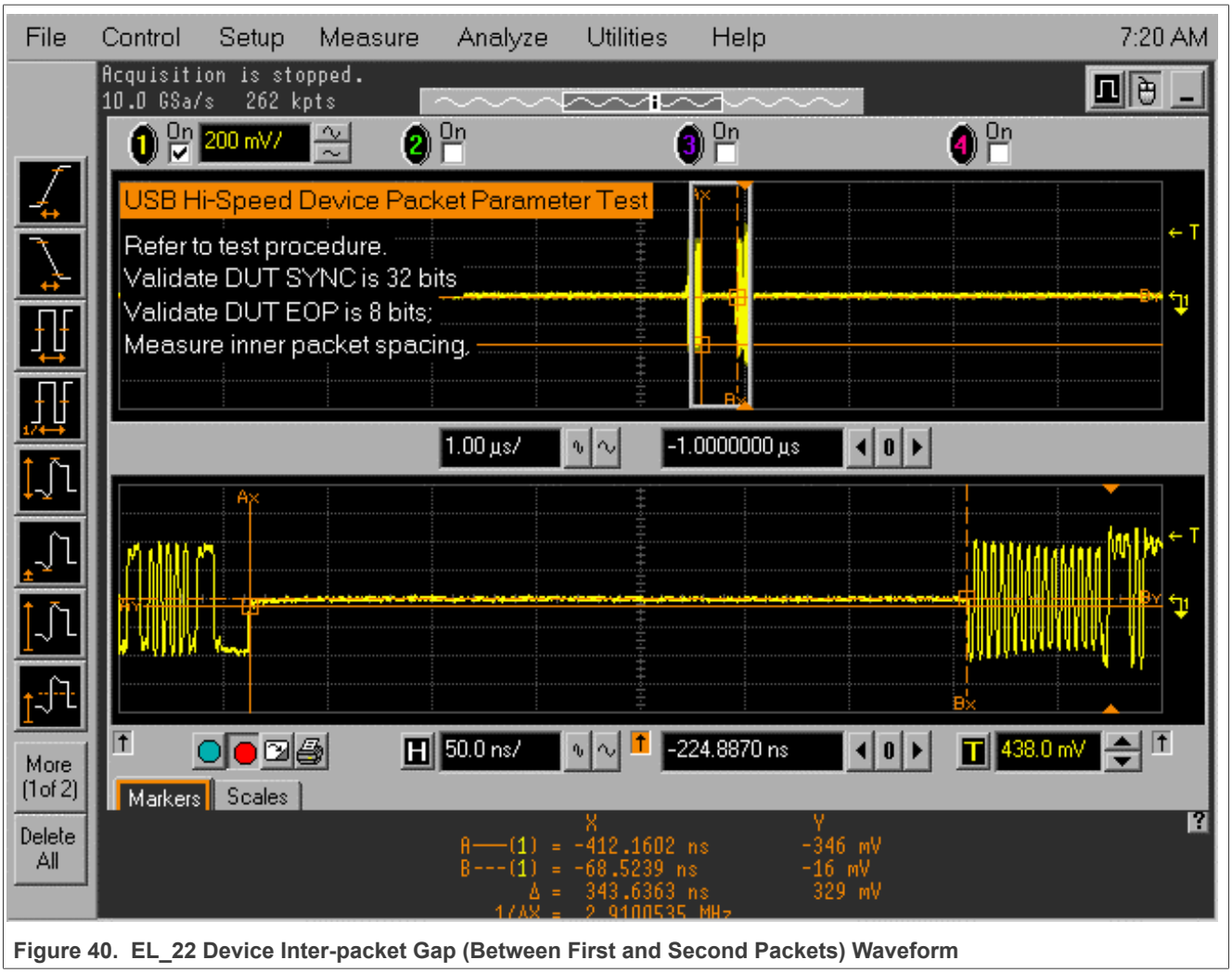

Figure 40. EL_22 Device Inter-packet Gap (Between First and Second Packets) Waveform

3.2.4 Device CHIRP timing test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 41 below, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 42 below.
   - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
   - Connect the [**INIT PORT**] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
   - Attach the single end probes on Channel 2 to D- of TP2, Channel 3 to D+ of TP2.
3. Reboot the device to restore the USB device to normal operation.
4. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Oscilloscope will capture and measure the Chirp handshake as shown in Figure 43 below.

5. When the Testing Complete dialog appears, click **OK.** The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

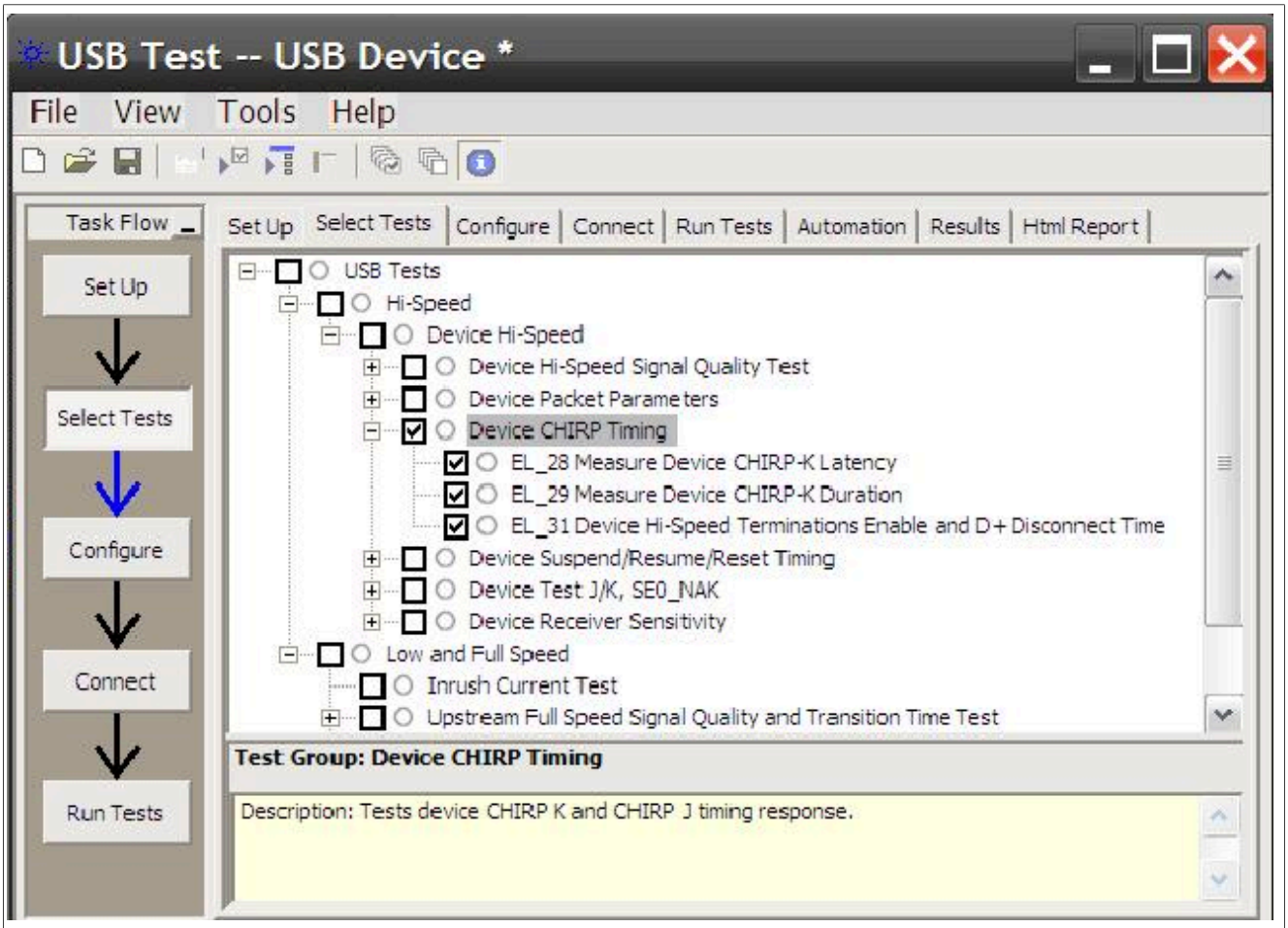

Figure 41. Device Chirp J/K Test

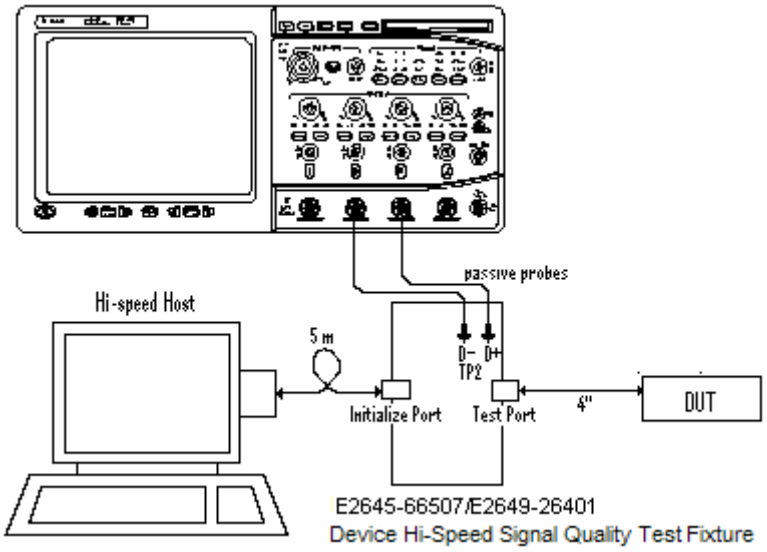

Figure 42. Device CHIRP J/K Test Environment

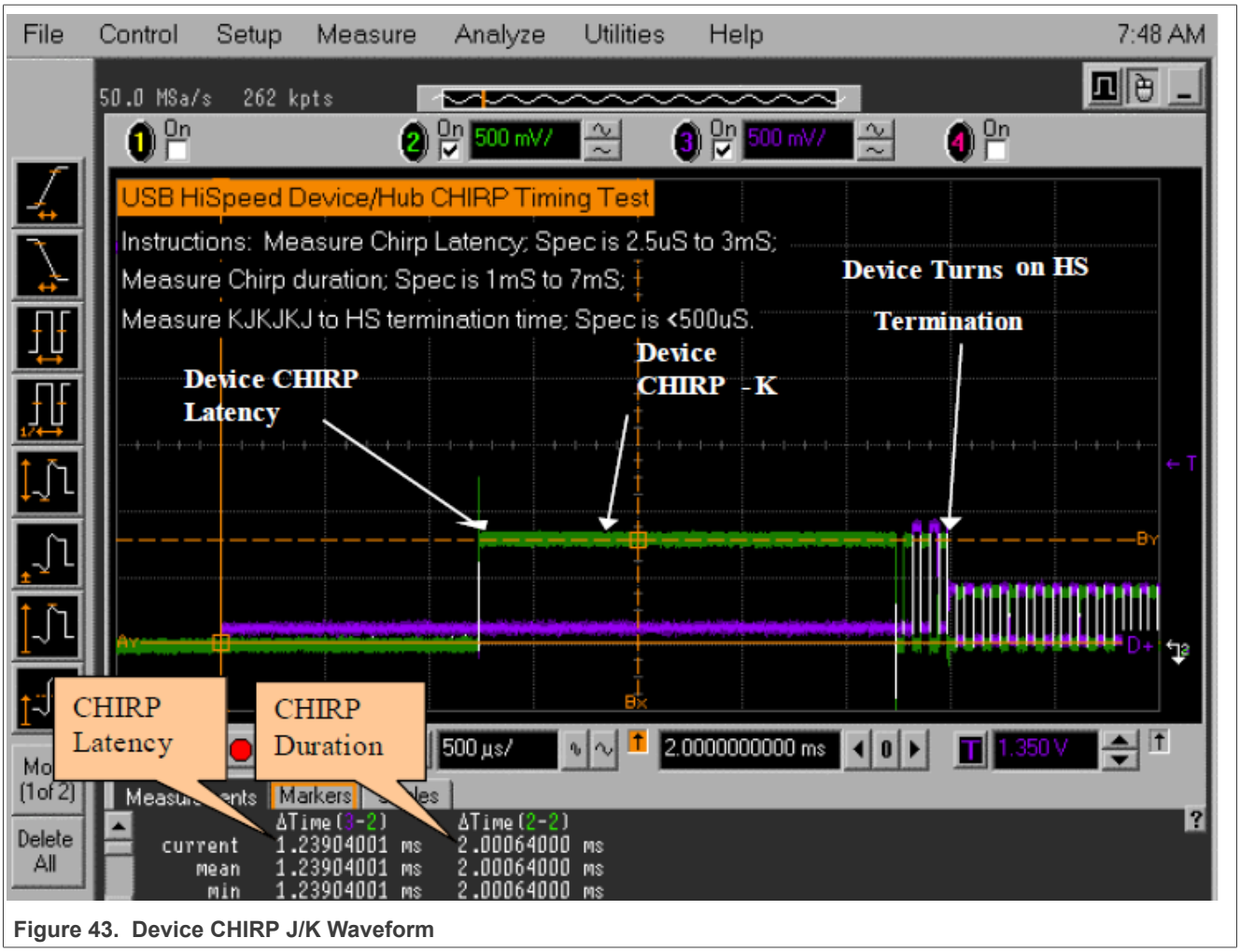

Figure 43. Device CHIRP J/K Waveform

3.2.5 Device Suspend/Reset/Resume timing test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 44 below, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in **Fig3-38** above.
   - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
   - Connect the [**INIT PORT**] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
   - Attach the single end probes on Channel 2 to D- of TP2, Channel 3 to D+ of TP2.
3. Reboot the device to restore the USB device to normal operation.
4. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Choose the right device, Select **SUSPEND** from the Device Command drop down menu, then click **EXECUTE** once to place the device into suspend. The captured suspend transition should appear as in Figure 45 below.
5. Select **RESUME,** then click **EXECUTE** once to resume the device from suspend. The captured resume transition should appear as in Figure 47 below.

6. Select **RESET,** then click **EXECUTE** once to reset the device operating in high speed. The captured transition should appear as Figure 49 below.
7. Select **SUSPEND**, and click **EXECUTE** to place the device into suspend once again. Then select **RESET** and click **EXECUTE** once to reset the device from suspend. The captured transition should appear as Figure 51 below.
8. When the Testing Complete dialog appears, click **OK.** The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

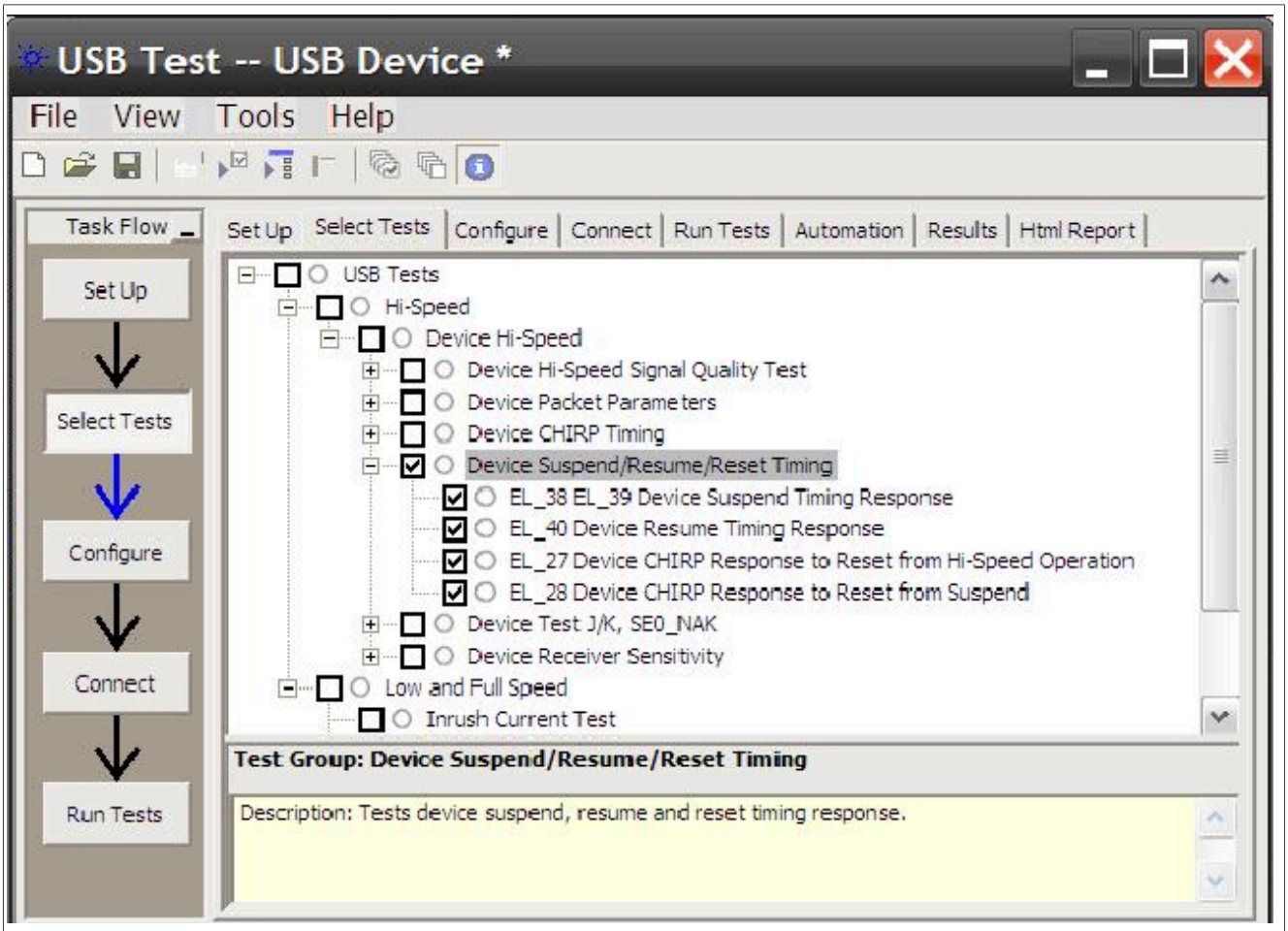

Figure 44. Device Suspend/Reset/Resume Timing Test

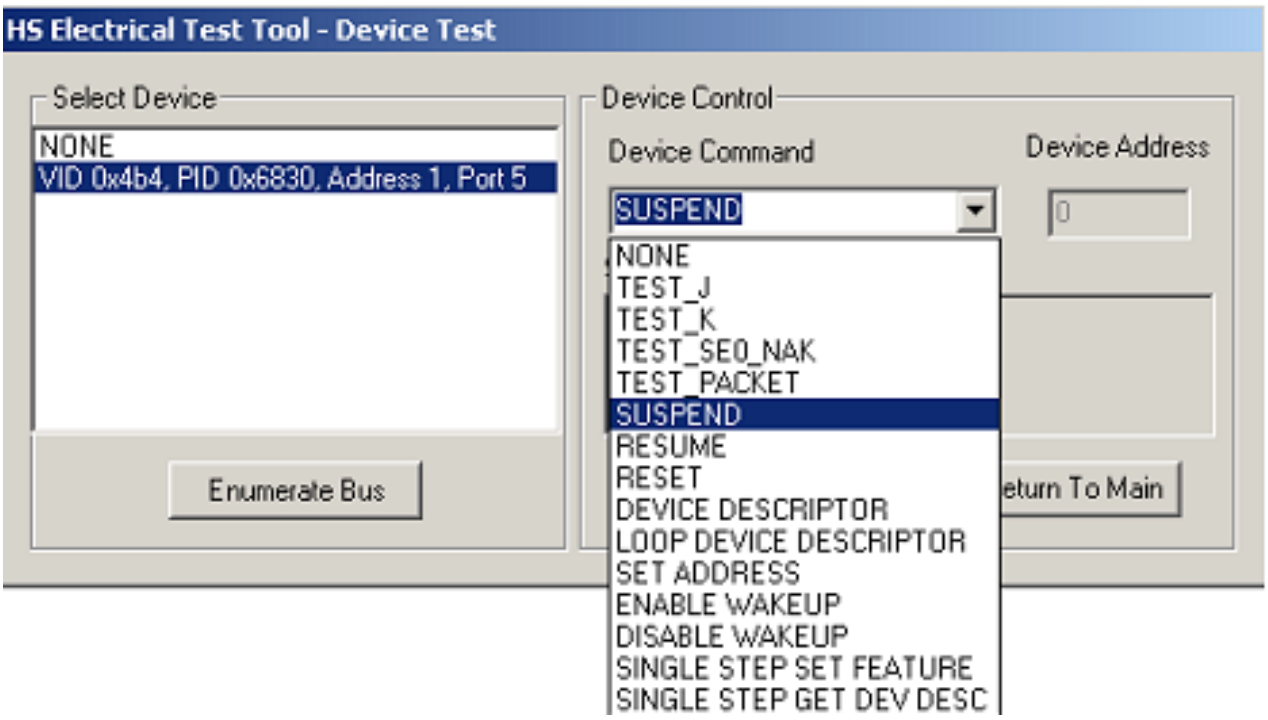

Figure 45. Device Suspend Command

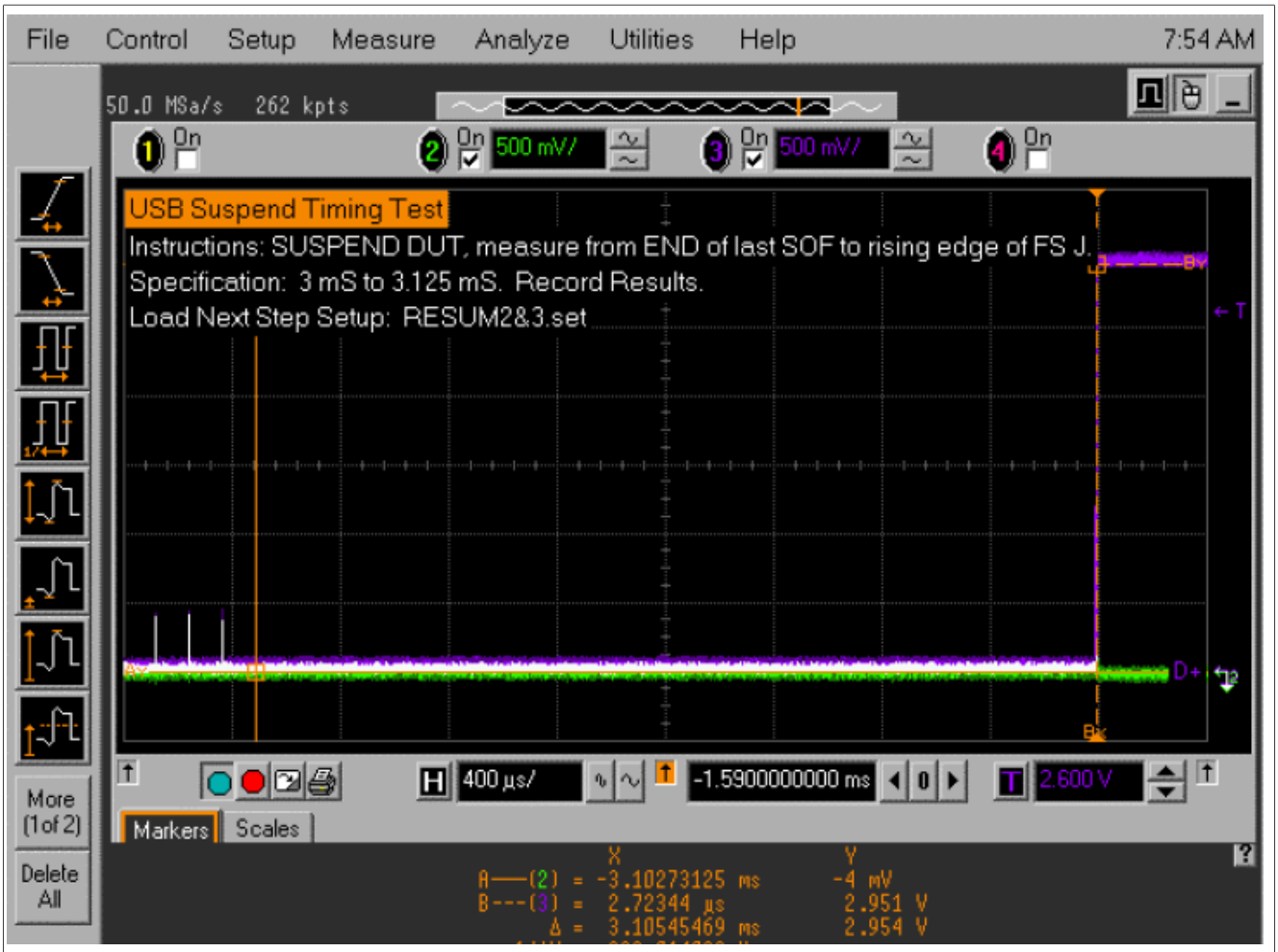

Figure 46. Device Suspend Waveform

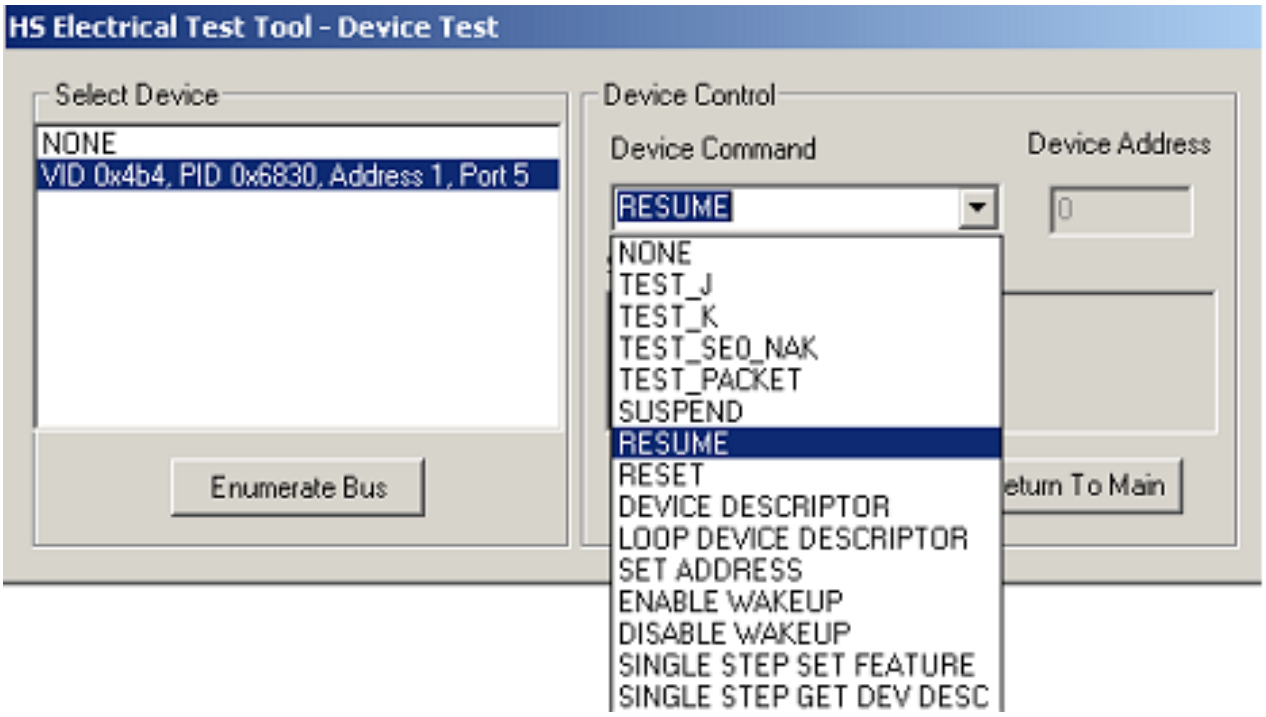

Figure 47. Device Resume Command

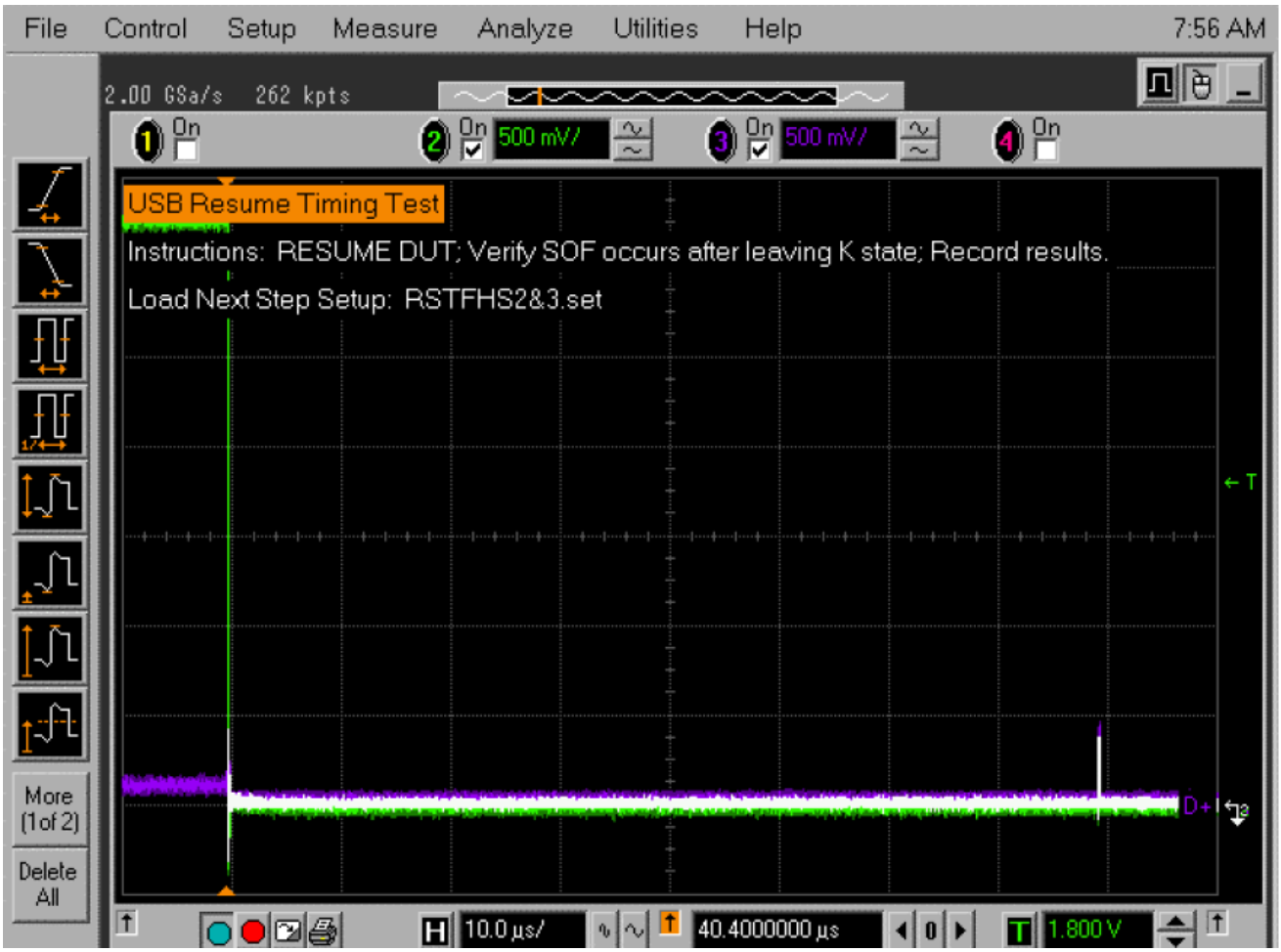

Figure 48. Device Resume Waveform

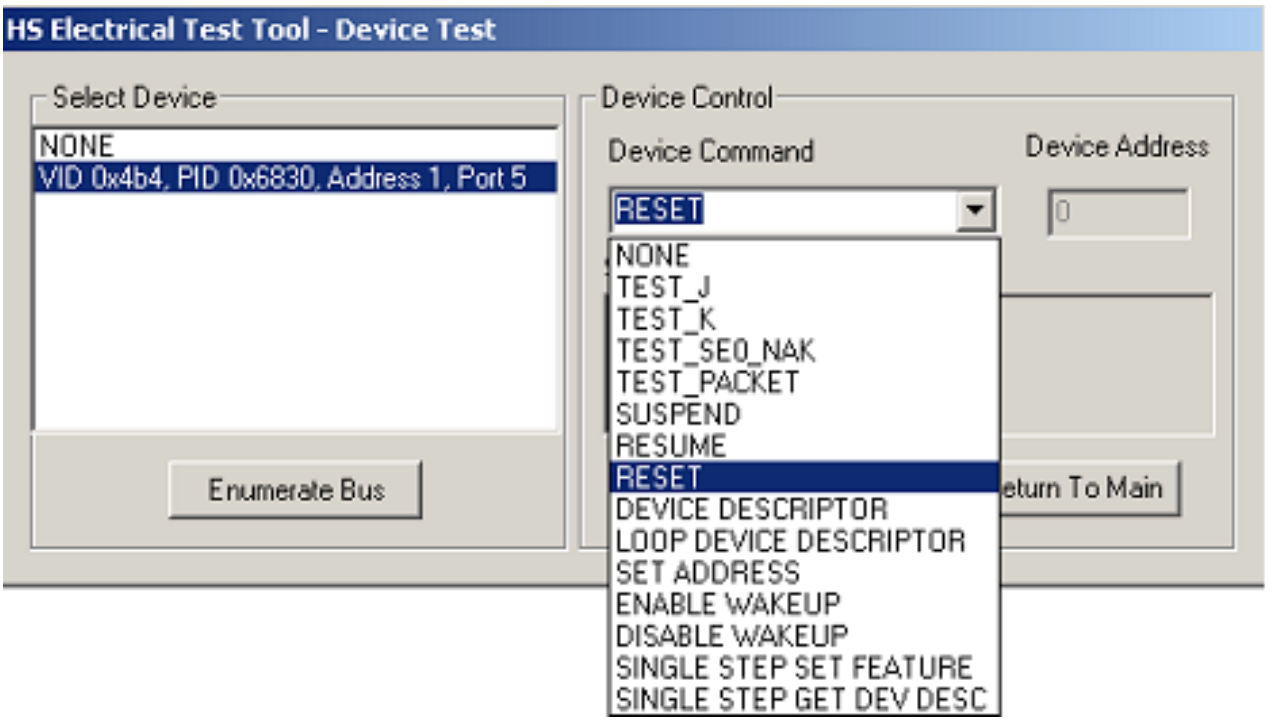

Figure 49. Device Reset Command

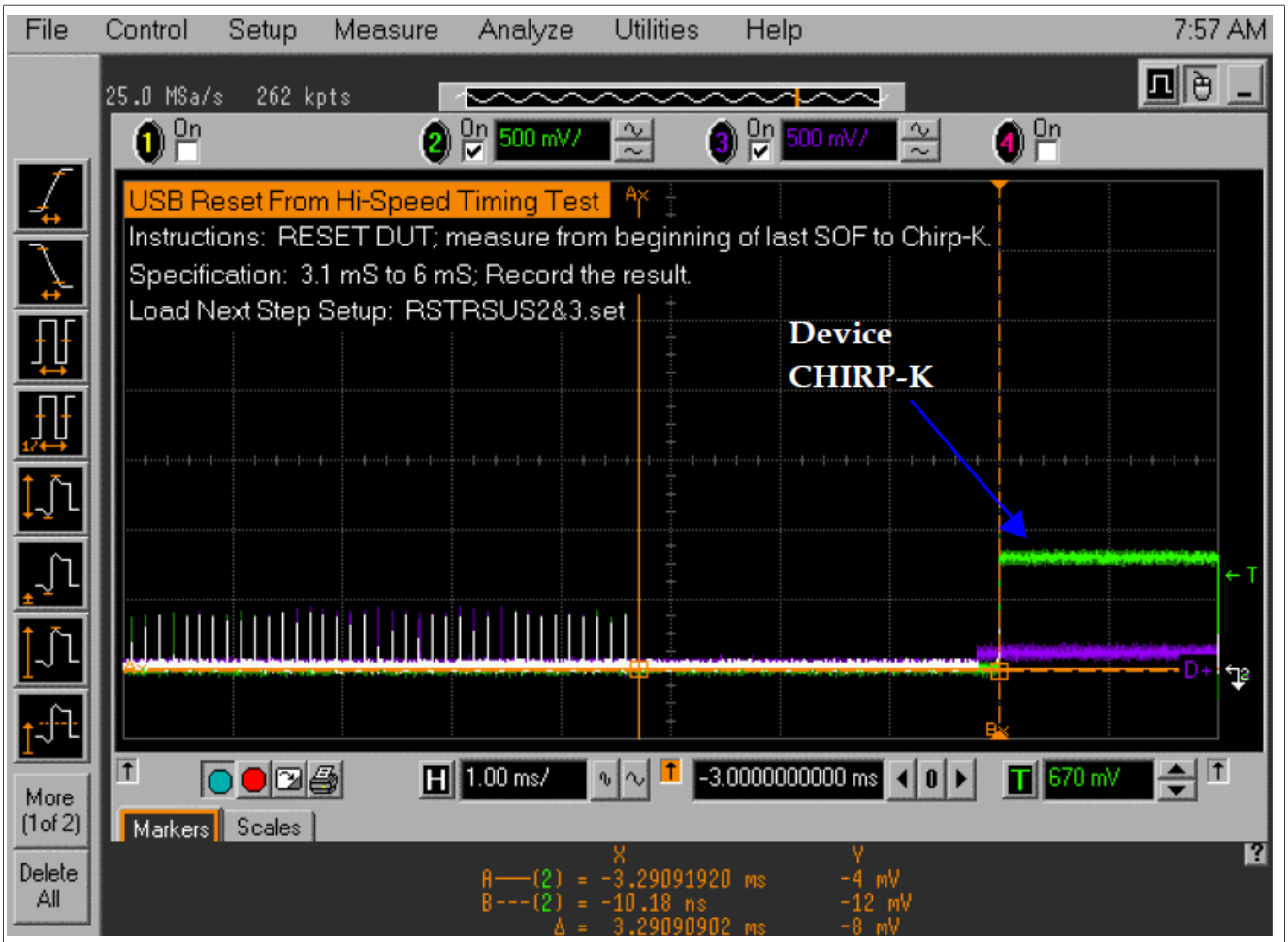

Figure 50. Device Reset from Hi-Speed Waveform

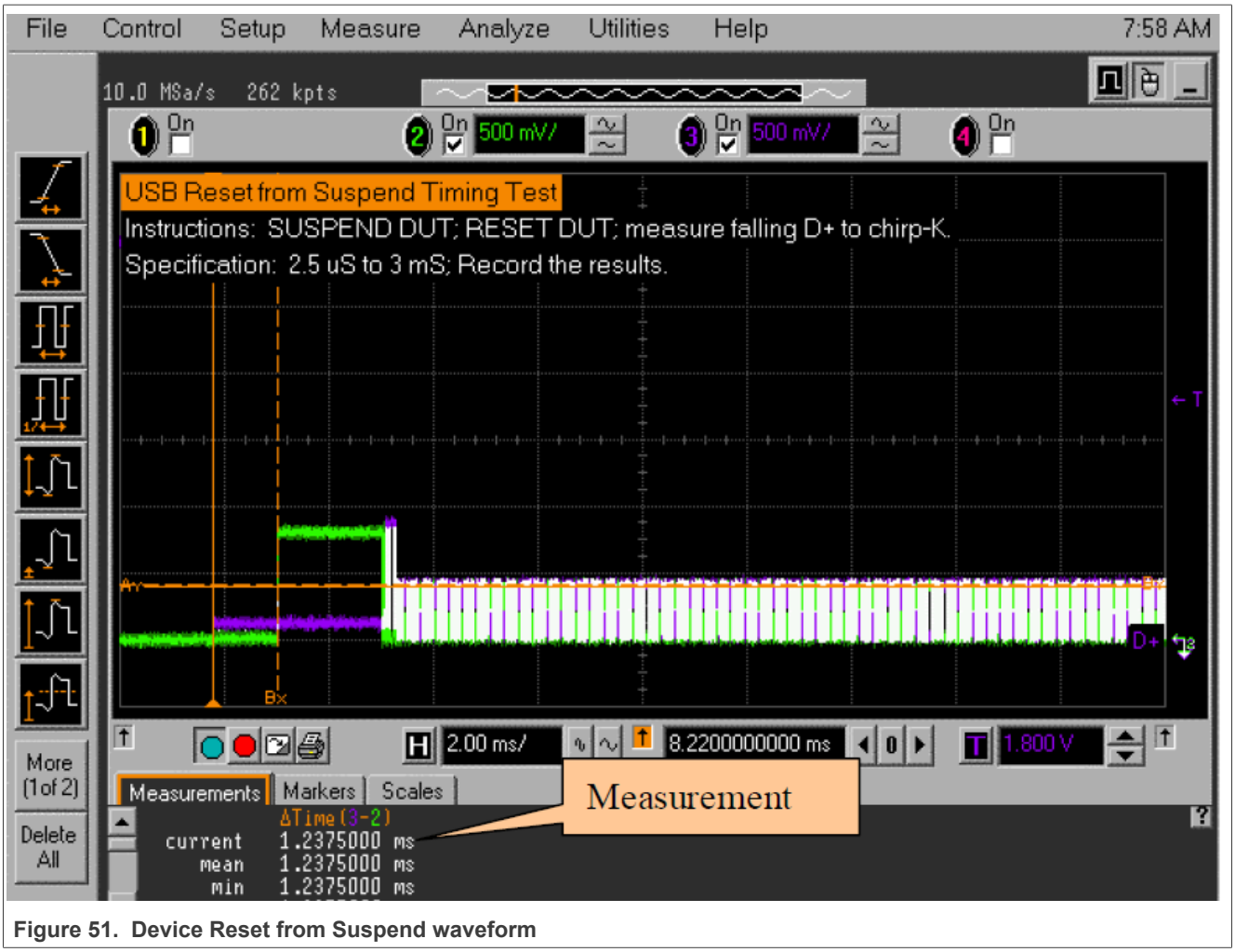

Figure 51. Device Reset from Suspend waveform

3.2.6 Device Test J/K, SE0_NAK test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 52 below.
2. Connect the equipment and test fixture as shown in Figure 53.
   - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
   - Connect the [**INIT PORT**] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
   - Attach the single end probes on Channel 2 to D- of TP2, Channel 3 to D+ of TP2.
3. Reboot the device to restore the USB device to normal operation.
4. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Choose the right device, Select **TEST_J** from the Device Command drop down menu, then click **EXECUTE** once to place the device into TEST_J test mode.
5. Switch the test fixture into the **TEST** position. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.

6. Reboot the device to restore the USB device to normal operation.
7. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Choose the right device, Select **TEST_K** from the Device Command drop down menu, then click **EXECUTE** once to place the device into TEST_K test mode.
8. Switch the test fixture into the **TEST** position. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
9. Reboot the device to restore the USB device to normal operation.
10. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Choose the right device, Select **TEST_SE0_NAK** from the Device Command drop down menu, then click **EXECUTE** once to place the device into TEST_SE0_NAK test mode.
11. Switch the test fixture into the **TEST** position. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
12. When the Testing Complete dialog appears, click **OK.** The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

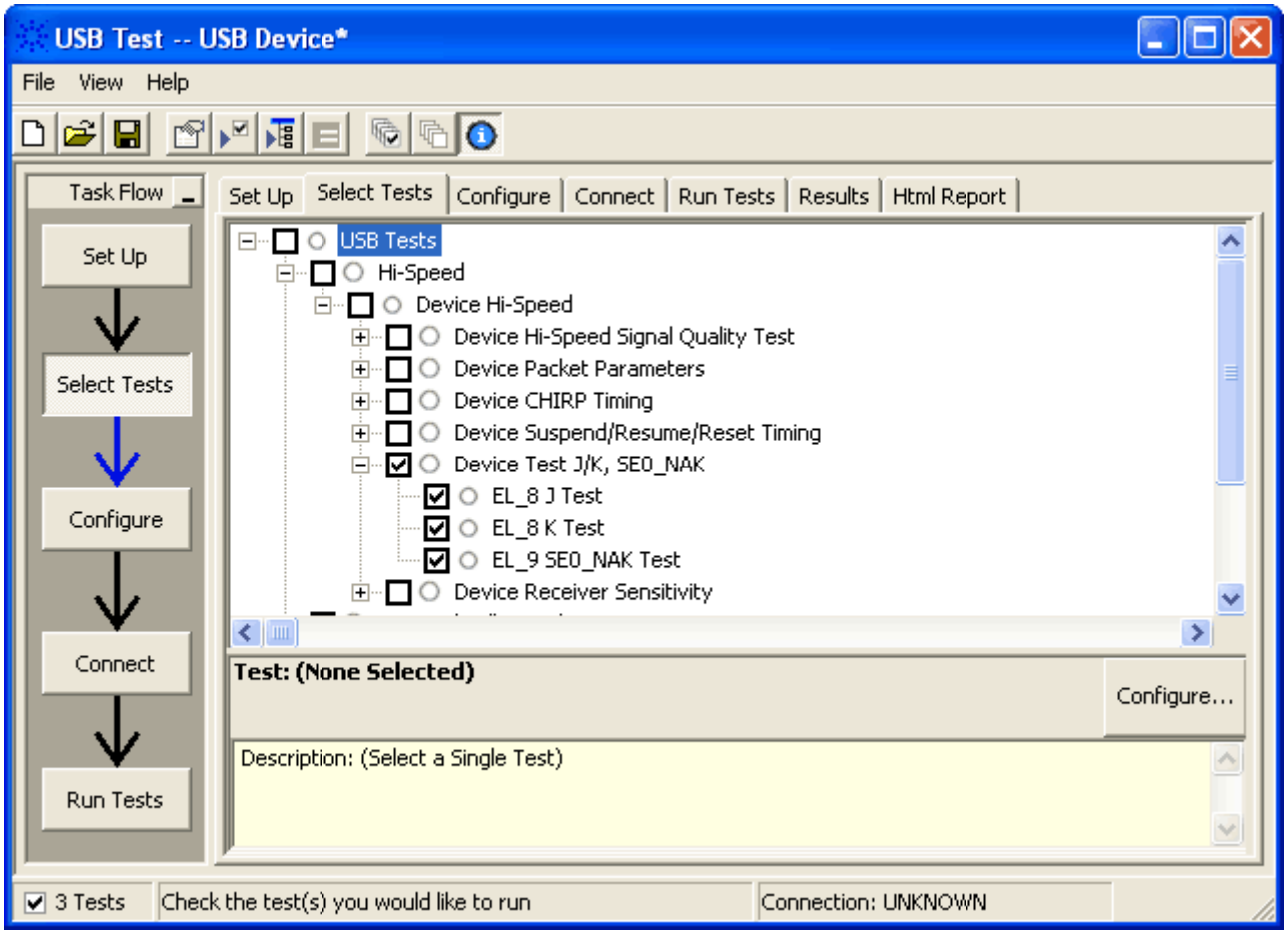

Figure 52. Device Test_J/K, SE0_NAK Test

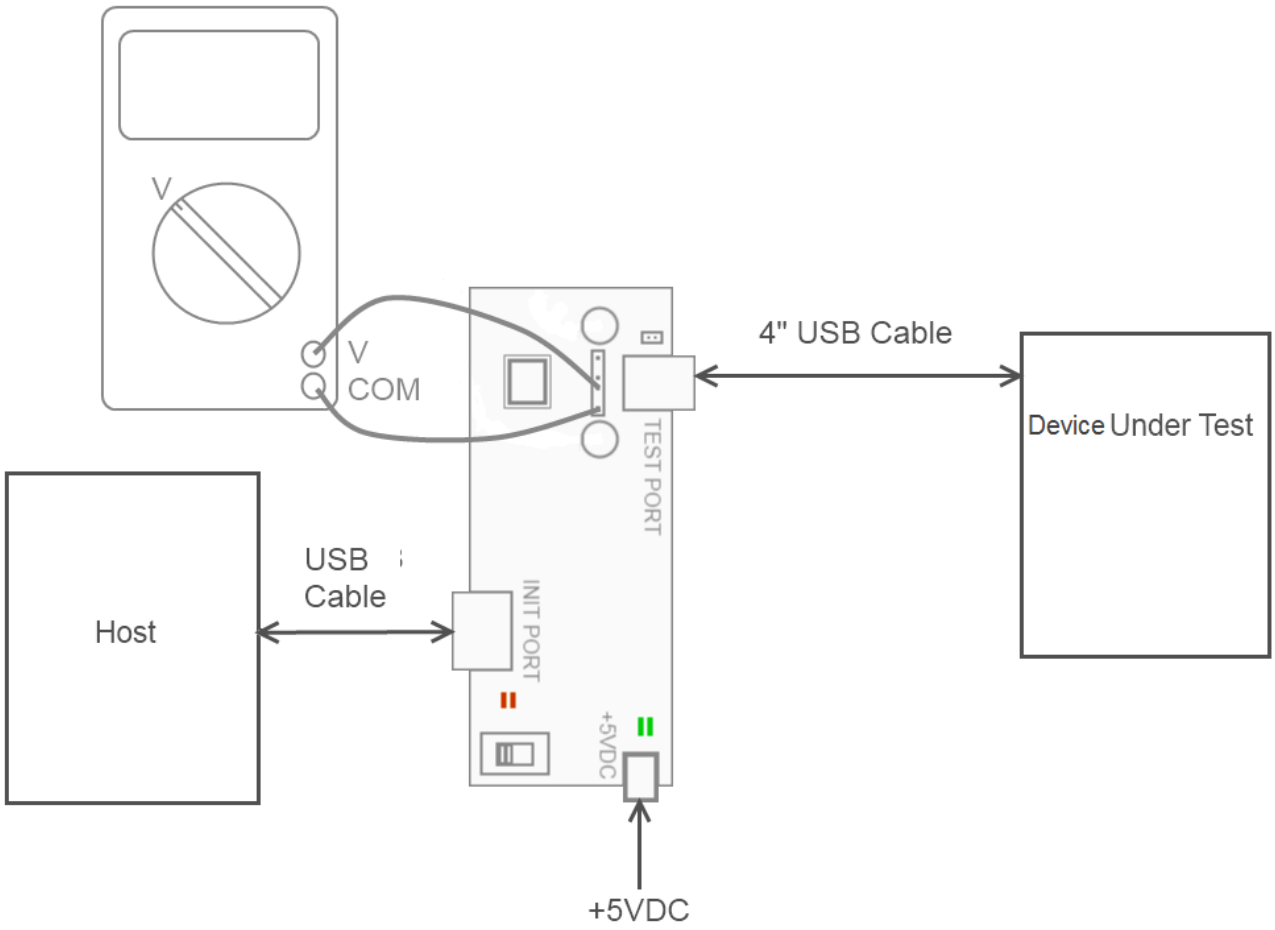

Figure 53. Device Test_J/K, SE0_NAK Test Environment

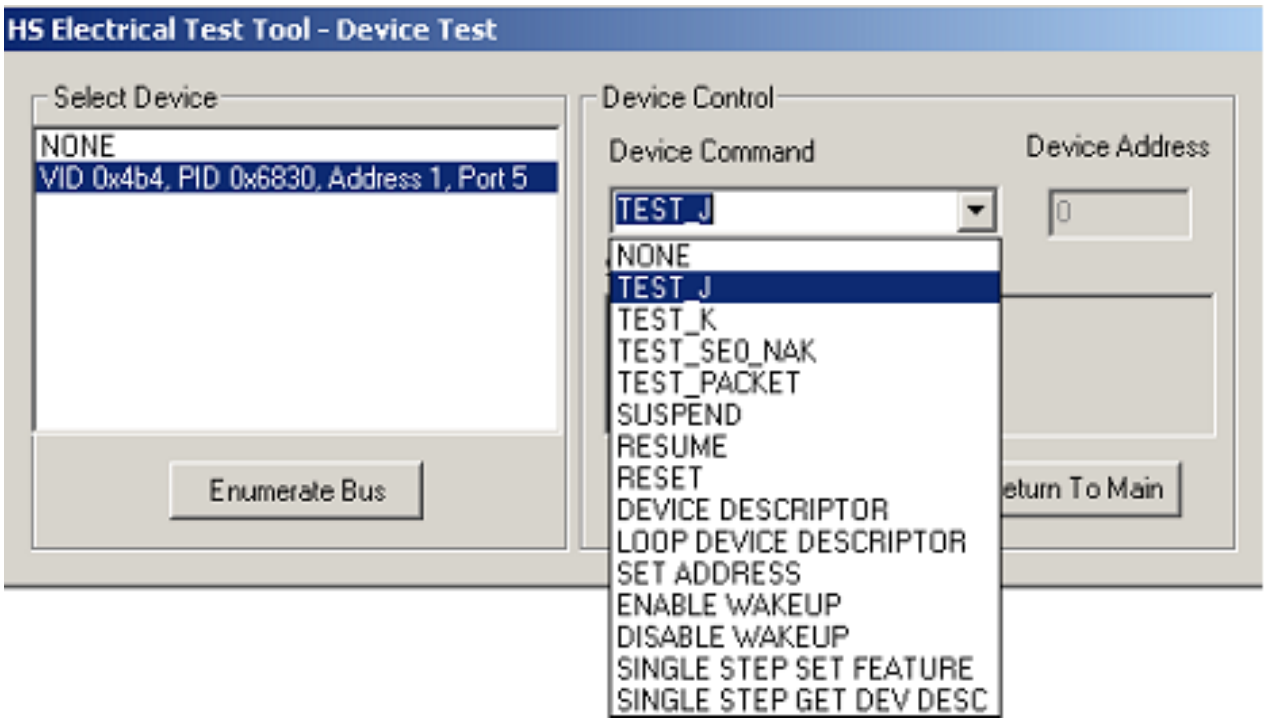

Figure 54. Device Test_J Command

Table 11. Host Drop Test Record

Test Mode	D+ Voltage(mV)	D- Voltage(mV)	Expected Value
J	415	4	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV
K	4	417	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
SE0_NAK	1	1	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV

3.2.7 Device receiver sensitivity test

Receiver Sensitivity and Squelch measurements are supposed to be made at the upstream port pins as defined in the USB 2.0 Specification.

A hi-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12-bit times. When all packets are NAK by the device this test (EL_18) is considered to have passed. In Section 7.1.7.2, it requires squelch (EL_16) to occur below 100 mV magnitude. So no packets must be acknowledged between -100 mV and +100 mV. Full squelch may occur at higher voltages, but it is mandatory between -100 mV and +100 mV.

Receiver sensitivity requires all packets to be reliably received down to 150 mV magnitude. Packets may be received at lower voltages, but it is mandatory at levels above 150 mV magnitude. This measurement is to be made at the upstream pins but the test fixture does not allow this. Therefore, the USB-IF requires packets to be reliably received at levels above 200 mV (50 mV waiver to compensate for the voltage drop) for EL_17. Packets can, but do not need to be, received between -200 mV and +200 mV.

See the detailed explanation of Device Receiver Sensitivity, you can visit follow link: http://compliance.usb.org/index.asp?UpdateFile=Electrical&Format=Standard#3

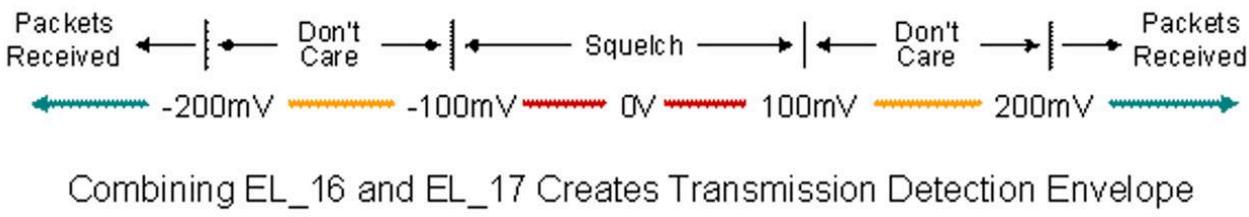

Figure 55. Device Sensitivity Detection Envelope

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 56 below, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 57 below.
   - Attach the 5 V power supply to J5 of the Device Hi-Speed signal quality test fixture (E2649- 66401). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the Device Hi- speed Signal Quality test fixture into the upstream facing port of the DUT, using the 4" USB cable.
   - Connect the [**INIT PORT**] of the test fixture to a Hi-Speed capable port of the Test Bed Computer with a 5 m USB cable.
   - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
3. Connect the 81130A pulse generator to the oscilloscope using the 82357A USB/GPIB Interface.
   - If you choose to use the Agilent 81130A Pulse/Pattern Generator, connect the 8493C 6 dB attenuators to OUTPUT1 and OUTPUT2 of Agilent 81130A Pulse/Pattern Generator.
4. Connect OUTPUT1 to SMA1 (D+) of the E2649- 66403 Device Receiver Sensitivity test fixture using the 8120- 4948 SMA cables.
5. Connect OUTPUT2 to SMA2 (D-) of the E2649- 66403 Device Receiver Sensitivity test fixture using the 8120- 4948 SMA cables.
6. On the 81130A, select the **MEMCARD** soft key. If **MEMCARD** is not in the menu, press the **MORE** key until **MEMCARD** is displayed. The content of the memory appears on the screen. Use the cursor and the rotary knob to select the **MIN_ADD1.ST0** setup file. Move the cursor to **Perform Operation** and turn the knob to select **Recall**]. Then press the **ENTER** key to load it. It generates **IN** packets (of compliant amplitude) with a 12-bit SYNC field packet pattern.
7. Reboot the device to restore the USB device to normal operation.
8. Click **Enumerate Bus** on the menu of the HS Electrical Test Tool. Choose the right device, Select **TEST_SE0_NAK** from the Device Command drop down menu, then click **EXECUTE** once to place the device into TEST_SE0_NAK test mode.
9. Place the test fixture Test Switch (S1) into the **TEST** position. It switches the data generator in place of the host controller. The data generator emulates the **IN** packets from the host controller.
10. Verify that all packets from the data generator are **NAK** ’d by the port under test as shown in Figure 58 below. Record the Pass/Fail in **EL_18**.
11. On the 81130A, use the cursor and the rotary knob to select the **IN_ADD1.ST0** setup file. Move the cursor to **Perform Operation** and turn the knob to select [**Recall**]. Then press the **ENTER** key to load it. It generates **IN** packets (of compliant amplitude) with a 32-bit SYNC field packet pattern.

12. Verify that all packets from the data generator are **NAK** ’d by the port under test as shown in Figure 60 below.
13. Adjust the output level of each channel as follows:
    - Select the [**LEVELS**] soft key, then move the cursor to the numeric value for [High] voltage value.
    - Adjust the output level with the rotary knob or using the number keys while monitoring the actual level on the oscilloscope.
    - Use the cursor arrow buttons to select the channel to change.
    - Reduce the amplitude of the data generator packets in 20 mV steps (on the generator before the attenuator) while monitoring the **NAK** response from the device on the oscilloscope. The adjustment should be made to both channels such that OUTPUT1 and OUTPUT2 are matched, as indicated by the data generator readout.
    - Reduce the amplitude until the **NAK** packets begins to become intermittent.
    - Increase the amplitude such that the **NAK** packet is not intermittent.
    - It is just above the minimum receiver sensitivity levels before squelch.
14. Using the oscilloscope markers to measure the packet amplitude. Read out the [Ay] and [By] values and record the measurement in **EL_17.**
15. Now further reduce the amplitude of the packet from the data generator in small steps.
    - Maintain the balance between OUTPUT1 and OUTPUT2 until the receiver just ceases to respond with a **NAK.**
    - This is the squelch level of the receiver.
16. Measure the packet amplitude. Read out the [Ay] and [By] values and record the measurement in **EL_16.**
17. When the Testing Complete dialog appears, click **OK.** The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

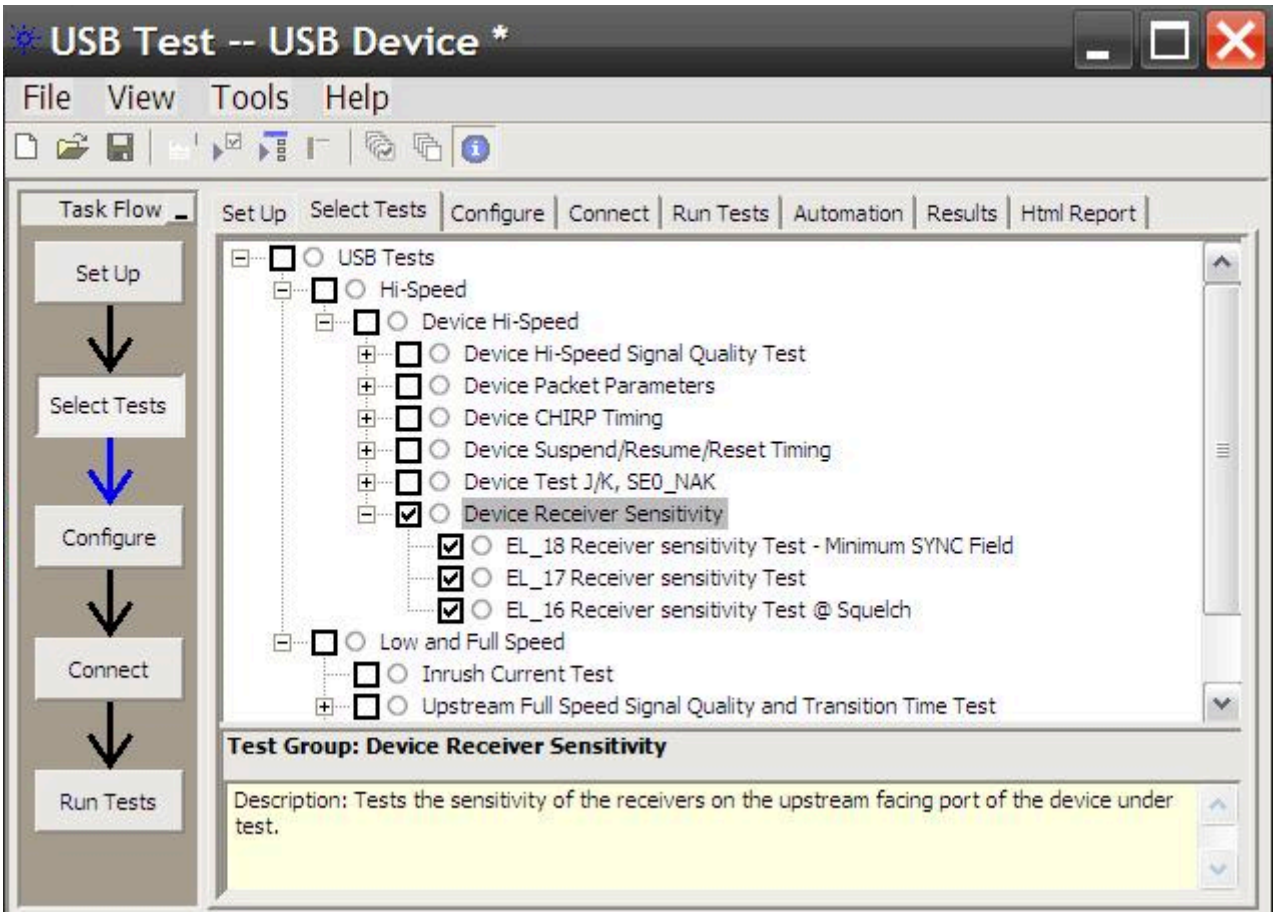

Figure 56. Device Receiver Sensitivity Test

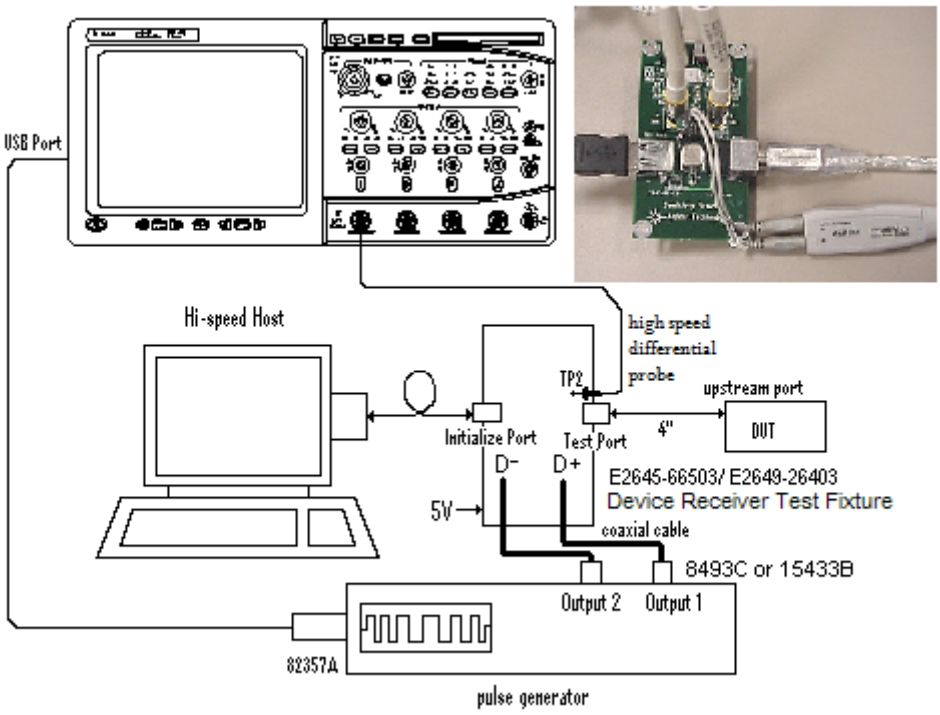

Figure 57. Device Receiver Sensitivity Test Environment

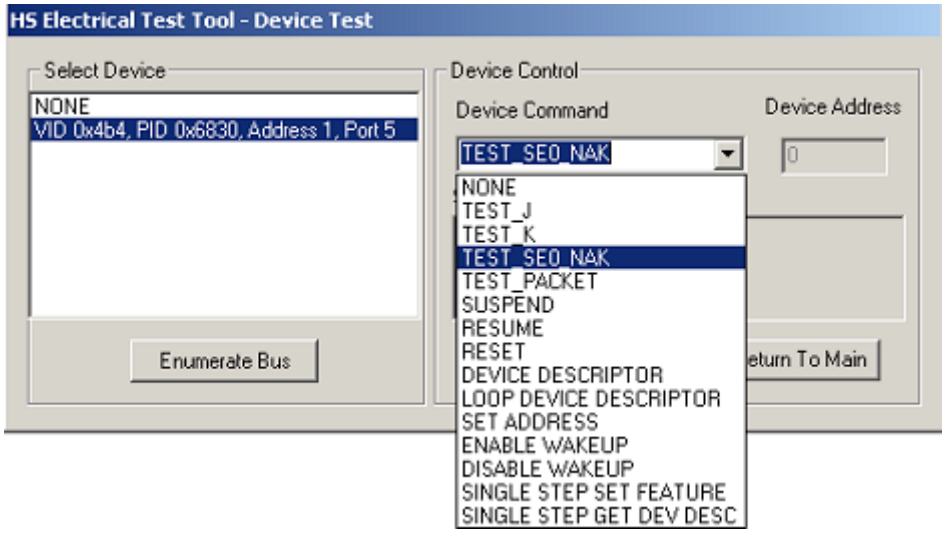

Figure 58. Device Test_SE0_NAK Command

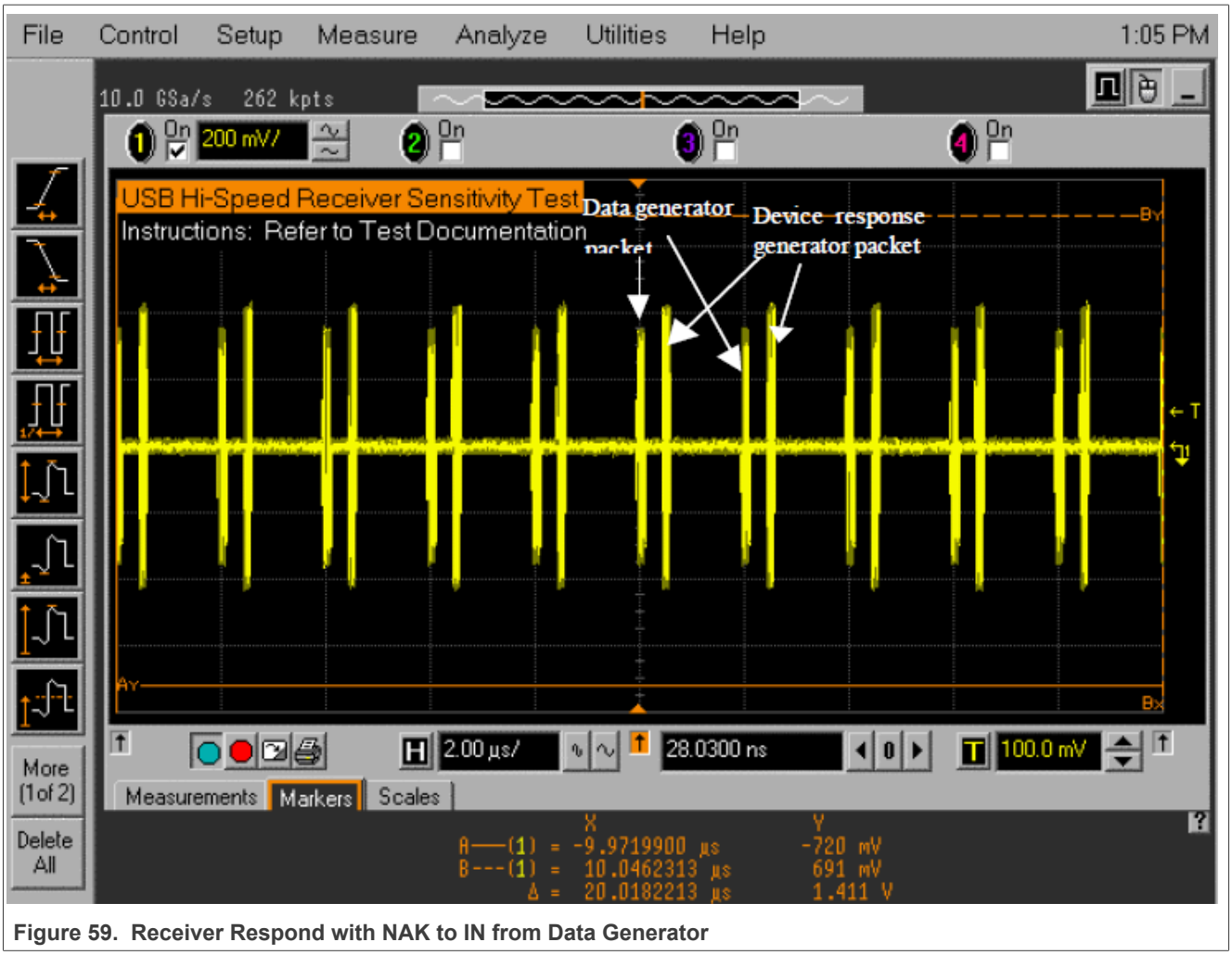

Figure 59. Receiver Respond with NAK to IN from Data Generator

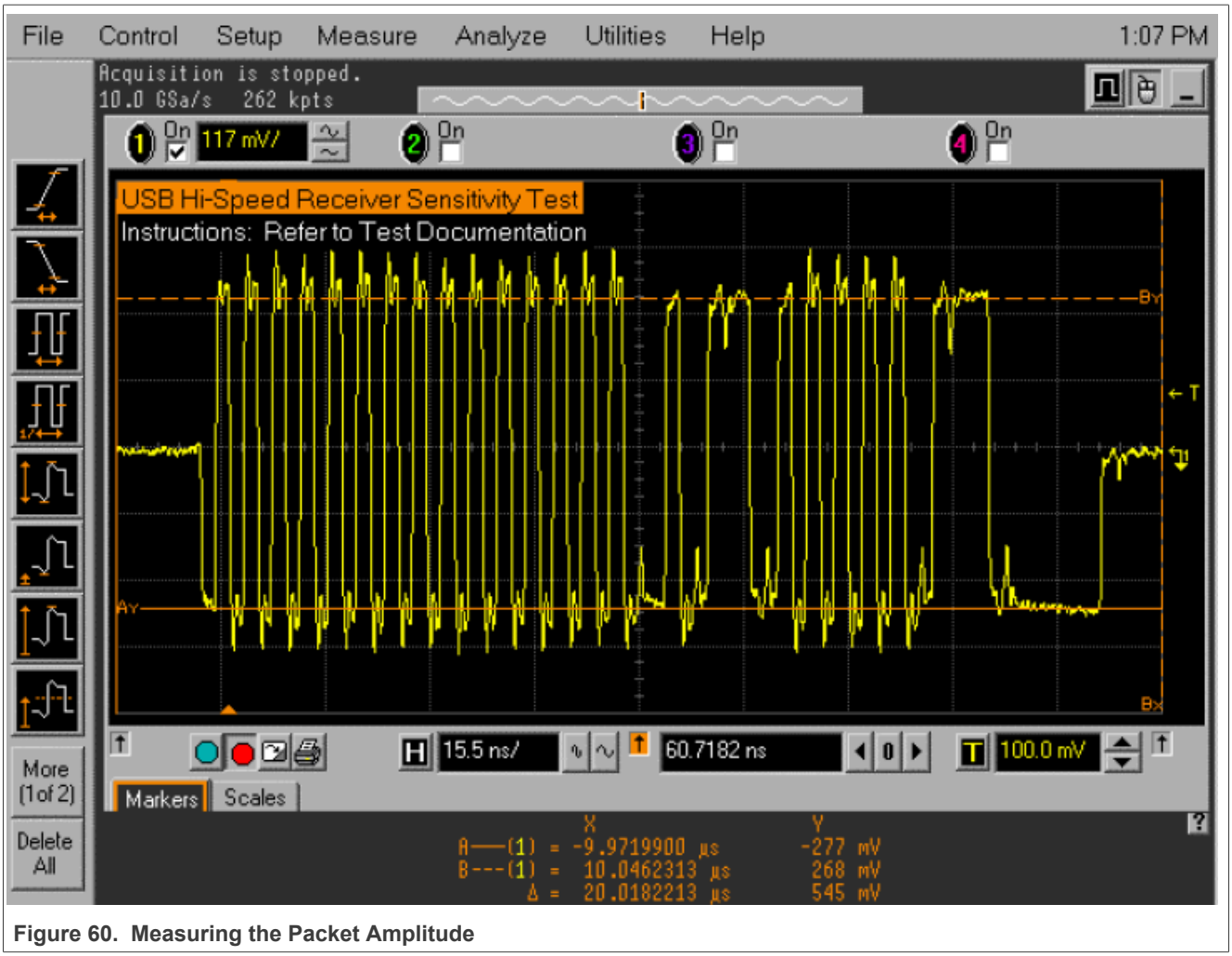

Figure 60. Measuring the Packet Amplitude

3.3 Host high-speed signal test

- Host High-Speed Signal Quality Test
  - **EL_2:** Data Rate Test
  - **EL_3:** Eye Pattern and Mask Test
  - **EL_6:** Rise and Fall Time Test
  - **EL_7:** Non-Monotonic Edge Test
- Host Packet Parameters Test
  - **EL_21:** Sync Field Length Test
  - **EL_25:** EOP Length Test
  - **EL_23:** Inter-packet Gap Between First 2 Packets Test
  - **EL_22:** Measure Inter-packet Gap Between Host and Device Packet Test
  - **EL_55:** SOF EOP Width Test
- Host CHIRP Timing Test
  - **EL_33:** Measure Host CHIRP response time
  - **EL_34:** Measure Host CHIRP-J/K duration
- Host Suspend/Resume Timing Test
  - **EL_39:** Host Suspend Timing Response

  - **EL_41:** Host Resume Timing Response
- Host Test J/K, SE0_NAK Test
  - **EL_8:** Host J Test
  - **EL_8:** Host K Test
  - **EL_9:** Host SE0_NAK Test

3.3.1 HS host electrical test limits

Table 12. HS Host Electrical Test Limits

Test Name	Pass Limits
EL_2 Data Rate	Within 480 Mb/s +/-0.05%
EL_3 Data Eye and Mask Test	Must meet Template 1 transform waveform requirements at TP2
EL_6 Host Rise/Fall Time	>500 ps
EL_7 Host Non-Monotonic Edge Test	Must have monotonic data transitions over the vertical openings
EL_21 Sync Field Length Test	32 bits, 65.62 ns <= VALUE <= 67.700 ns
EL_25 EOP Length Test	8 bits, 15.620 ns <= VALUE <= 17.700 ns
EL_23 Inter-packet Gap Between First 2 Packets Test	183.000 ns <= VALUE <= 399.400 ns
EL_55 SOF EOP Width Test	40 bits, 81.100 ns <= VALUE <= 83.388 ns
EL_22 Inter-packet Gap Between Host and Device Packet Test	16.640 ns <= VALUE <= 399.90 ns
EL_33 CHIRP Timing Response	1 ns <= VALUE <= 100.000 µs
EL_34 CHIRP J/K Width	40.000 µs <= VALUE <= 60.000 µs
EL_35 SOF Timing Response	100.000 µs <= VALUE <= 500.000 µs
EL_39 Suspend Timing Response	3.000 ms <= VALUE <= 3.125 ms
EL_41 Resume Timing Response	VALUE <= 3.000 ms
EL_8 Host J Test	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV
EL_8 Host K Test	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
EL_9 Host SE0_NAK Test	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV

3.3.2 Test method and tool

In USB Certification, Host means a product base on Windows x86 or x64 systems, which can implement the HS Electrical Test Tool on it to run the Host test, and an Embedded Host means a product base on Linux, Android, or other RTOS. Anyway, USB-IF defines a method about entering the specified test modes via PID/VID detection. See chapter **6.4.1** of "*On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification*".

Certification Lab usual provides an HSEHET Board for Host or Embedded Host test, which can be set to different PIDs, as shown Figure 61 below.

Table 13. Test Modes

PID	Test Mode
0x0101	Test_SE0_NAK
0x0102	Test_J
0x0103	Test_K
0x0104	Test_Packet

Table 13. Test Modes *...continued*

PID	Test Mode
0x0105	Reserved
0x0106	HS_HOST_PORT_SUSPEND_RESUME
0x0107	SINGLE_STEP_GET_DEV_DESC
0x0108	SINGLE_STEP_ GET_DEV_DESC_DATA

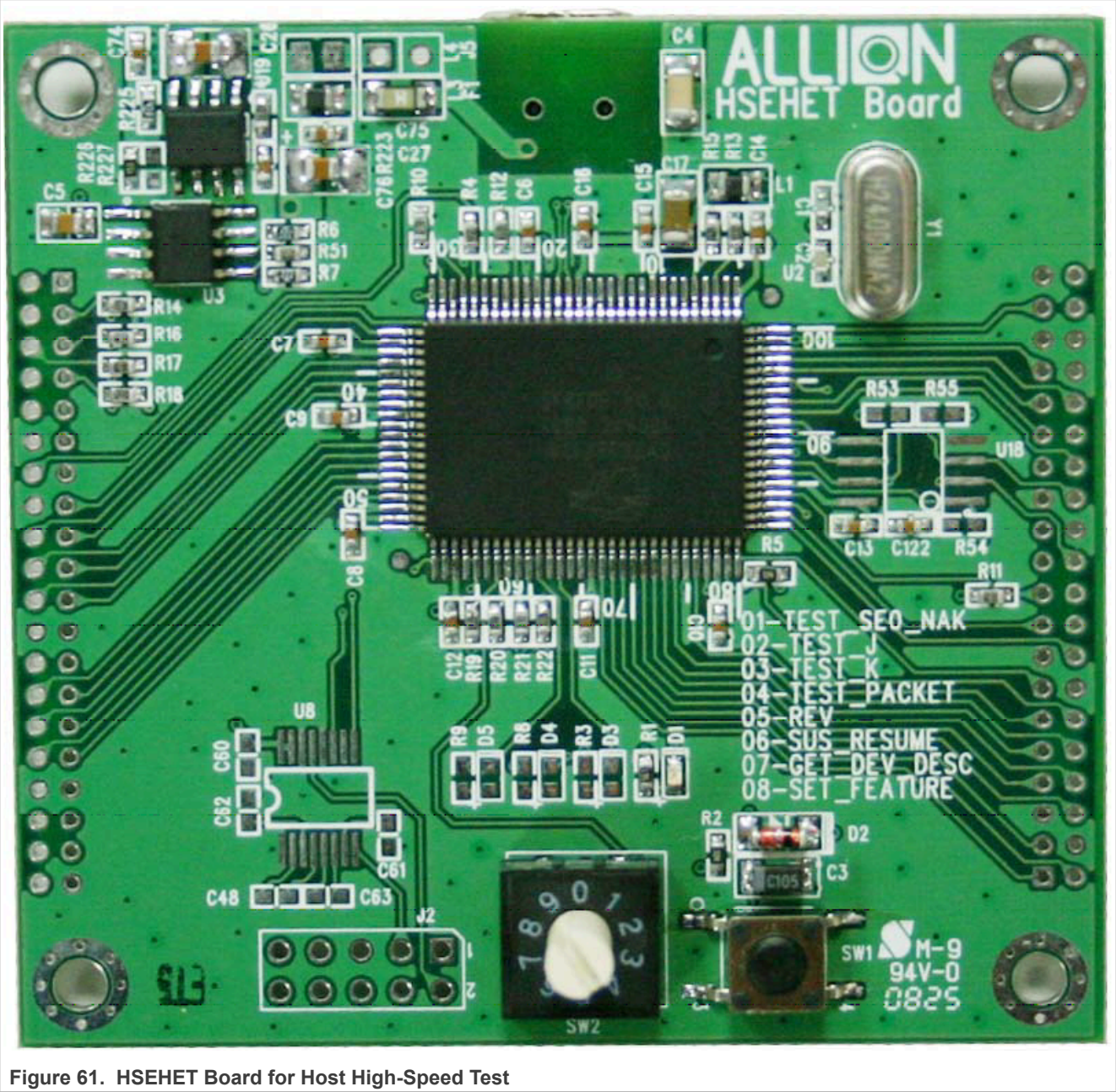

Figure 61. HSEHET Board for Host High-Speed Test

3.3.3 Host high-speed signal quality test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 62 and Figure 63 below, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 64 below.
   - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
   - Before connecting the HSEHET Board, put it in the right position by selecting **Test_Packet.** Then connect the board to the [**INIT PORT**] with a 5 m cable.
   - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
3. Click **Run Tests** button of Automated Test Software on Oscilloscope.
4. Host enumerates the HSEHET board and responds to send continuously **Test_Packet.** Flip the switch of the test fixture that switches the termination on. Verify that the yellow TEST LED is lit.
5. You should see the transmitted test packet on oscilloscope as shown in Figure 65and Figure 66 below.
6. When the Testing Complete dialog appears, click **Ok.** The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

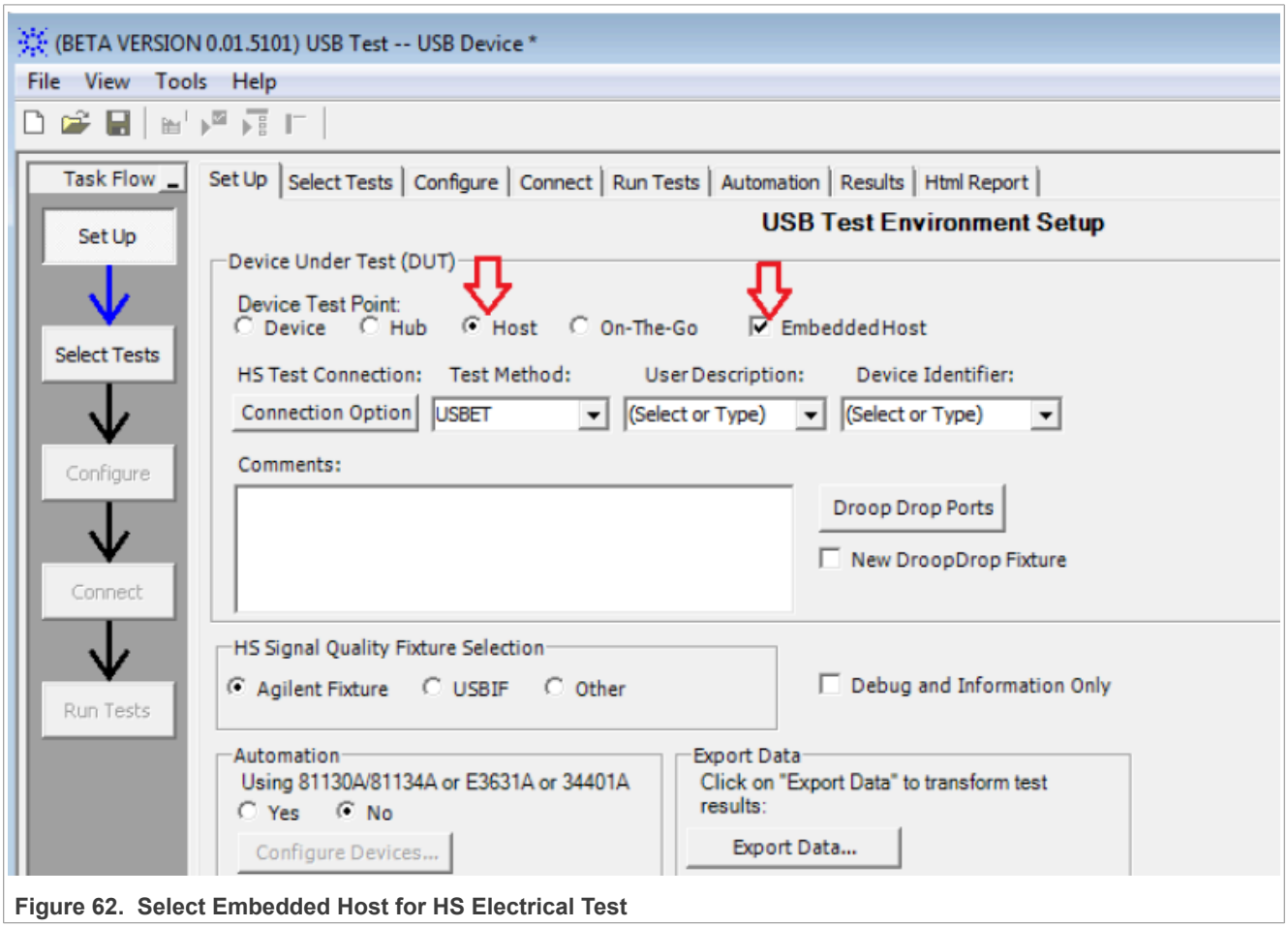

Figure 62. Select Embedded Host for HS Electrical Test

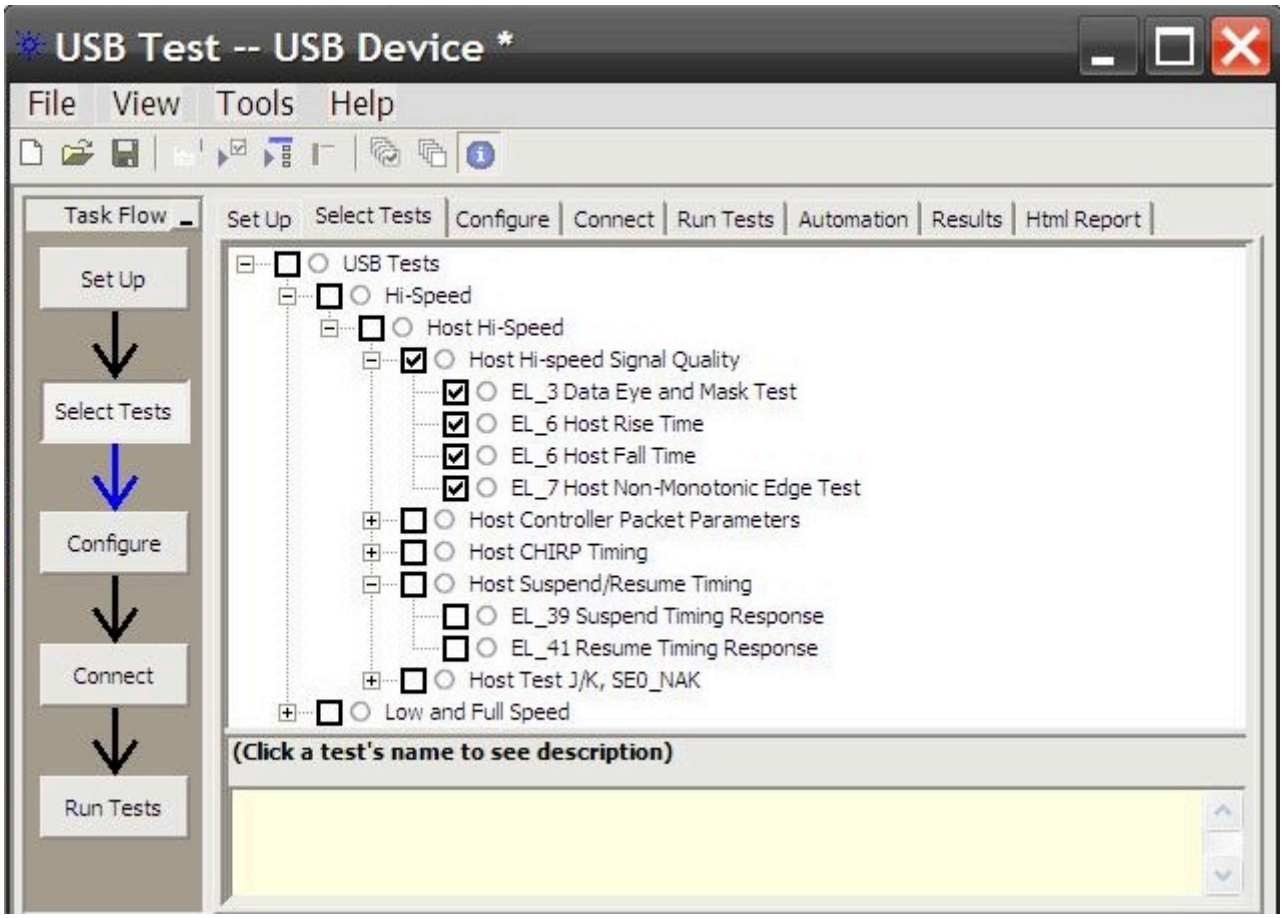

Figure 63. Host HS Signal Quality Test

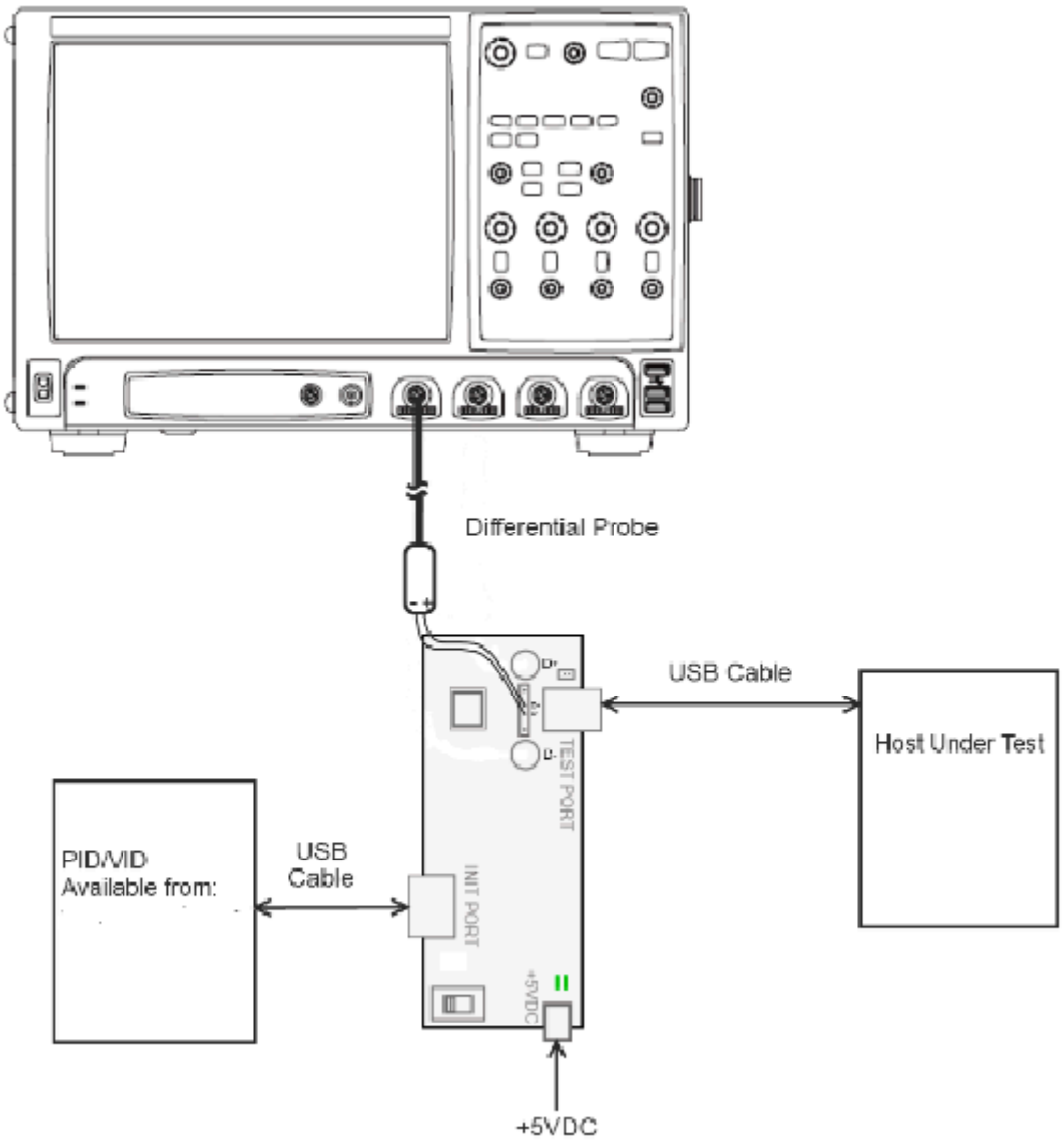

Figure 64. Host HS Signal Quality Test Environment

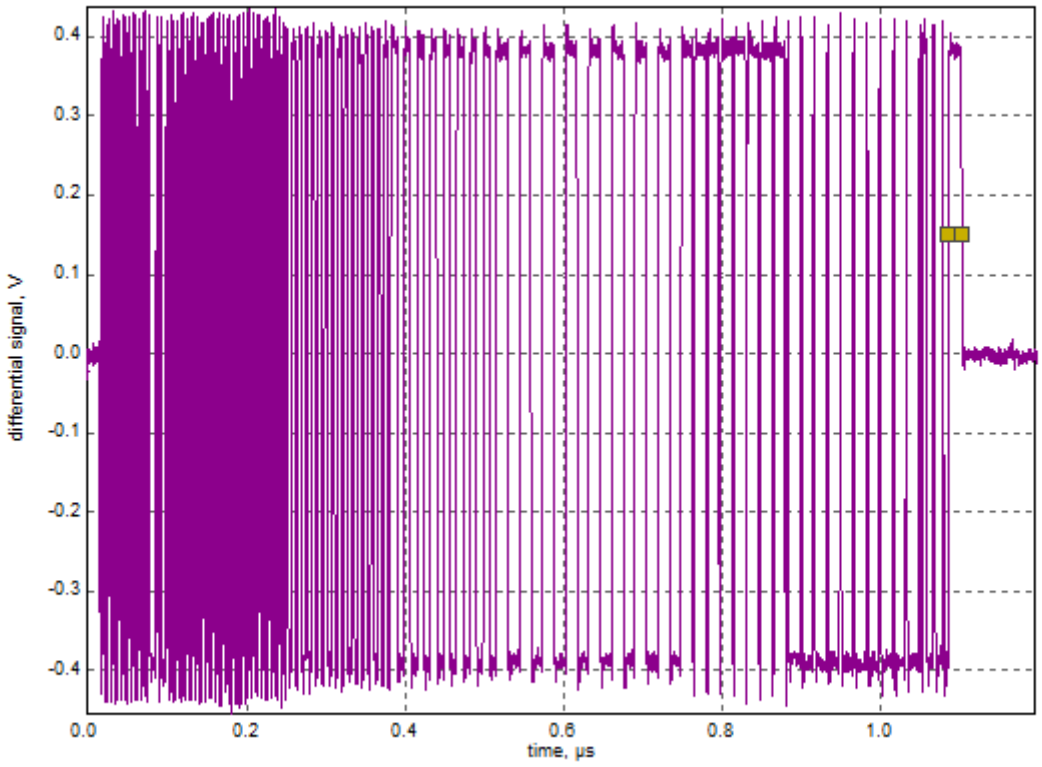

Figure 65. Host HS Test Packet

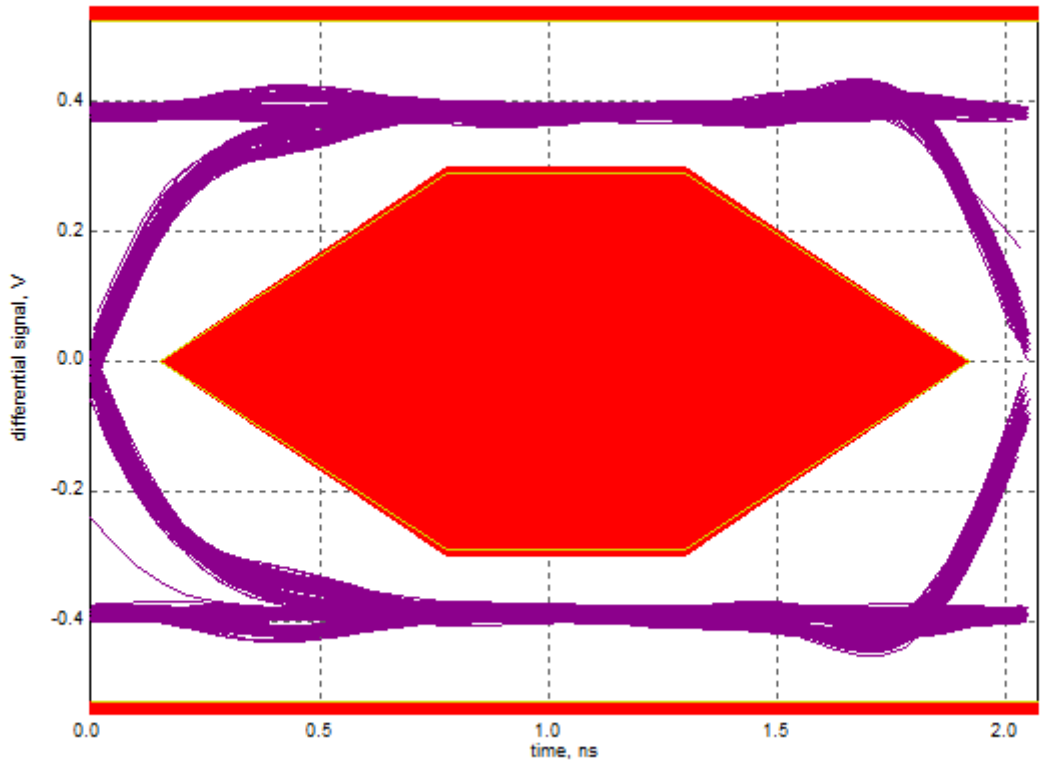

Figure 66. Host HS Eye Diagram

Note: *Select Embedded Host for non-Windows products. Click Connection Option button here to select Differential or Single-End probe if you are using the latest software.*

3.3.4 Host packet parameters test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 67 below, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 66 above.
   - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
   - Before connecting the HSEHET Board, put it in the right position by selecting **SINGLE_STEP_GET_DEVICE_DESCRIPTOR**. Then connect the board to the [**INIT PORT**] with a 5 m cable.
   - Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture, Ensure the + polarity on the probe lines up with D+.
3. Click **Run Tests** button of Automated Test Software on Oscilloscope.

4. Host enumerates the HSEHET board and responds to send **SOF** s for 15 seconds. Click **OK** to close the Test Instruction dialog.
5. After 15 seconds of **SOF** s, the host initiates the setup phase of the **GetDescriptor()** command. The host sends **SETUP** and **DATA** (first and second packet), then Device sends an **ACK**. You should see the transmitted test packet on the oscilloscope as shown in Figure 71 below. Click **OK** to close the Test Instruction dialog.
6. Disconnect the HSEHET Board, put it in the right position by selecting **SINGLE_STEP_GET_DEVICE_DESCRIPTOR_DATA**, then reconnect it to test fixture.
7. Host enumerates the HSEHET board and request **GetDescriptor()**, then wait for 15 seconds. After that, Host initiates an **IN** token, Device responds a **DATA**, then Host send an **ACK**. You should see the transmitted test packet on the oscilloscope as shown in Figure 70 below.
8. When the Testing Complete dialog appears, click **Ok.** The **Results** tab shows the test results, and the **HTML Report** shows the whole report.
   •

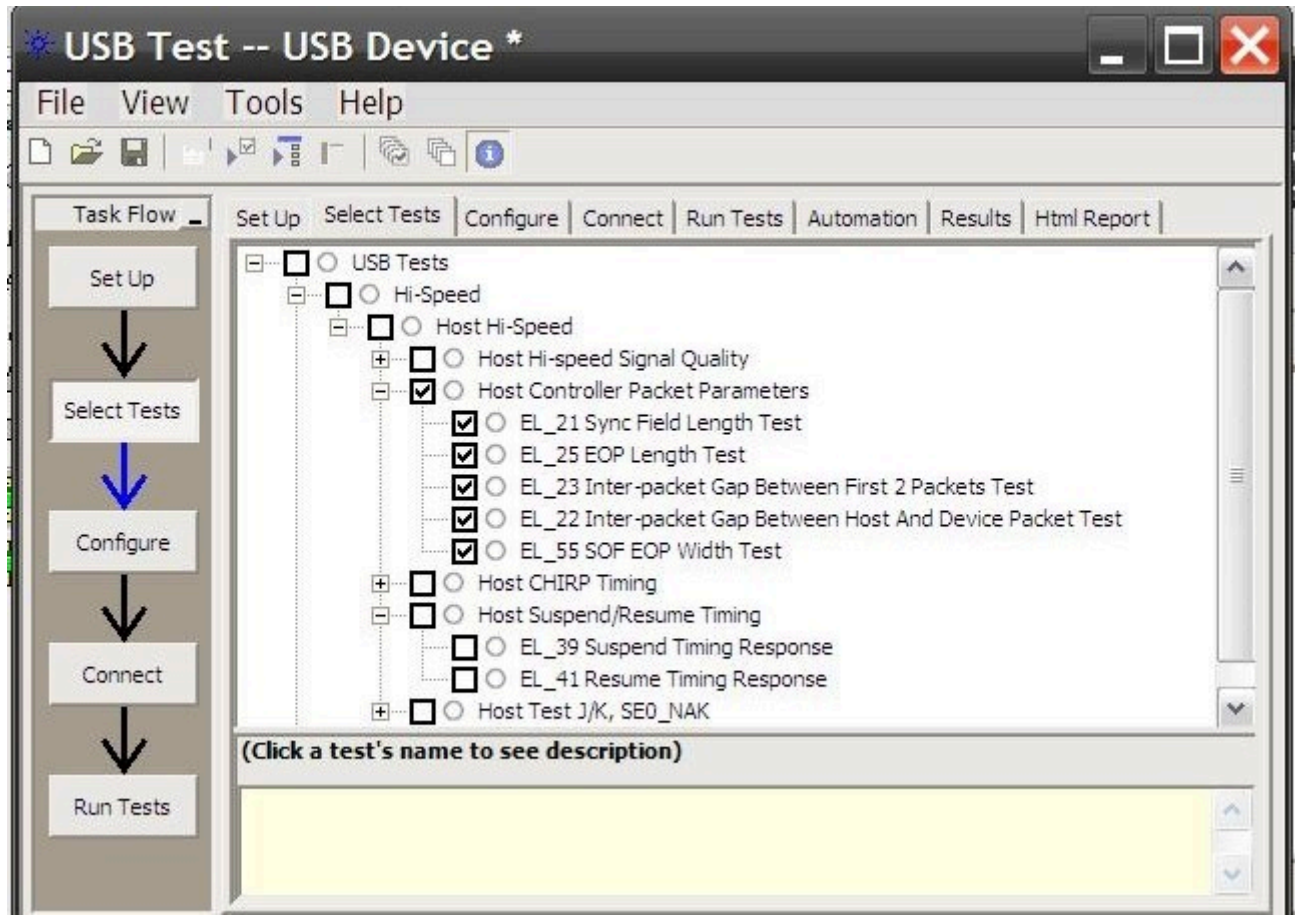

Figure 67. Host HS Packet Parameters Test

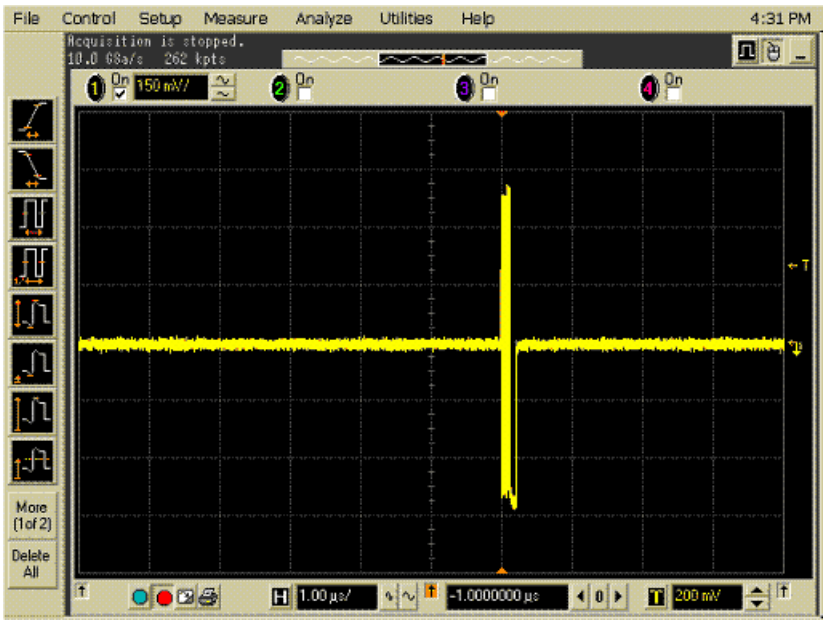

Figure 68. Host SOF Waveform

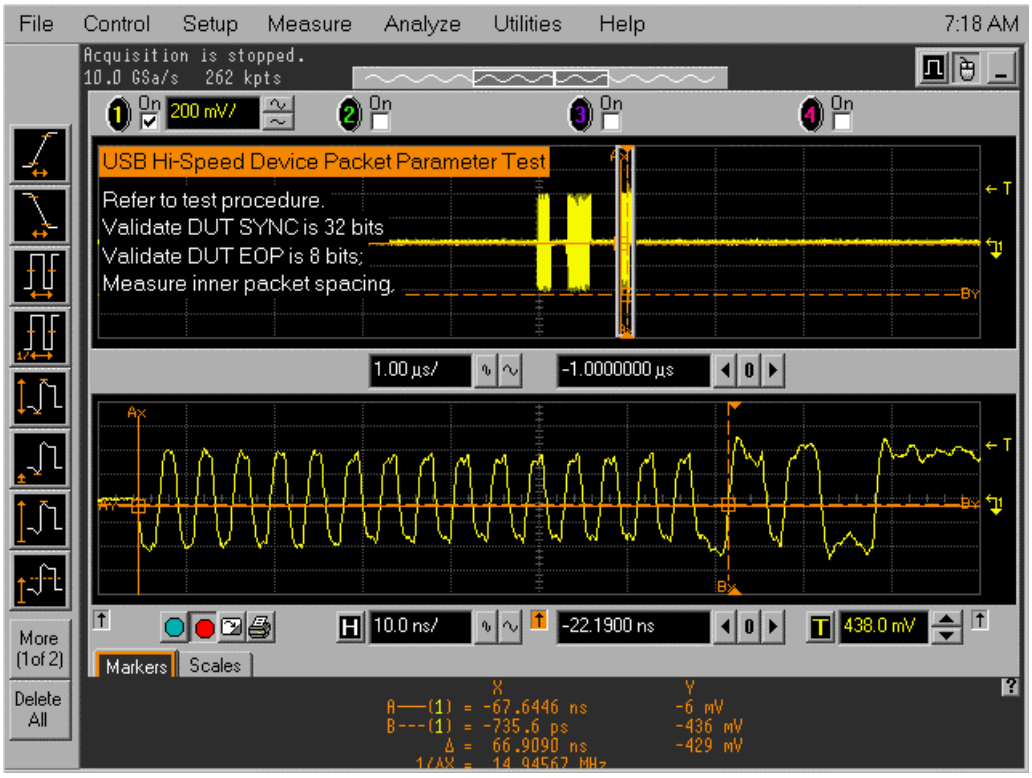

Figure 69. EL_21 Host Sync Field Length Waveform

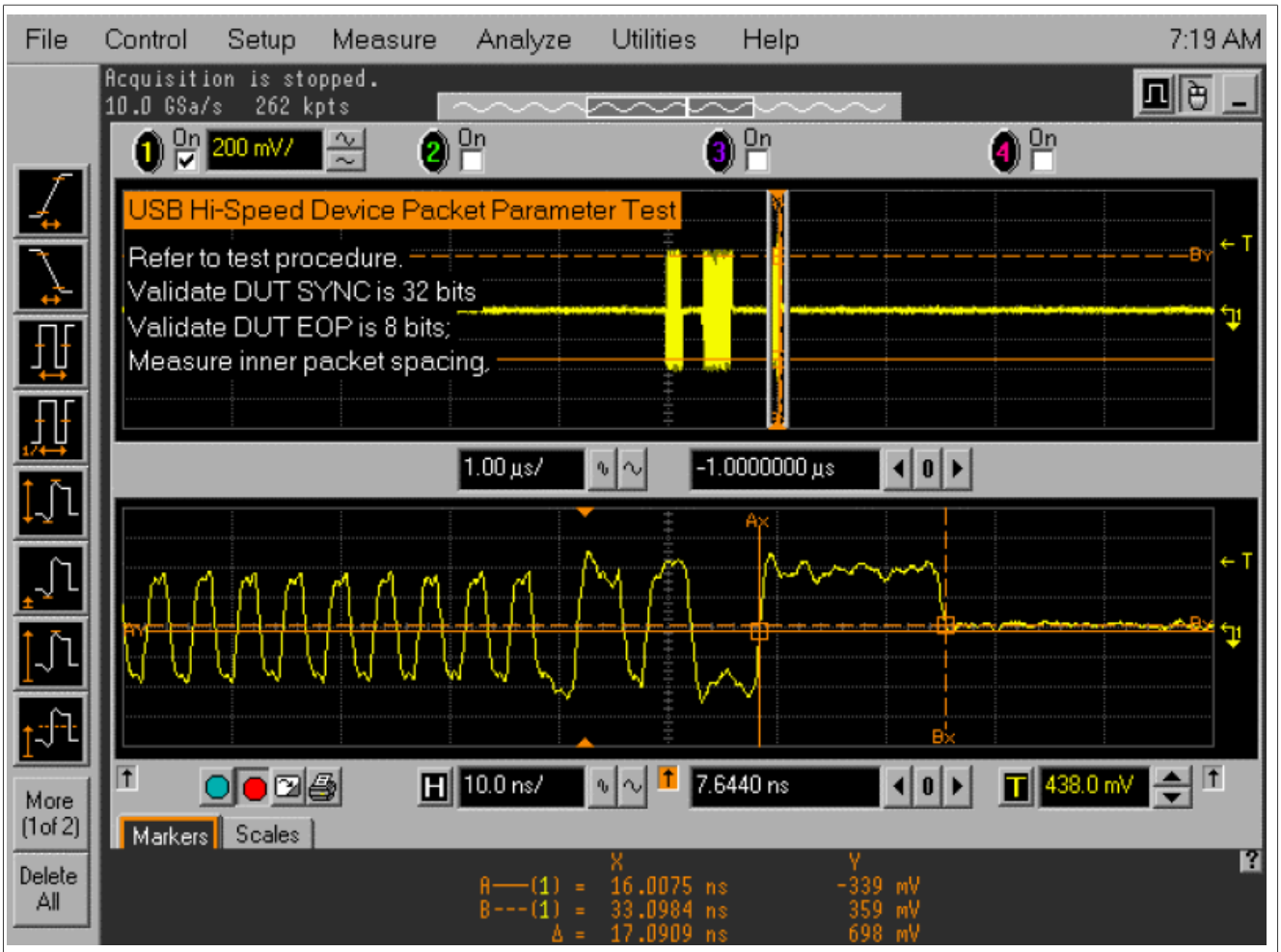

Figure 70. EL_25 Host EOP Length Waveform

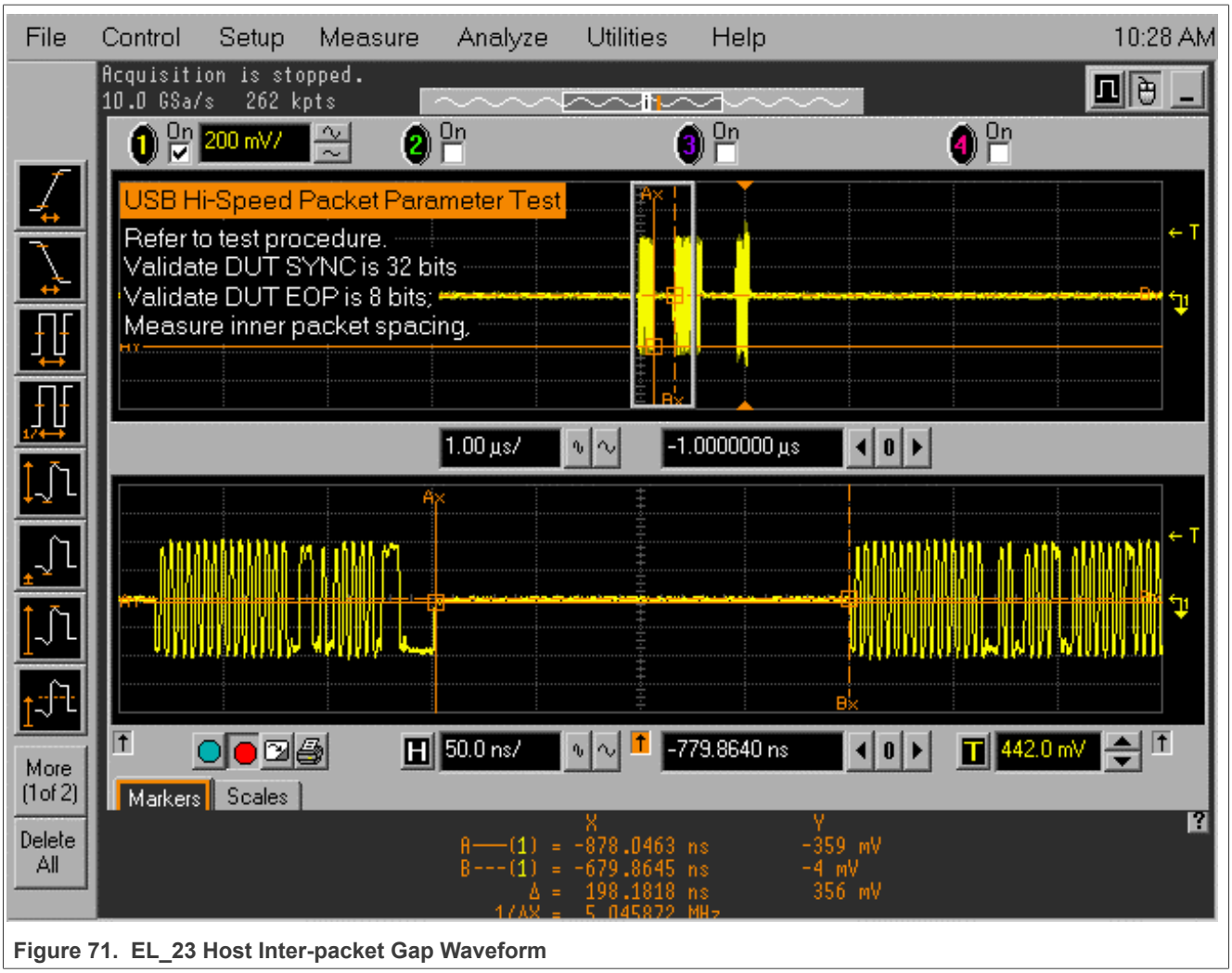

Figure 71. EL_23 Host Inter-packet Gap Waveform

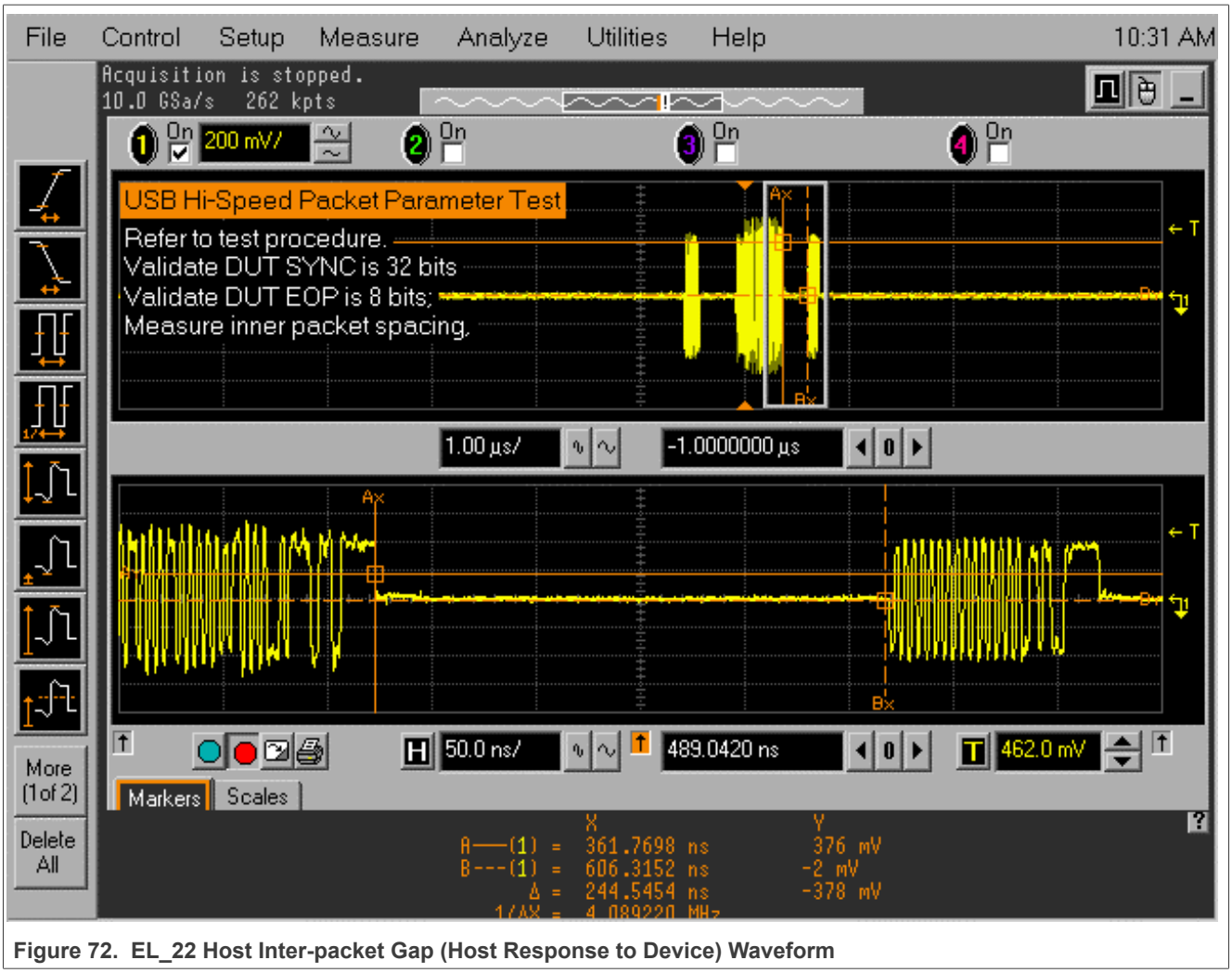

Figure 72. EL_22 Host Inter-packet Gap (Host Response to Device) Waveform

3.3.5 Host CHIRP timing test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 73 below, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 74.
   - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
   - Attach the single-ended probes on channel 2 to D-, channel 3 to D+ of TP2 on the test fixture.
3. Click **Run Tests** button of Automated Test Software on Oscilloscope.
4. Connect any known good Hi-Speed device to the initialize port. Capture the CHIRP handshake as shown in Figure 75 and Figure 76.
5. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

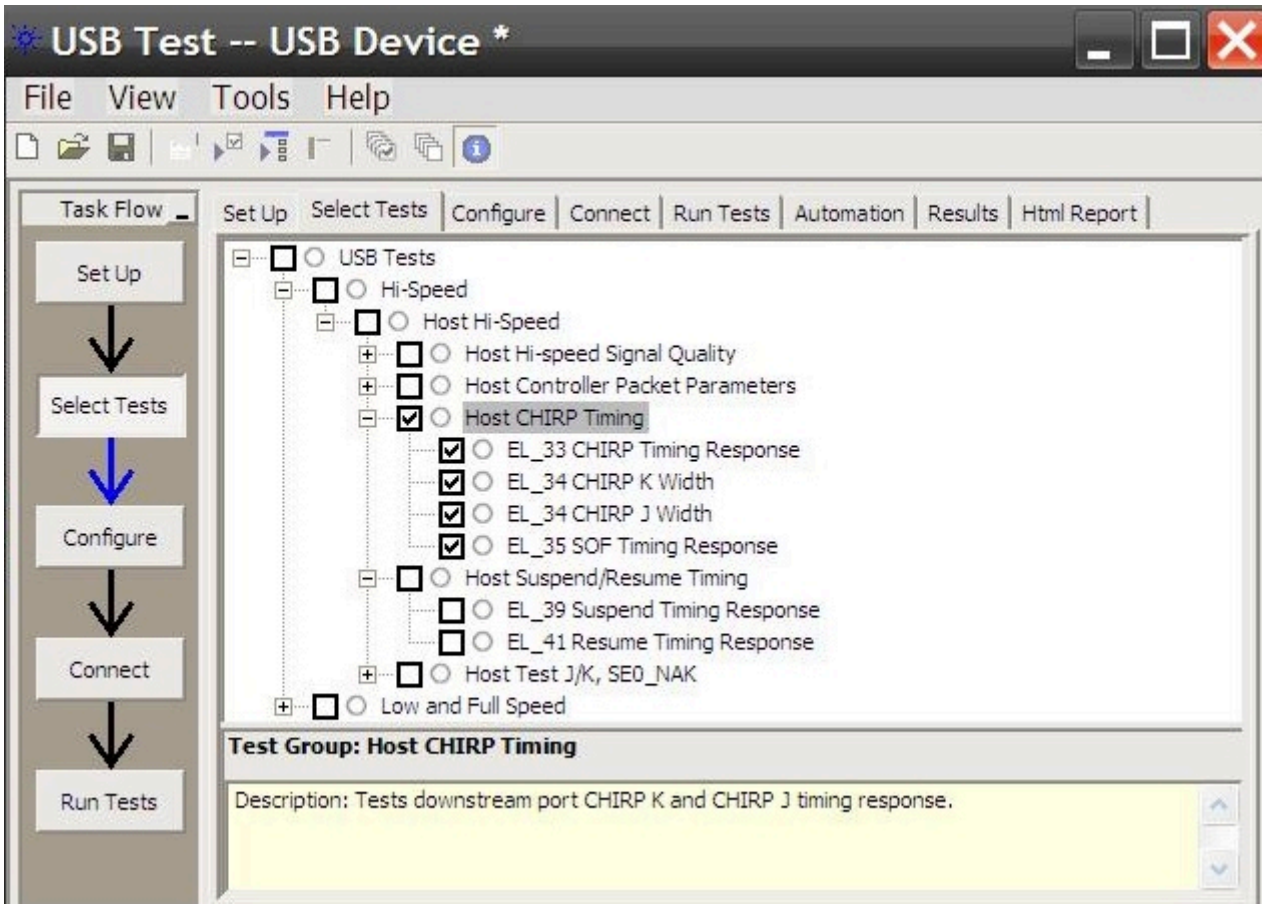

Figure 73. Host CHIRP Timing Test

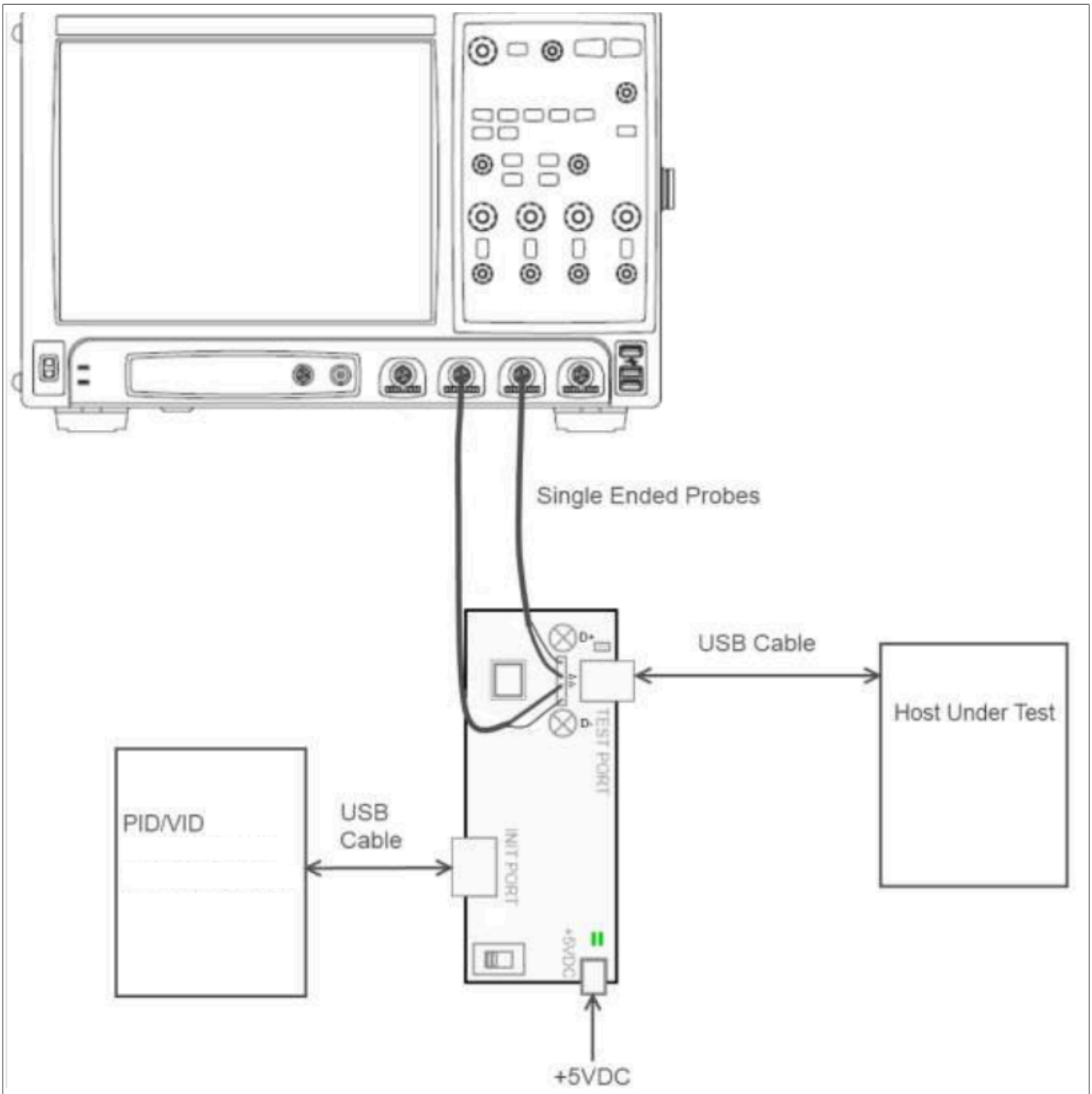

Figure 74. Host CHIRP Timing Test Environment

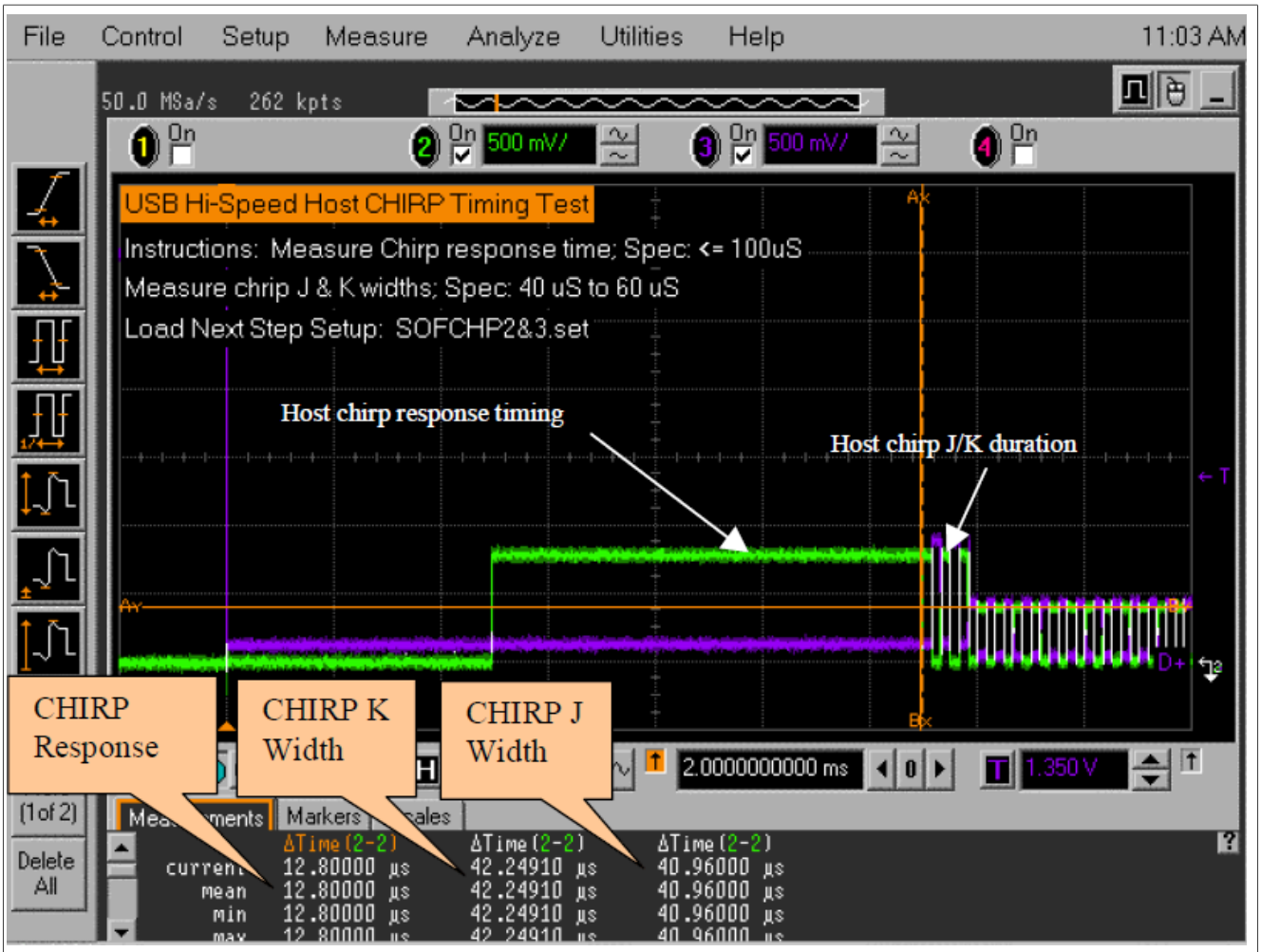

Figure 75. Host CHIRP J/K Waveform

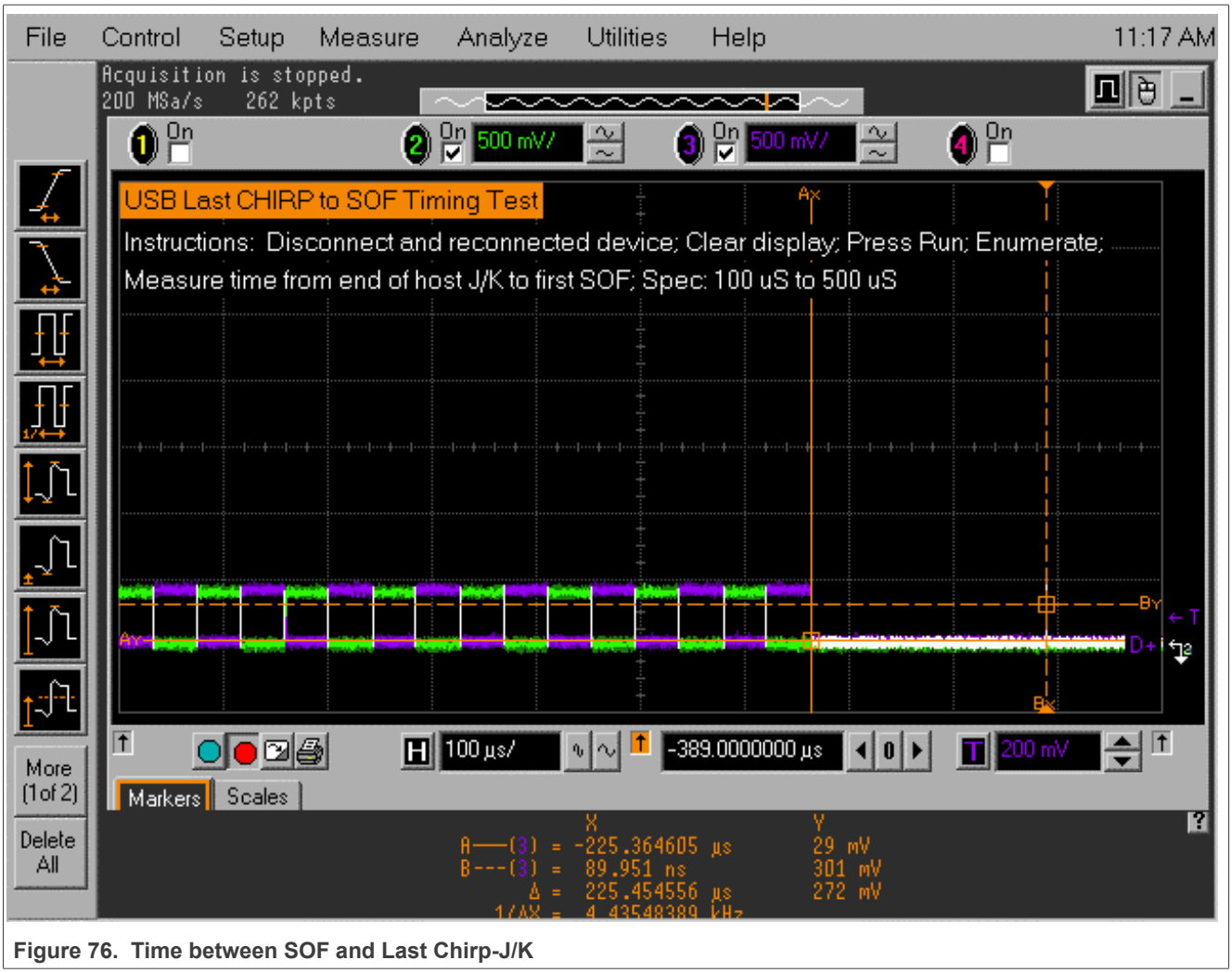

Figure 76. Time between SOF and Last Chirp-J/K

3.3.6 Host Suspend/Resume timing test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 77 below, and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture.
   - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
   - Attach the single-ended probes on channel 2 to D-, channel 3 to D+ of TP2 on the test fixture.
   - Before connecting the HSEHET Board, put it in the right position by selecting **HS_HOST_PORT_SUSPEND_RESUME**. Then connect the board to the [**INIT PORT**] with a 5 m cable.
3. Click **Run Tests** button of Automated Test Software on Oscilloscope.
4. After 15 seconds the host port enters Suspend state, as shown in Figure 78 below. Click **OK** to close the Test Instruction dialog.

5. After 15 seconds of suspend state the host shall issue a **Resume K** state on the bus, then continue sending SOFs. The captured transition should be as shown in Figure 79 below.
6. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

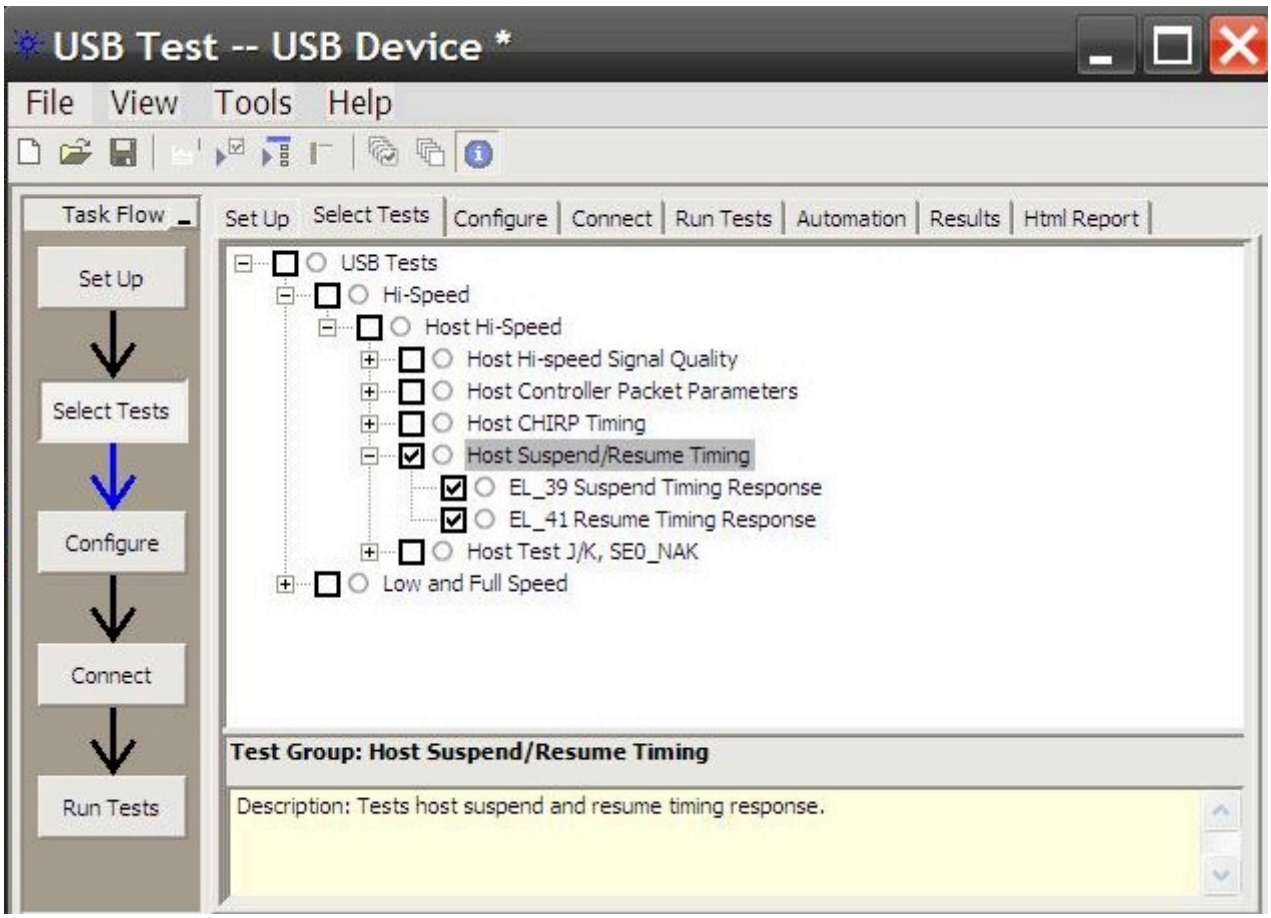

Figure 77. Host Suspend/Resume Timing Test

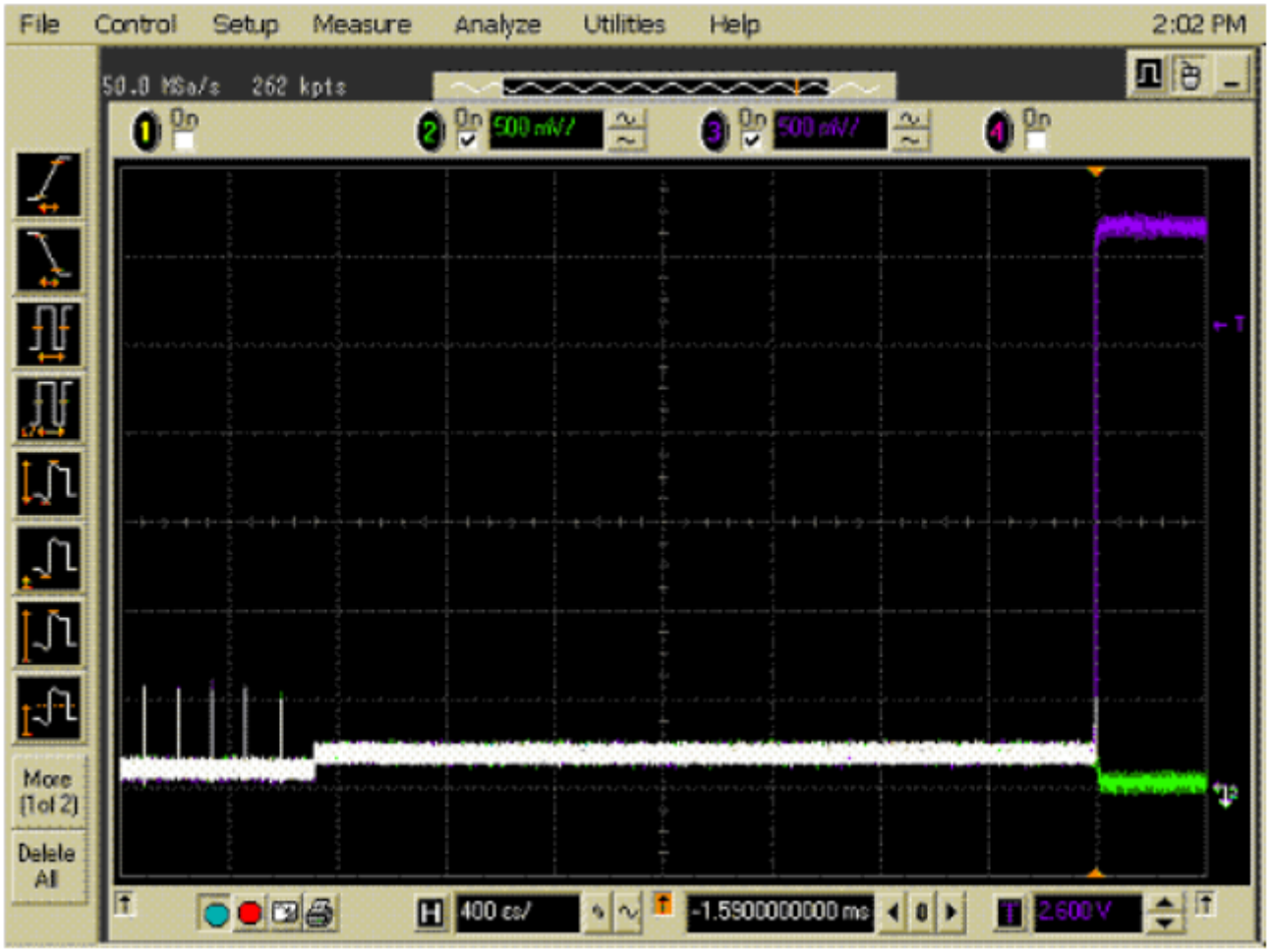

Figure 78. EL_39 Host Suspend waveform

Figure 79. EL_41 Host resume waveform

Note: *Attach the HSEHET board slightly earlier before clocking the* ***Run Tests*** *button, in case you capture the Bus Enumeration instead of Suspend transition.*

3.3.7 Host test J/K, SE0_NAK test

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 80 below and make sure you set the Test Type configuration option to “Hi-Speed Near End” before running the test.
2. Connect the equipment and test fixture as shown in Figure 81 below.
   - Attach the 5 V power supply to J5 of the Host Hi-Speed signal quality test fixture (E2649- 66402). Leave the TEST switch at the OFF position. Verify that the green Power LED is lit and the yellow Test LED is not lit.
   - Connect the [**TEST PORT**] of the test fixture into the downstream facing port of the DUT, using the 4" USB cable.
   - Before connecting the HSEHET Board, put it in the right position by selecting **Test_J**. Then connect the board to the [**INIT PORT**] with a 5 m cable.
   - Attach the single-ended probes on channel 2 to D-, channel 3 to D+ of TP2 on the test fixture.
3. Click **Run Tests** button of Automated Test Software on Oscilloscope.

4. Host enumerates the HSEHET board and enters a Hi-Speed **J State** (D+ high; D- low). Flip the switch of the test fixture that switches the termination on. Verify that the yellow TEST LED is lit. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
5. Flip the switch of the test fixture to OFF mode.
6. Press the RESET button on DUT or repower it to reset the system.
7. Remove the HSEHET board from [**INIT PORT**] of the test fixture, and put it in the right position by selecting **Test_K**. Then connect the board to the [**INIT PORT**] again with a 5 m cable.
8. Host enumerates the HSEHET board and enters a Hi-Speed **K State** (D+ low; D- high). Flip the switch of the test fixture that switches the termination on, verify that the yellow TEST LED is lit. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
9. Flip the switch of the test fixture to OFF mode.
10. Remove the HSEHET board from [**INIT PORT**] of the test fixture, and put it in the right position by selecting **Test_SE0_NAK**. Then connect the board to the [**INIT PORT**] again with a 5 m cable.
11. Host enumerates the HSEHET board and enters the **SE0 State** (D+ low; D- low). Flip the switch of the test fixture that switches the termination on, verify that the yellow TEST LED is lit. Use multimeter to measure the DC voltage on the D+/- lines at TP2 with respect to GND, then record in the pop out dialog.
12. When the Testing Complete dialog appears, click **OK**. The **Results** tab shows the test results, and the **HTML Report** shows the whole report.

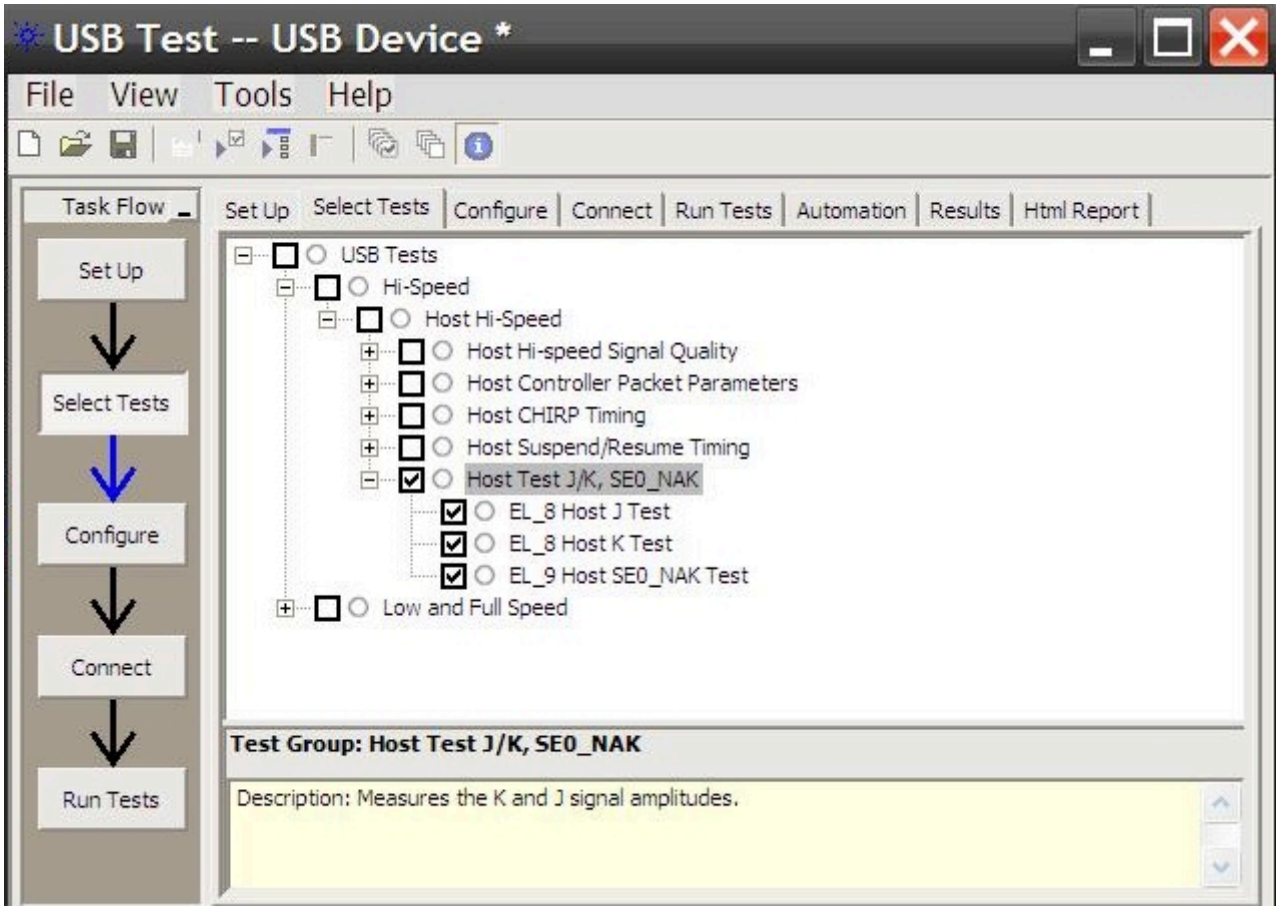

Figure 80. Host Test_J/K, SE0_NAK Test

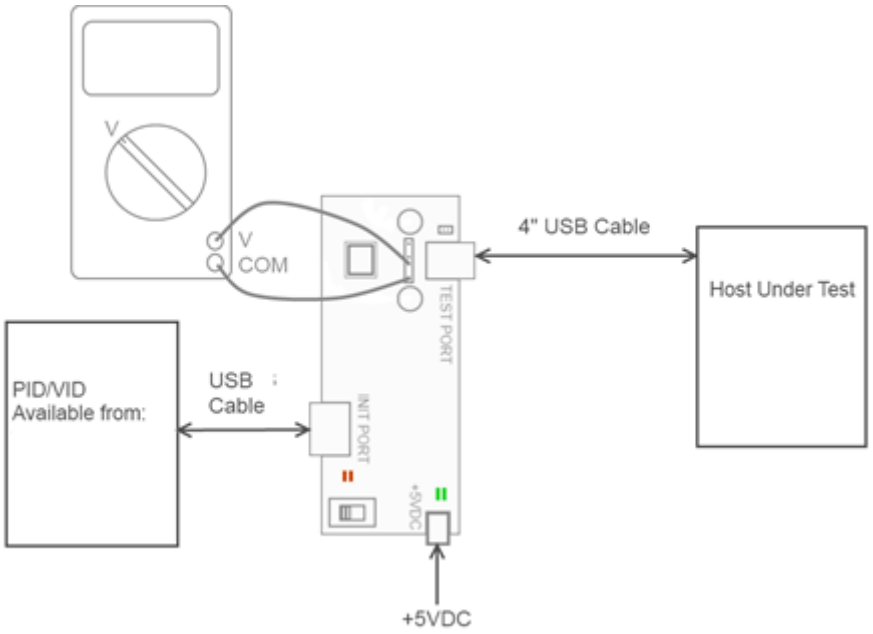

Figure 81. Host Test_J/K, SE0_NAK Test Environment

Table 14. Host Drop Test Record

Test Mode	D+ Voltage(mV)	D- Voltage(mV)	Expected Value
J	400	4	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV
K	4	400	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
SE0_NAK	1	1	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV

3.4 USB3.0 super speed transmitter compliance tests

- Host Low Frequency Periodic Signaling TX Tests
- Host Transmitted SSC Tests
- Host Transmitter Eye Short Channel Tests
- Host Transmitter Eye Far End(TP1) Tests
- Device Low Frequency Periodic Signaling TX Tests
- Device Transmitted SSC Tests
- Device Transmitter Eye Short Channel Tests
- Device Transmitter Eye Far End(TP1) Tests

3.4.1 USB 3.0 super speed transmitted electrical test limits

Table 15. Super Speed Electrical Test Limits

Test Name	Pass Limits
5G LFPS Peak-Peak Differential Output Voltage	800.0 mV <= VALUE <= 1.2000 V
5G LFPS Period (tPeriod)	20.0000 ns <= VALUE <= 100.0000 ns
5G LFPS Burst Width (tBurst)	600.0 ns <= VALUE <= 1.4000 µs

Table 15. Super Speed Electrical Test Limits*...continued*

Test Name	Pass Limits
5G LFPS Repeat Time Interval (tRepeat)	6.0000 µ s <= VALUE <= 14.0000 µs
5G LFPS Rise Time	VALUE <= 4.0000 ns
5G LFPS Fall Time	VALUE <= 4.0000 ns
5G LFPS Duty cycle	40.0000 % <= VALUE <= 60.0000 %
5G LFPS AC Common Mode Voltage	VALUE <= 100.0 mV
5G TSSC-Freq-Dev-Min	-5.300000 kppm <= VALUE <= -3.700000 kppm
5G TSSC-Freq-Dev-Max	TSSCMin ppm <= VALUE <= TSSCMax ppm
5G SSC Modulation Rate	30.000000 kHz <= VALUE <= 33.000000 kHz
5G SSC Slew Rate	VALUE <= 10.000 ms
5G Short Channel Random Jitter	Information Only
5G Short Channel Maximum Deterministic Jitter	VALUE <= 86.000 ps
5G Short Channel Total Jitter at BER-12	VALUE <= 132.000 ps
5G Short Channel Template Test	VALUE = 0.000
5G Short Channel Differential Output Voltage	100.0 mV <= VALUE <= 1.2000 V
5G Random Jitter (CTLE ON)	Information Only
5G Far End Maximum Deterministic Jitter (CTLE ON)	VALUE <= 86.000 ps
5G Far End Total Jitter at BER-12 (CTLE ON)	VALUE <= 132.000 ps
5G Far End Template Test (CTLE ON)	VALUE = 0.000
5G Far End Differential Output Voltage (CTLE ON)	100.0 mV <= VALUE <= 1.2000 V

3.4.2 Host low frequency periodic signaling TX test

This test verifies that the low frequency periodic signal transmitter meets the timing requirements when measured at the compliance test port.

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 82, and make sure you set the Test Type configuration option in Figure 83. If the DUT is a Standard A port, “Configure Transfer Function” should be “**Std A to Std B**”. If the DUT is a Type-C port, “Configure Transfer Function” should be “**C to C**”.
2. Select the test items in the USB Automated Test Software in Figure 84
3. Set the test configures default in Figure 85.
4. Connect your Device Under Test to the Host Test Fixture 1. VBUS is not required. If the DUT is a Standard A port, we choose Test Topology of Standard-A Port in Figure 86. If the DUT is a Type-C port, we choose Test Topology of Type-C Port in Figure 87. And you need **a Jumper** to cover the CC pin to GND on which path you choose.
5. Connect 5 Inch Host Test Fixture 2 to Host Test Fixture 1 using Type A to Type B cable. When Type-C port is tested, a hub from Type A to Type C is needed in Figure 90.
6. Connect **RX+** of the Test Fixture 2 to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes.
7. Connect **TX+** and **TX-** of the Test Fixture 1 to Oscilloscope Channel 1 and Channel 3 using SMA cables. The full connection diagram is show in Figure 89 and Figure 90
8. Click **Run Tests** in the USB Automated Test Software on Oscilloscope. After the test is finished, you can view the report in HTML Report page.

Figure 82. Automated Test Software for USB 3.0

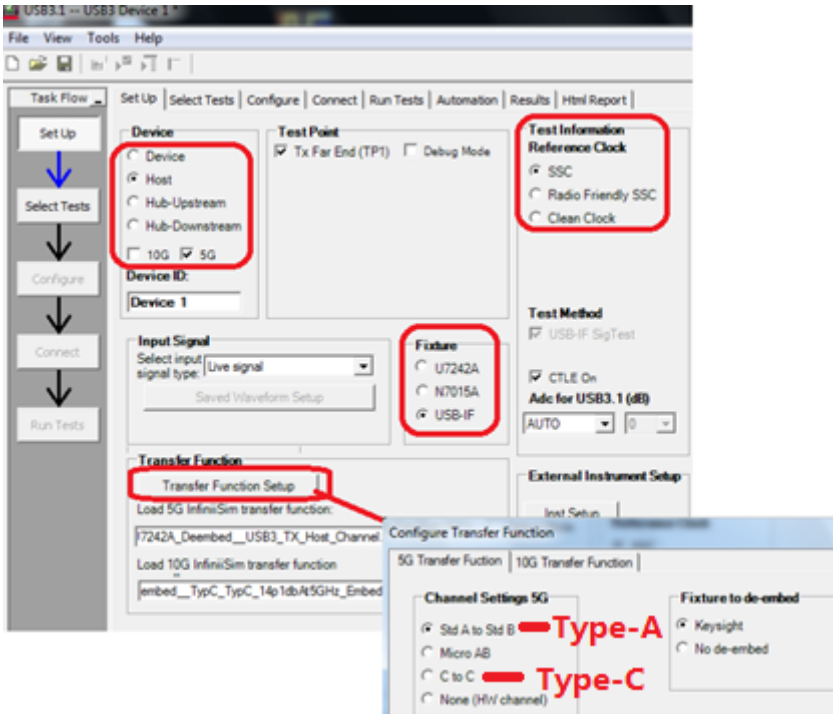

Figure 83. Automated Test Software setting for Standard-A Super Speed Signal Test

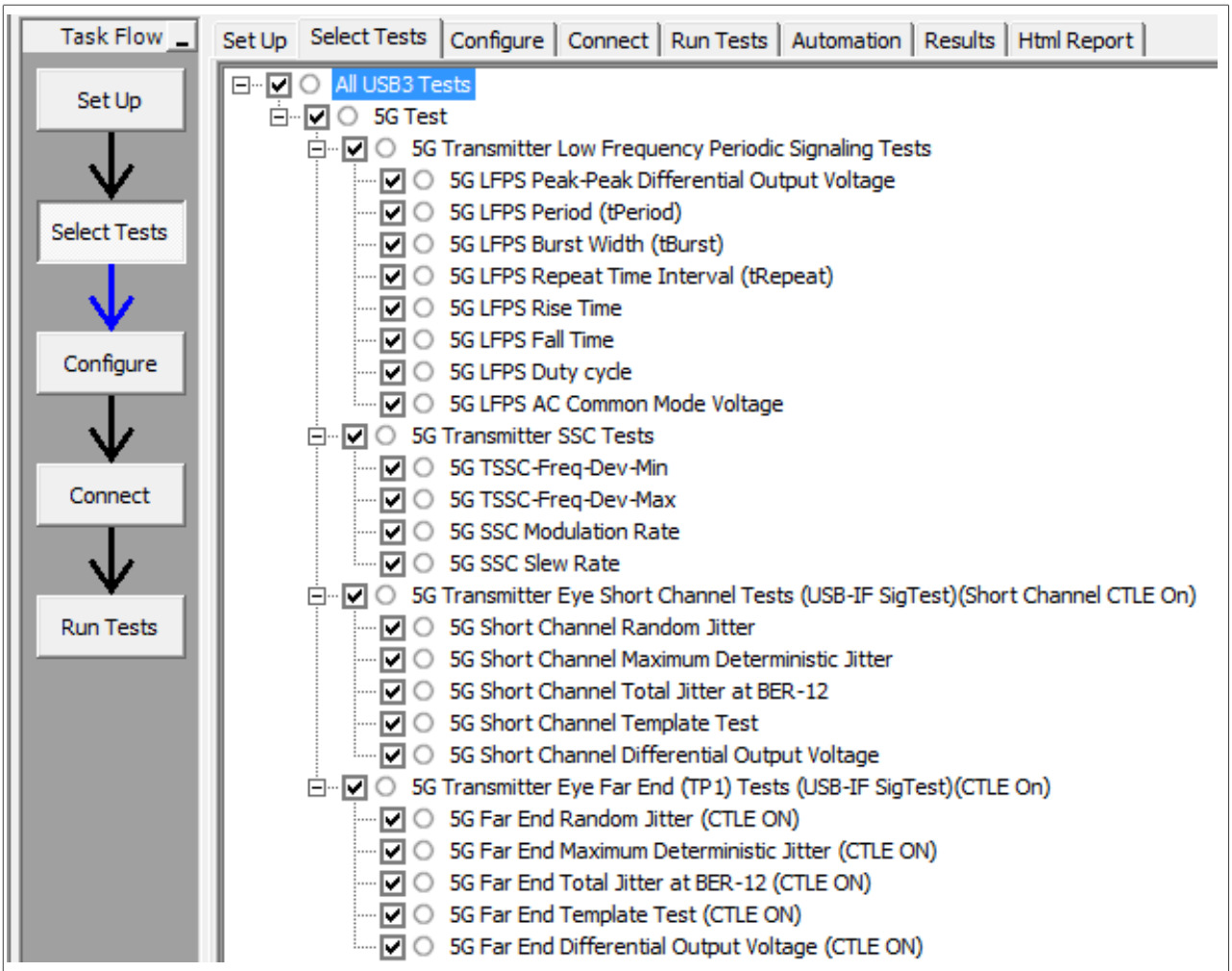

Figure 84. Automated Test Software setting for Testing Items

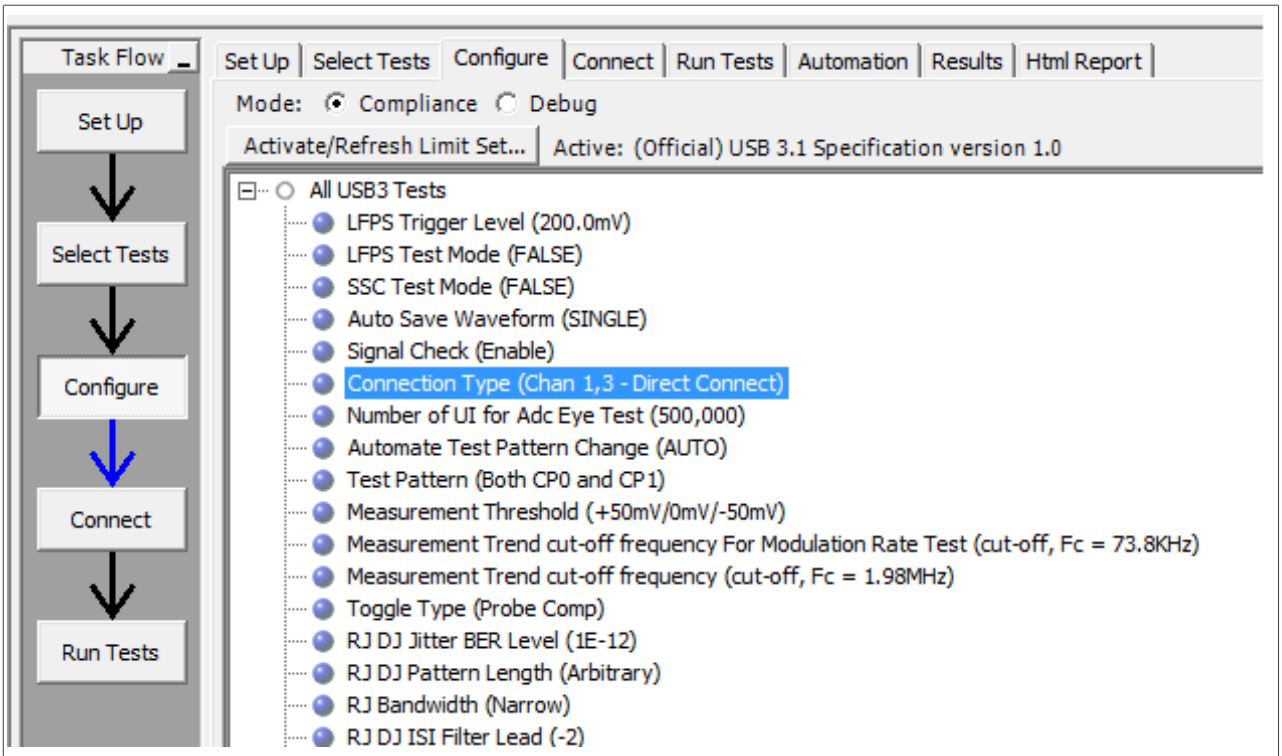

Figure 85. Automated Test Software setting for Testing Configure

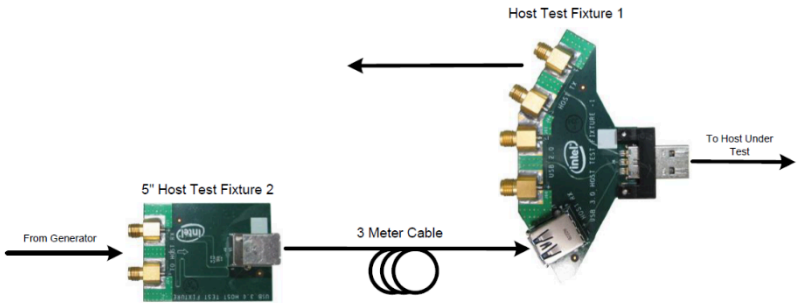

Figure 86. Host TX Test Topology of Standard-A Port

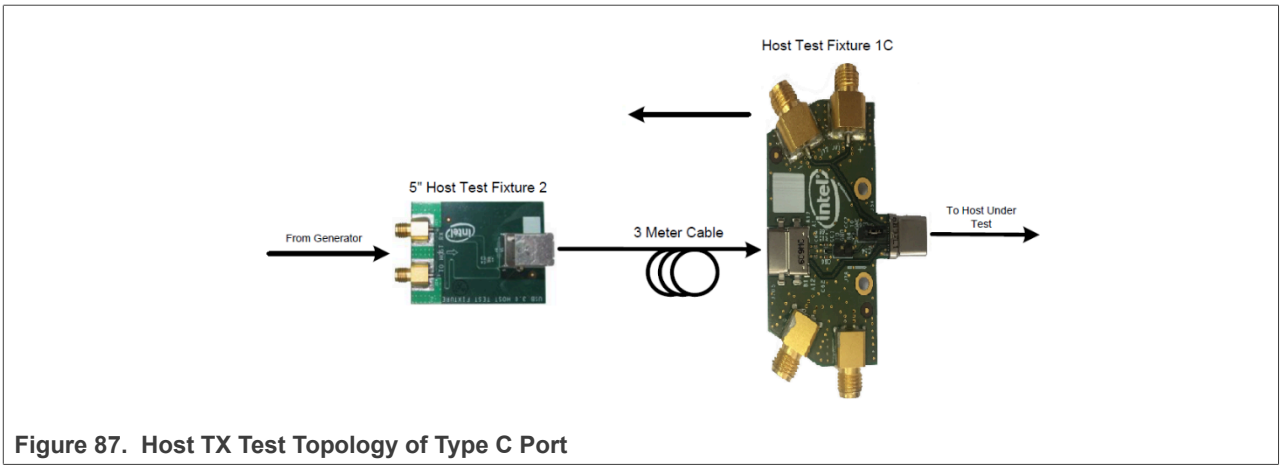

Figure 87. Host TX Test Topology of Type C Port

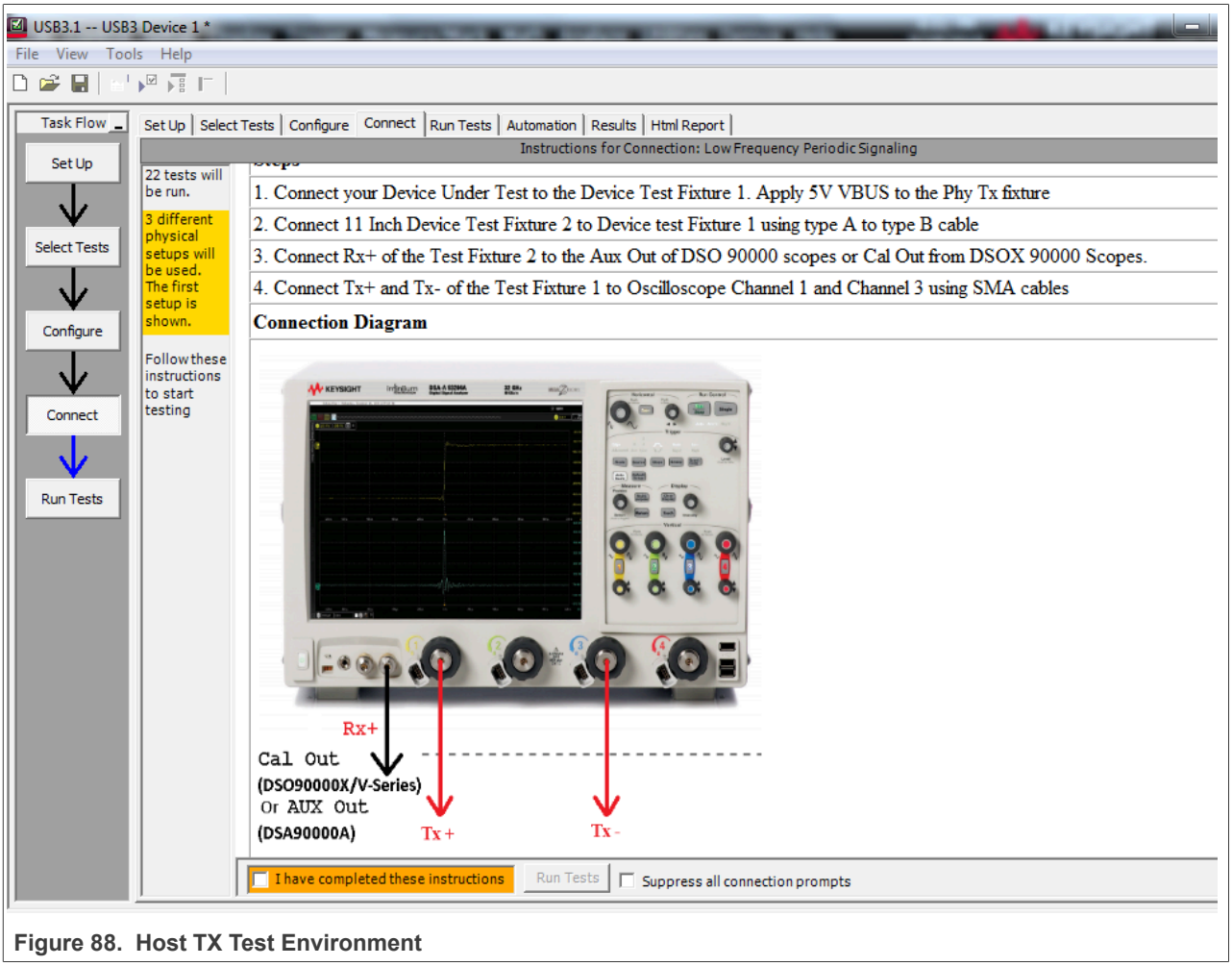

Figure 88. Host TX Test Environment

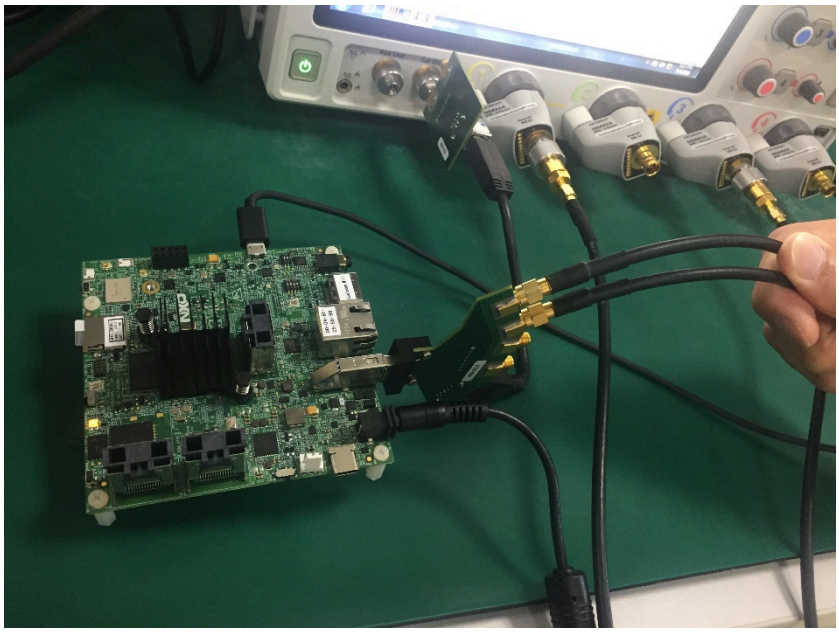

Figure 89. Full Connection Diagram of Host TX Test Topology with Standard-A Port

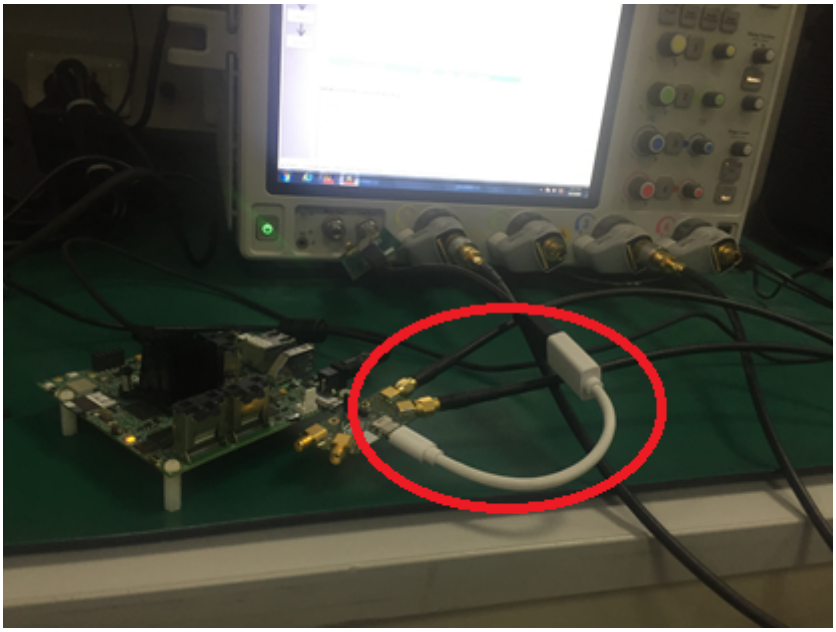

Figure 90. Full Connection Diagram of Host TX Test Topology with Type-C Port

9. In test execution, the test software pops up the right image in Figure 91. Disconnect the DUT and USB test fixture, then **restart DUT**, and click OK.
   When the dialog information appears again, power on DUT normally, then connect DUT to USB test fixture, and make sure that the LFPS signal is captured at the same time. If the captured waveform is the same with the reference, click **OK** in Figure 92.

10. The software automatically completes the test in Figure 93 and Figure 94.

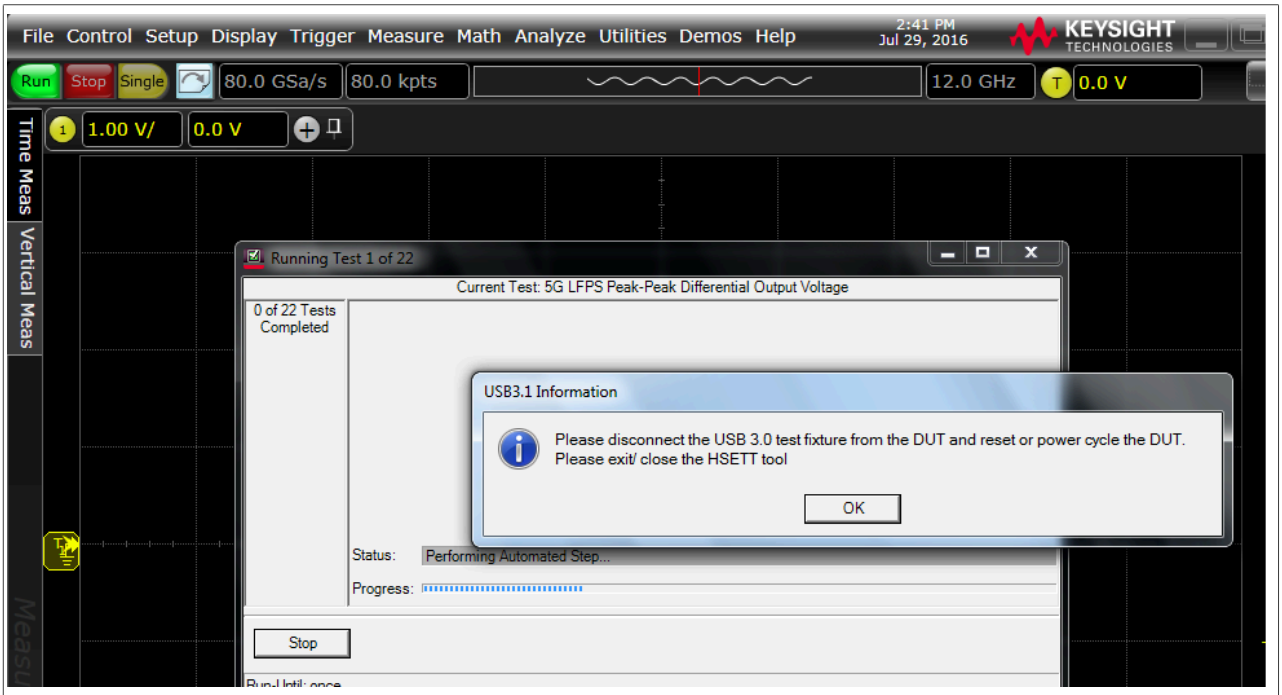

Figure 91. Prompt Box in Test

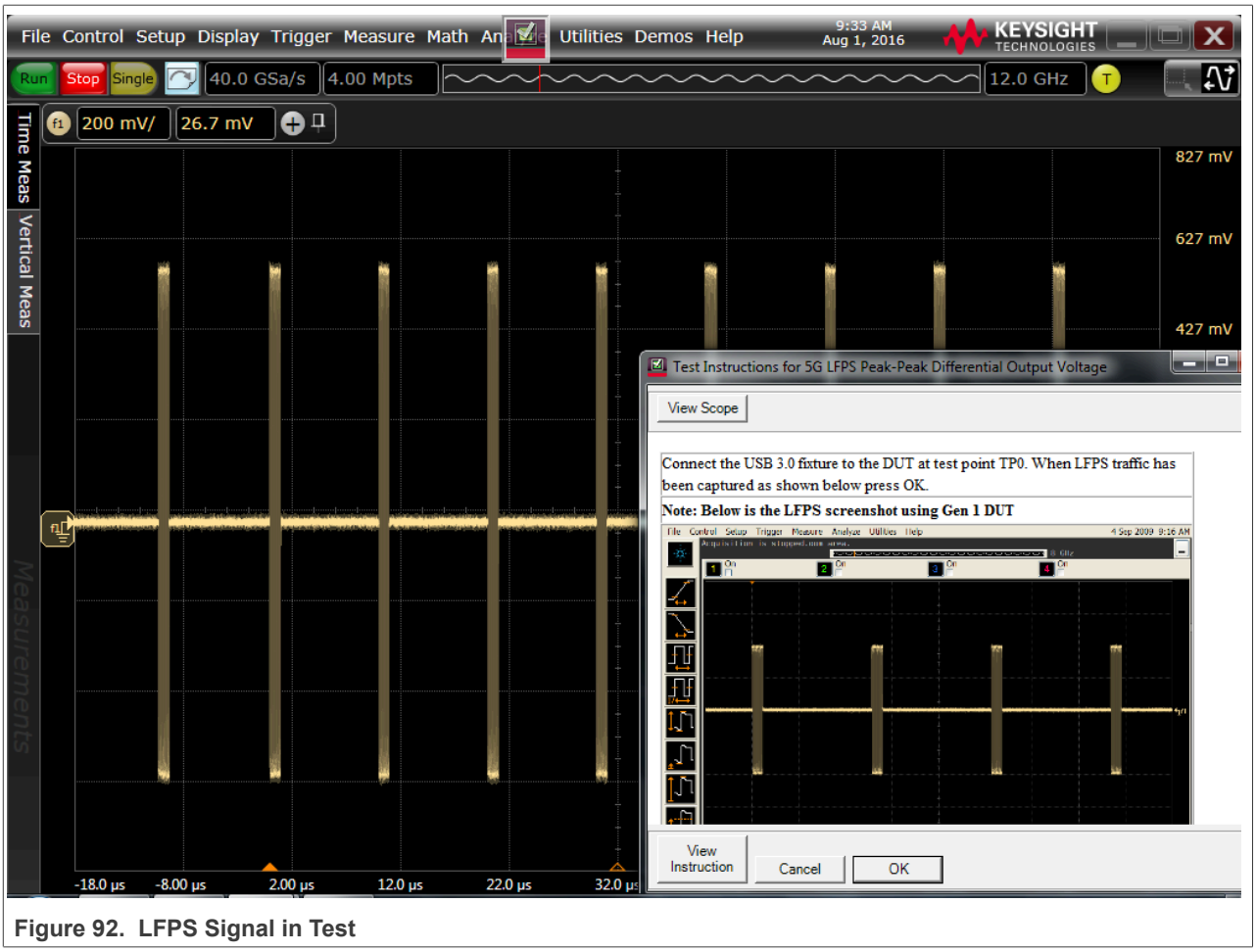

Figure 92. LFPS Signal in Test

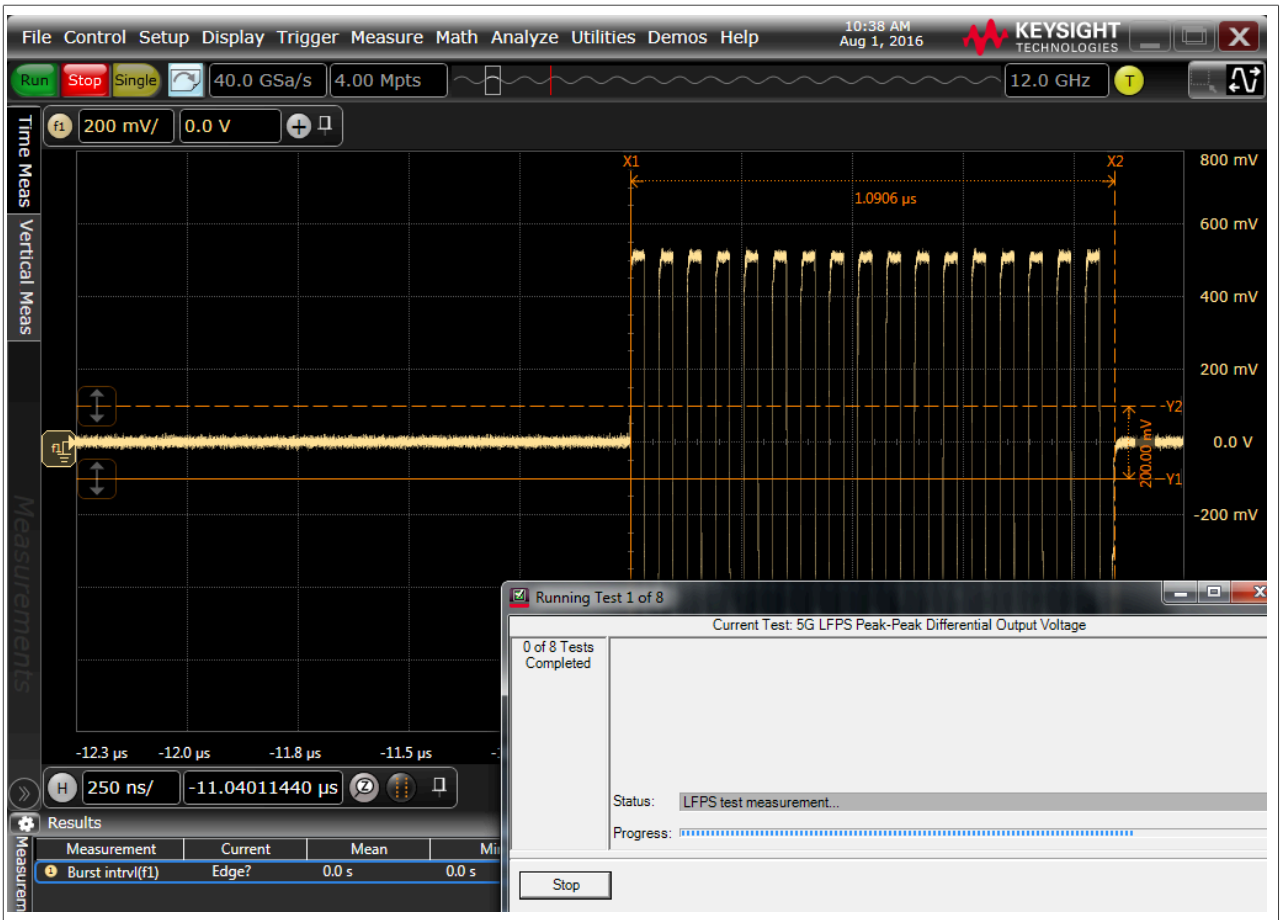

Figure 93. LFPS Signal in Test

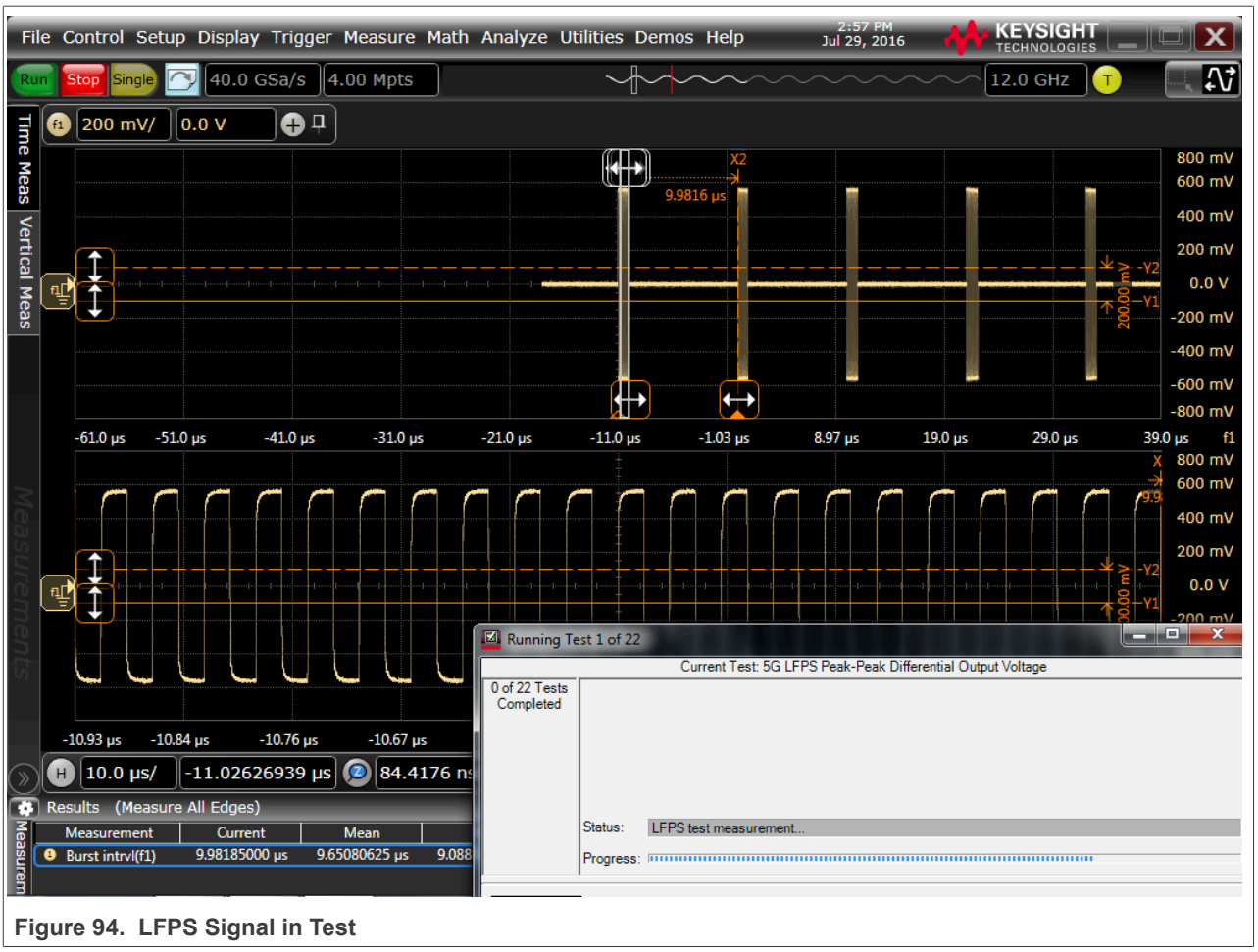

Figure 94. LFPS Signal in Test

3.4.3 Host transmitted SSC/ Eye short / Eye far end tests

Transmitted SSC test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with spec required TX equalization. To comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Transmitted Eye Test at 5 GT/s verifies that the transmitter meets the eye width, deterministic jitter, and random jitter requirements when measured at the compliance test port with nominal transmitter equalization and after processing with the appropriate channels and post-processing as shown in Table 16.

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Table 16. Channels and Reference Equalizer for Testing Device Types

Connector Type	Channel	Reference Equalizer
Std-A	3 m Cable + 5" PCB	Long Channel
Std-B	3 m Cable + 11" PCB	Long Channel
Type-C(Host)	Device Under Test >> USB 3.1 Host Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB) SSGen1_TxComp12p7dB_Embedding.s4p	Long Channel

Table 16. Channels and Reference Equalizer for Testing Device Types ***...continued***

Connector Type	Channel	Reference Equalizer
Type-C(Device)	Device Under Test >> USB 3.1 Device Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB) SSGen1_TxComp12p7dB_Embedding.s4p	Long Channel
Micro-B	1 m Cable + 11” PCB	Long Channel
Micro-AB (Host only)	1 m Cable + 5” PCB + Micro-A to Std-A Receptacle adapter	Long Channel
Micro-AB(DRD)	1 m Cable + 11” PCB (device mode) 1 m Cable + 5” PCB + Micro-A to Std-A Receptacle adapter (host mode) Both tests are required	Long Channel
Tethered (Standard A Plug)	11” PCB	Long Channel
All Types	No Channel (break-out fixture only)	Short Channel

Note:

Note: Refer to https://usb.org/sites/default/files/EnhancedSuperSpeedPHYComplianceTestSpec.pdf for embedding the long channels when using breakout fixtures.

Test Instructions:

1. The connection will remain unchanged in Figure 95, and the **“I have completed these instructions”** will be directly checked, and then click **Next**. After LFPS TX test is over, then continue to start **SSC Test** automatically.
2. In the stage of automatic test, if below dialog in Figure 96 appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP1 test pattern** manually.
   Make sure that the Cal output channel is connected to the SSRX port of fixture, then click **“Toggle”** button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click **OK** and continue to do next test.
3. If below dialog in Figure 97 appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP0 test pattern**. Make sure that the Cal output channel is connected to the SSRX port of fixture, then click toggle button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click **OK** and continue to do next test.
4. After SSC test is over, then continue to start **“Transmitter Eye Short Channel Test”** automatically in Figure 98.
   After each test item is over, the software shows change physical connection/setup dialog window, select **I have completed these instructions** and click **Next** to start new test in Figure 99.
5. After “Transmitter Eye Short Channel Test” is end, then begin to the **“Transmitter Eye Far End Test”** automatically. the software shows change physical connection/setup dialog window, select **“I have completed these instructions”** and click **“Next”** to next step in Figure 100.
6. All the electrical compliance test is finished, save the test report from the menu **“File”->”Save Project As”** in Figure 101.And export results.

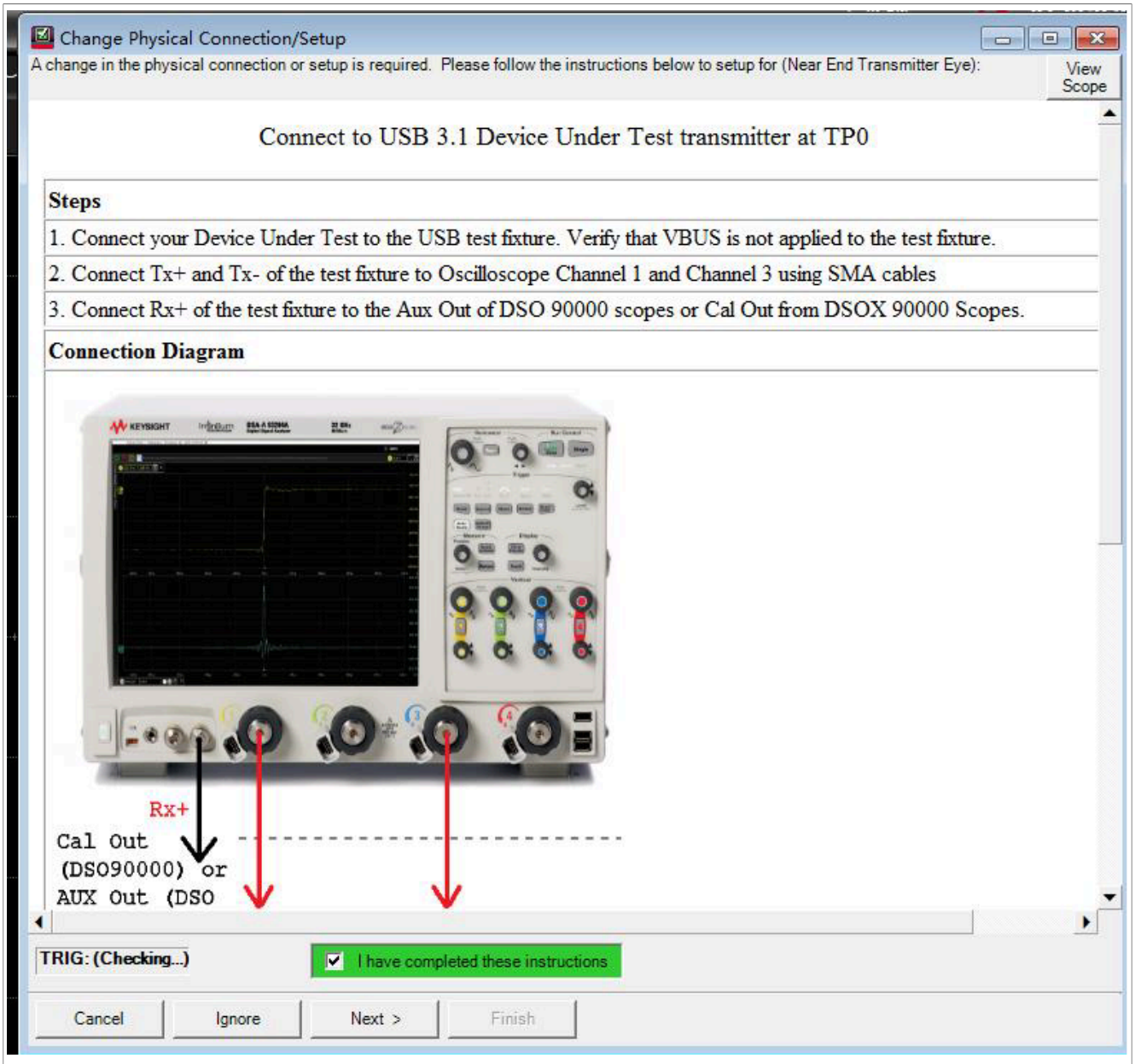

Figure 95. SSC Test

Figure 96. SSC Test procedure

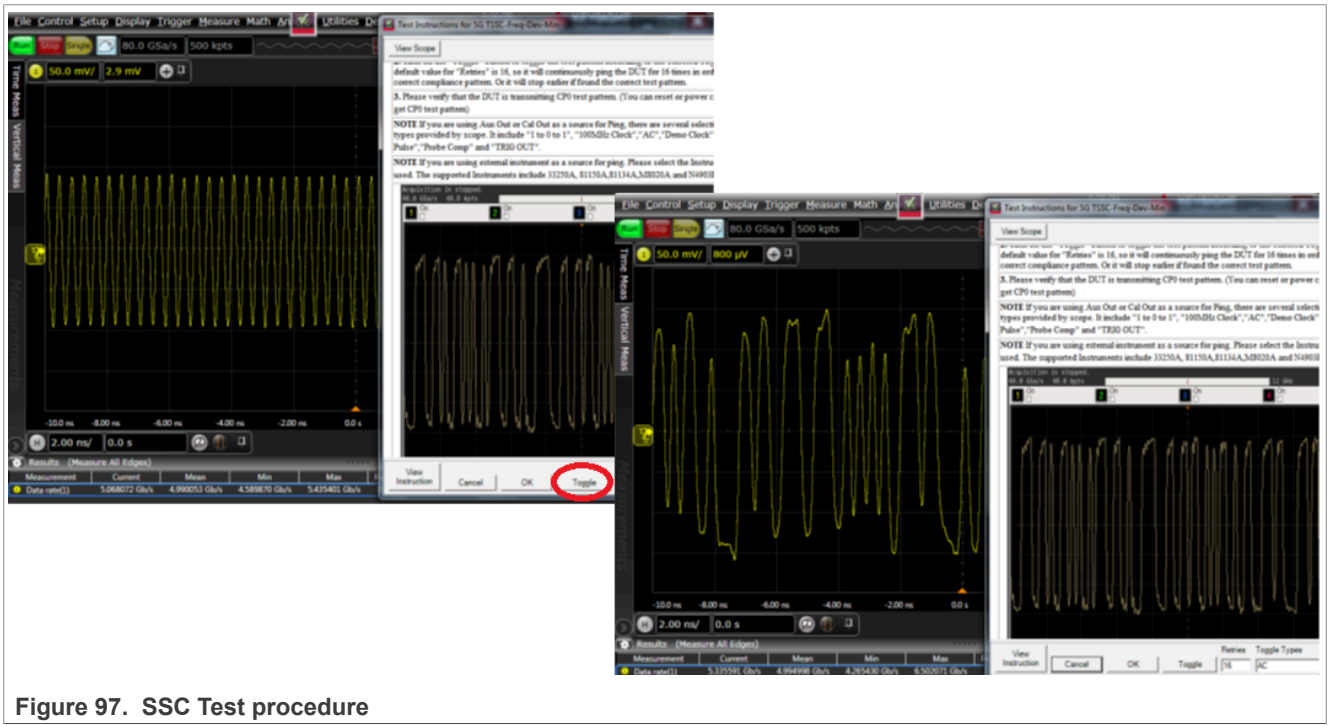

Figure 97. SSC Test procedure

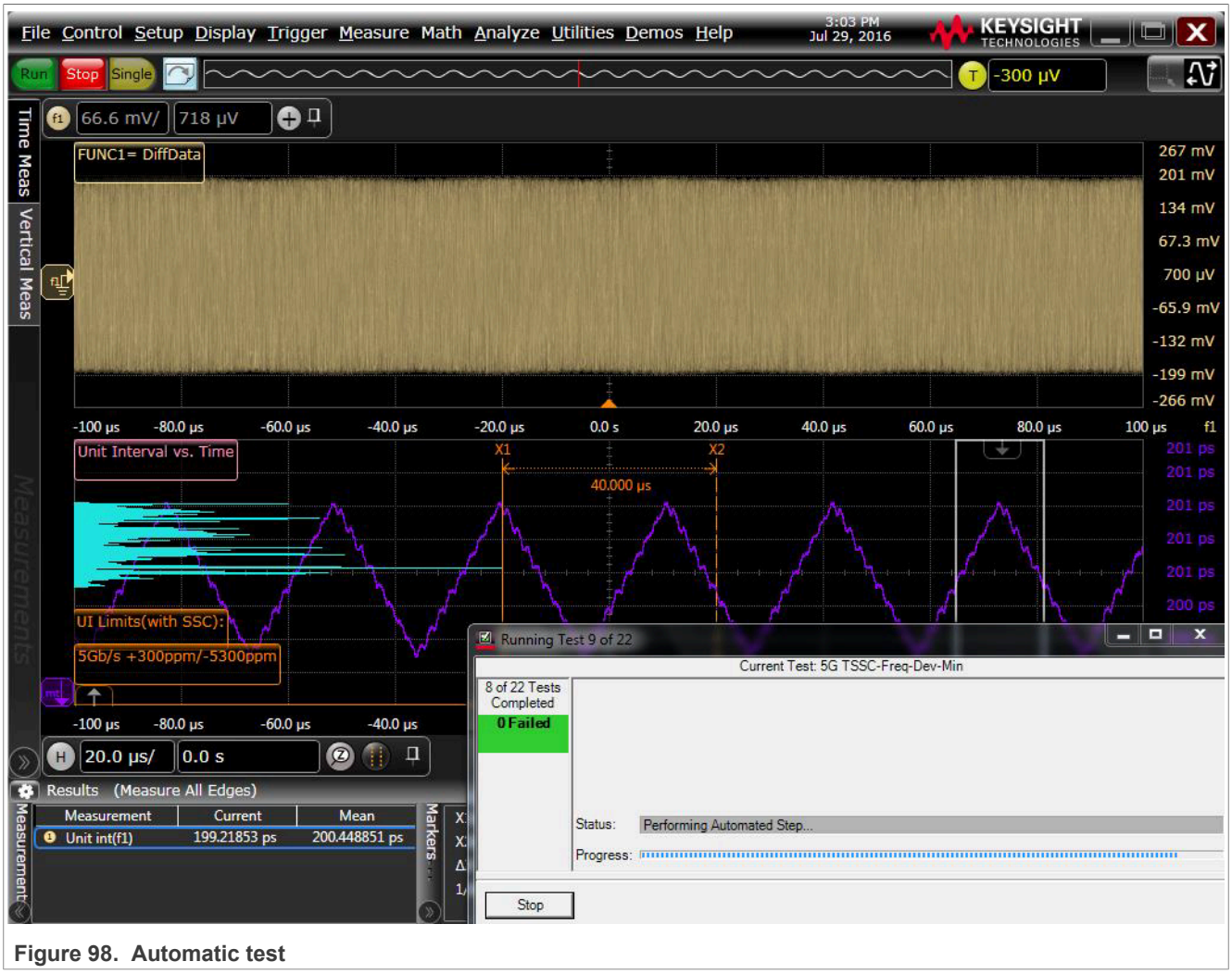

Figure 98. Automatic test

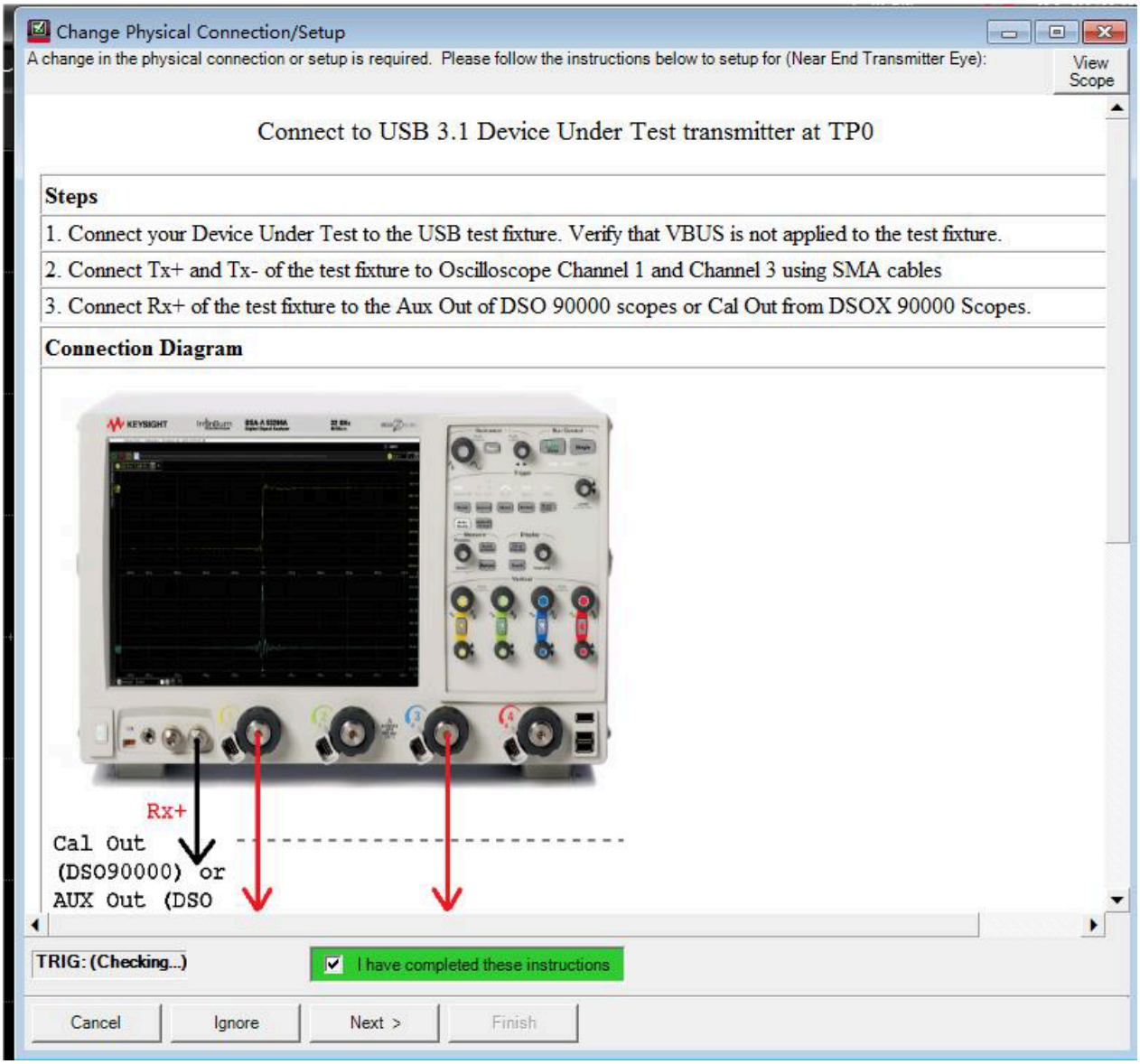

Figure 99. Transmitter Eye Short Channel/Far End Test

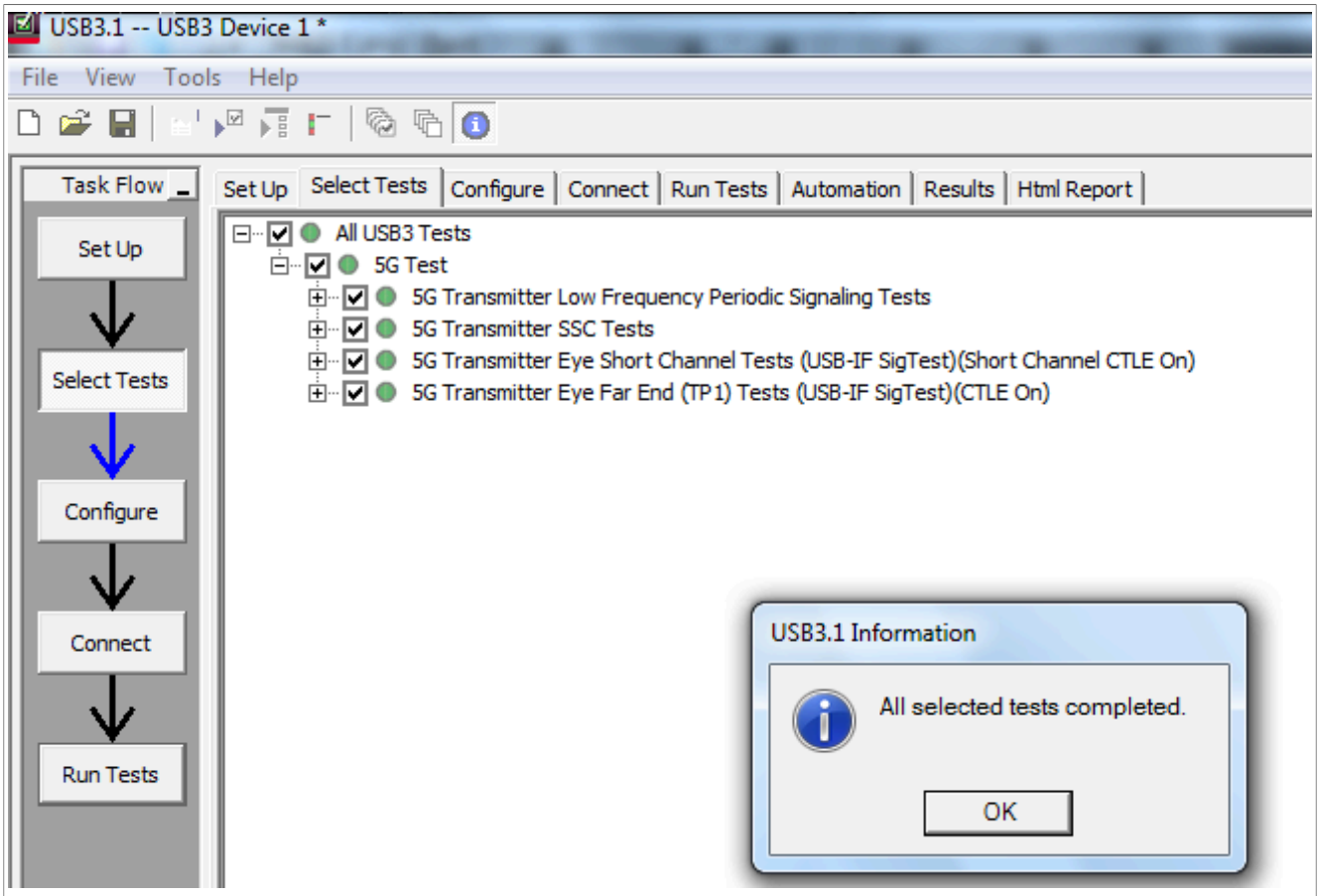

Figure 100. Test Completed

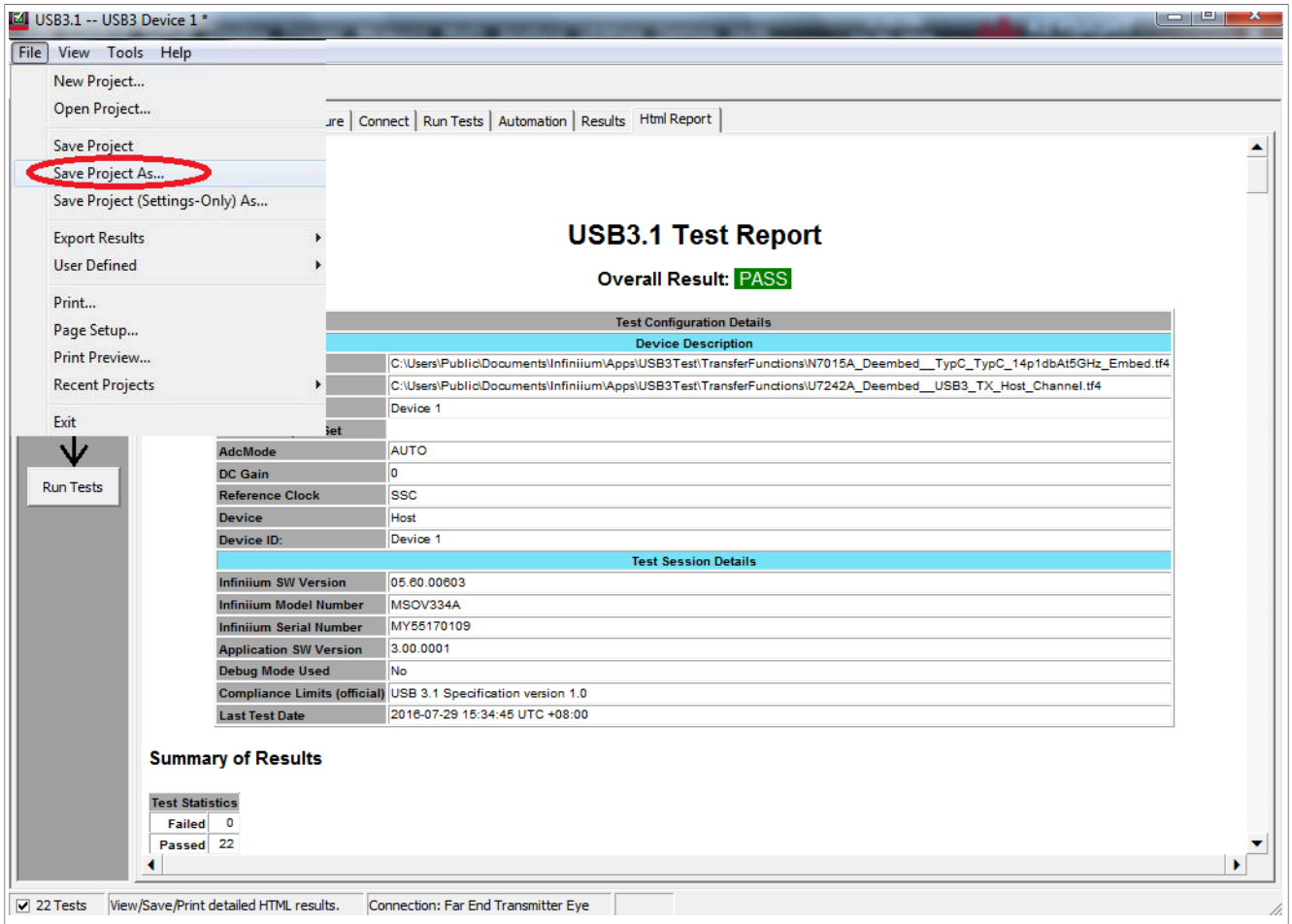

Figure 101. Save Project

3.4.4 Device low frequency periodic signaling TX test

This test verifies that the low frequency periodic signal transmitter meets the timing requirements when measured at the compliance test port.

Test Instructions:

1. Select the test items in the USB Automated Test Software on Oscilloscope as shown in Figure 102 below, and make sure you set the Test Type configuration option in Figure 103. If the DUT is a Standard A port, “Configure Transfer Function” should be “**Std A to Std B**”. If the DUT is a Type-C port, “Configure Transfer Function” should be “**C to C**”.
2. Select the test items in the USB Automated Test Software in Figure 104
3. Set the test configures default in Figure 105.
4. Connect your Device Under Test to the Device Test Fixture 1. VBUS is not required. If the DUT is a Standard A port, we choose **Test Topology of Standard-A Port** in Figure 106. If the DUT is a Type-C port, we choose **Test Topology of Type-C Port** in Figure 107. And you need **a Jumper** to cover the CC pin to VCC on which path you choose.
5. Connect 5 Inch Device Test Fixture 2 to Device test Fixture 1 using type A to type B cable. When Type-C port is tested, a hub from type A to Type C is needed in Figure 109.
6. Connect **RX+** of the Test Fixture 2 to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes in Figure 108.

7. Connect **TX+** and **TX-** of the Test Fixture 1 to Oscilloscope Channel 1 and Channel 3 using SMA cables. The full connection diagram is show in Figure 109.
8. Click **Run Tests** in the USB Automated Test Software on Oscilloscope. After the test is finished, you can view the report in HTML Report page.

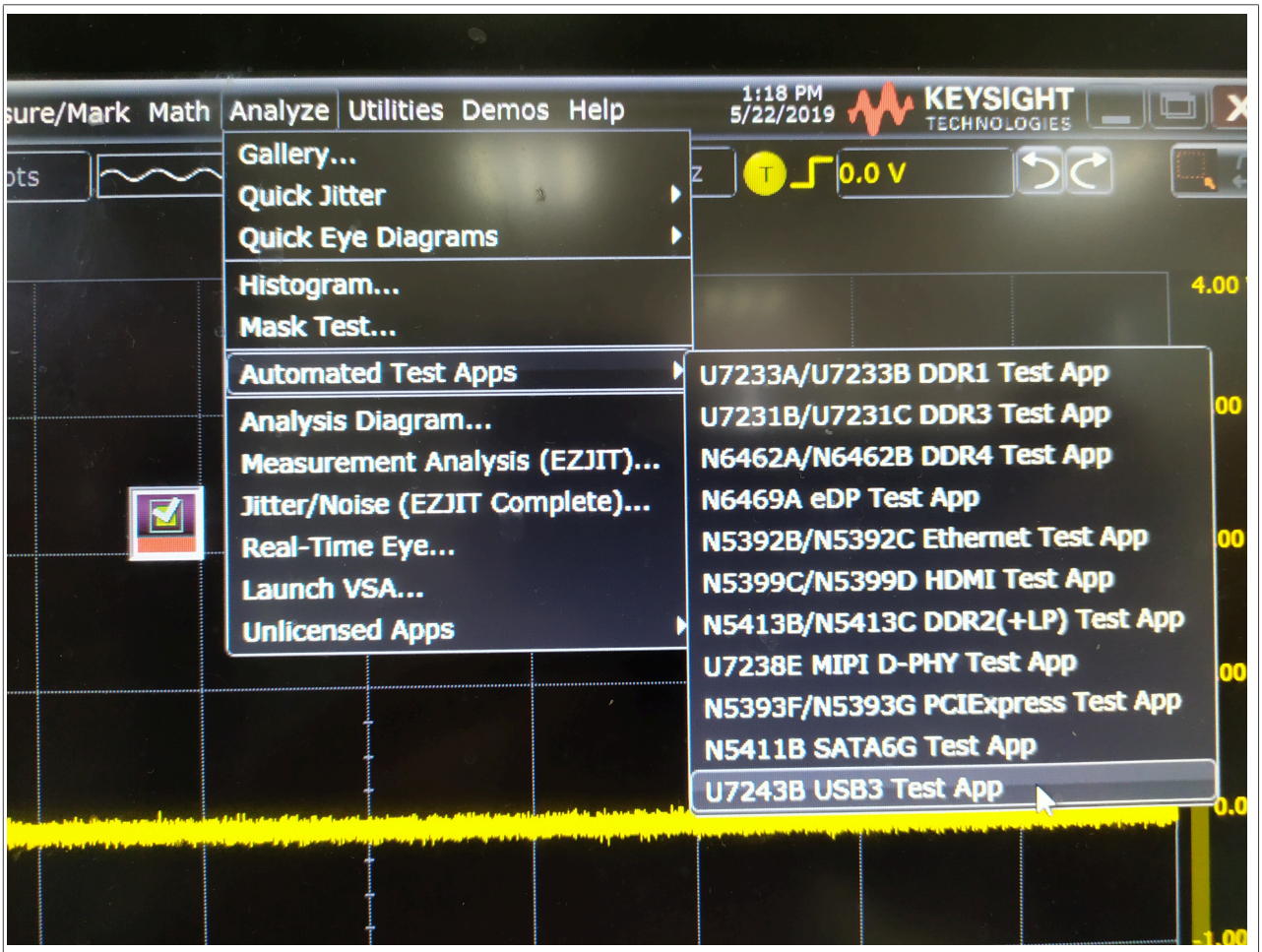

Figure 102. Automated Test Software for USB 3.0

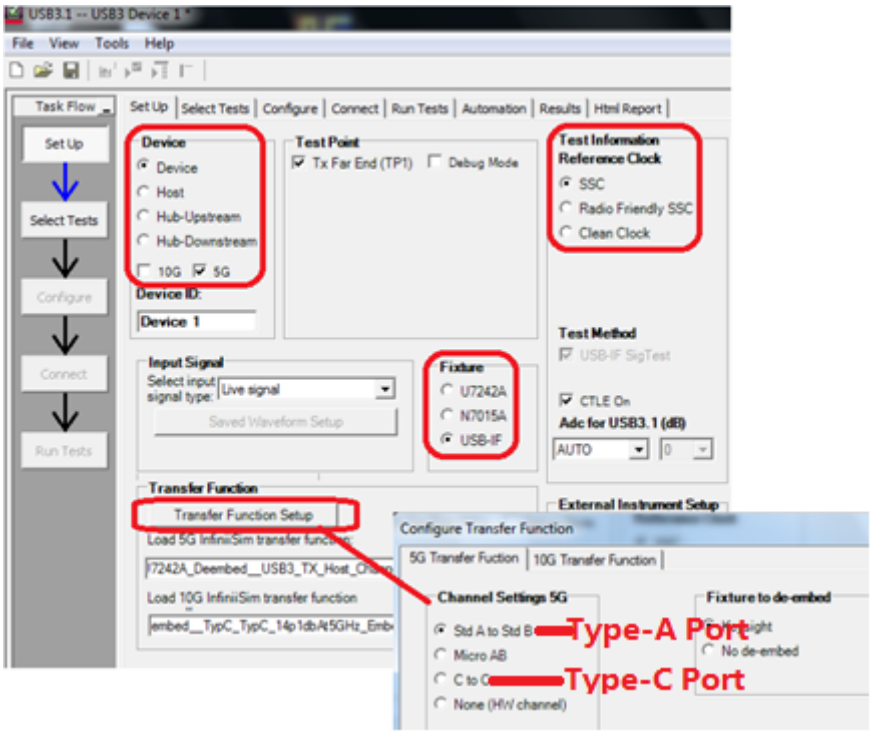

Figure 103. Automated Test Software setting for Standard-A Super Speed Signal Test

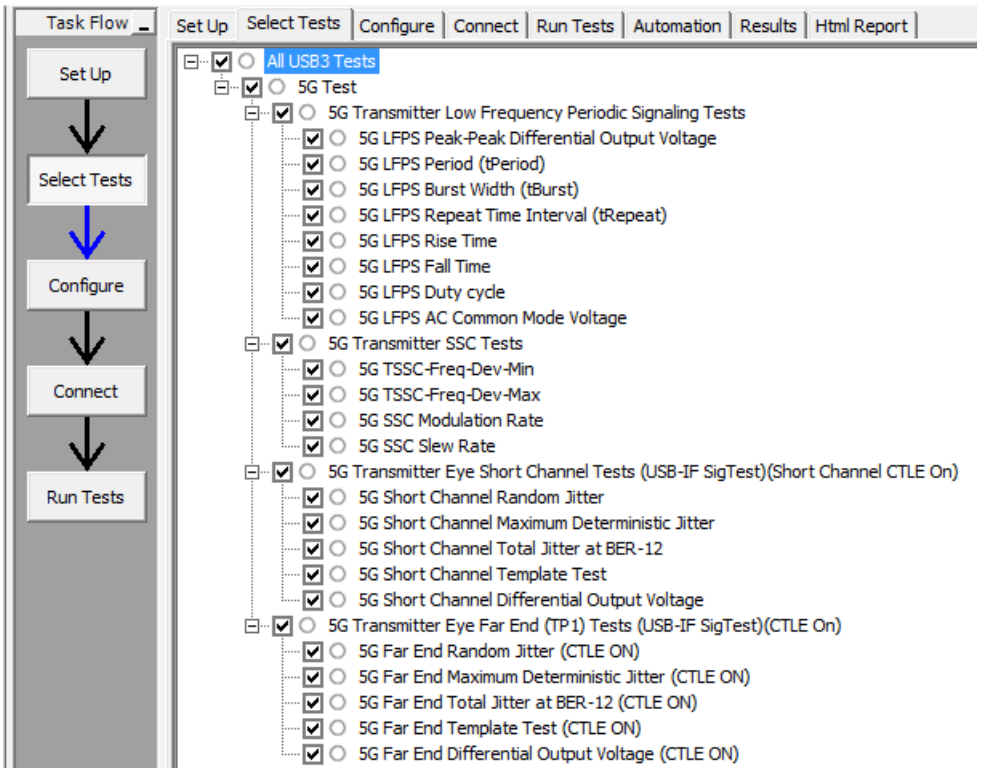

Figure 104. Automated Test Software setting for Testing Items

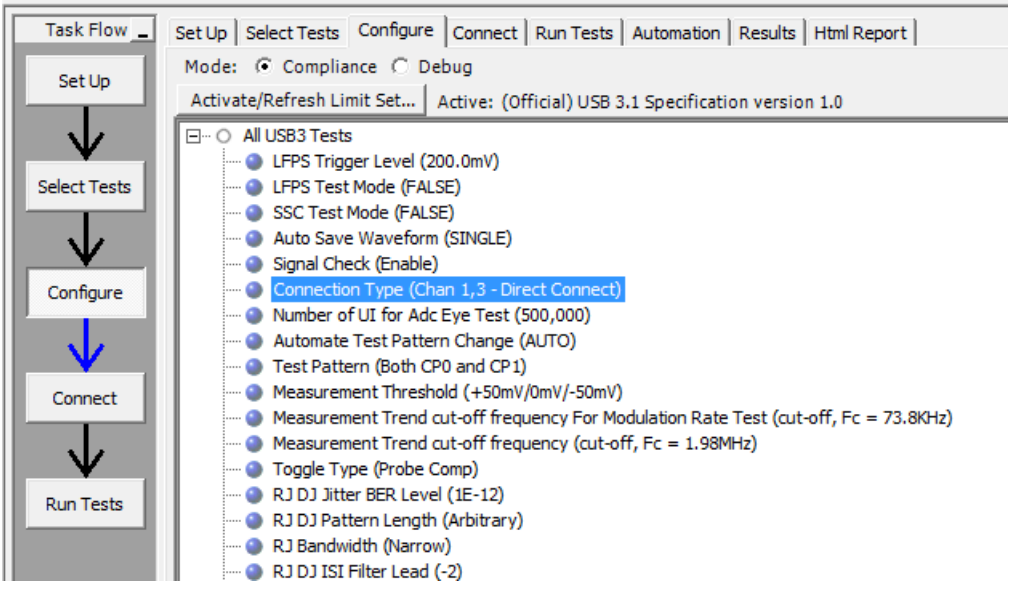

Figure 105. Automated Test Software setting for Testing Configure

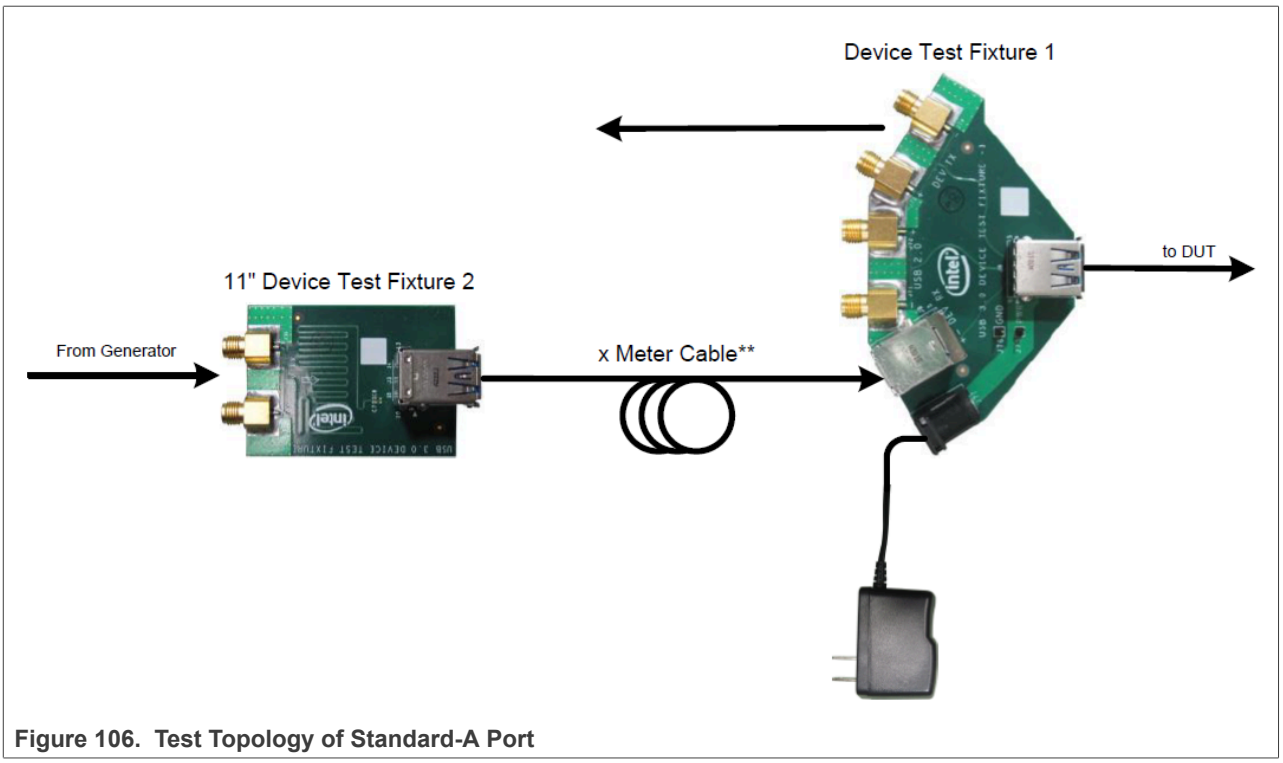

Figure 106. Test Topology of Standard-A Port

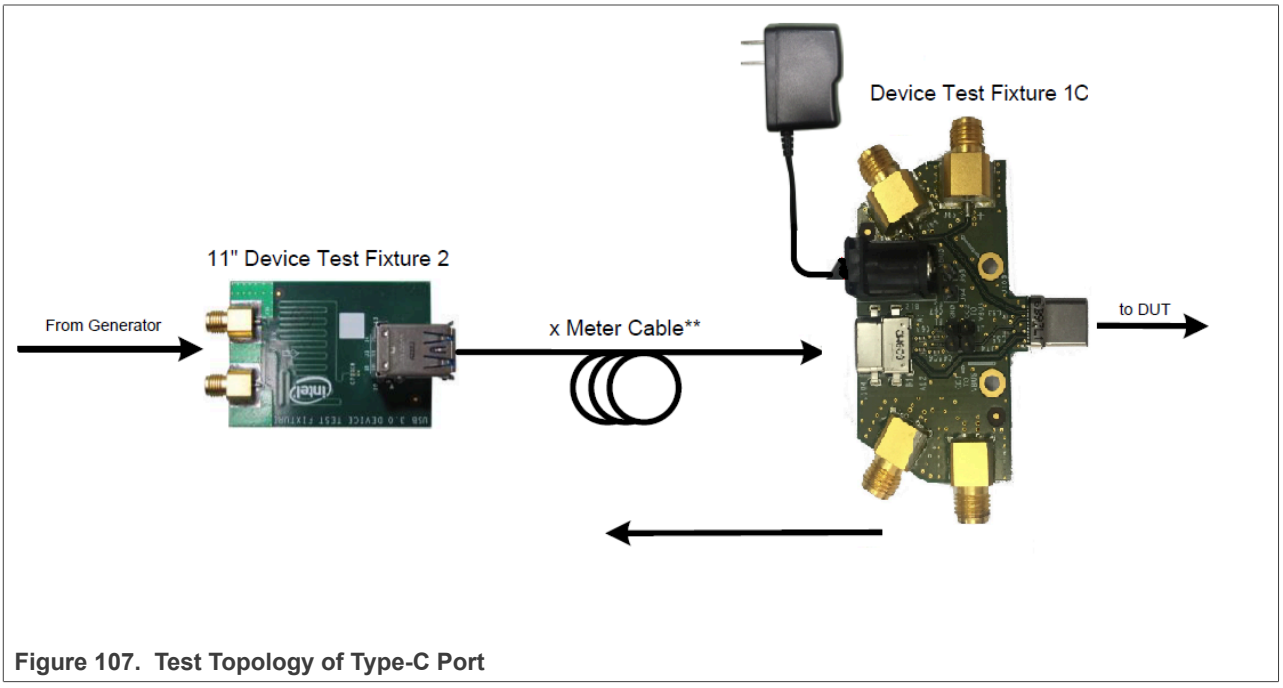

Figure 107. Test Topology of Type-C Port

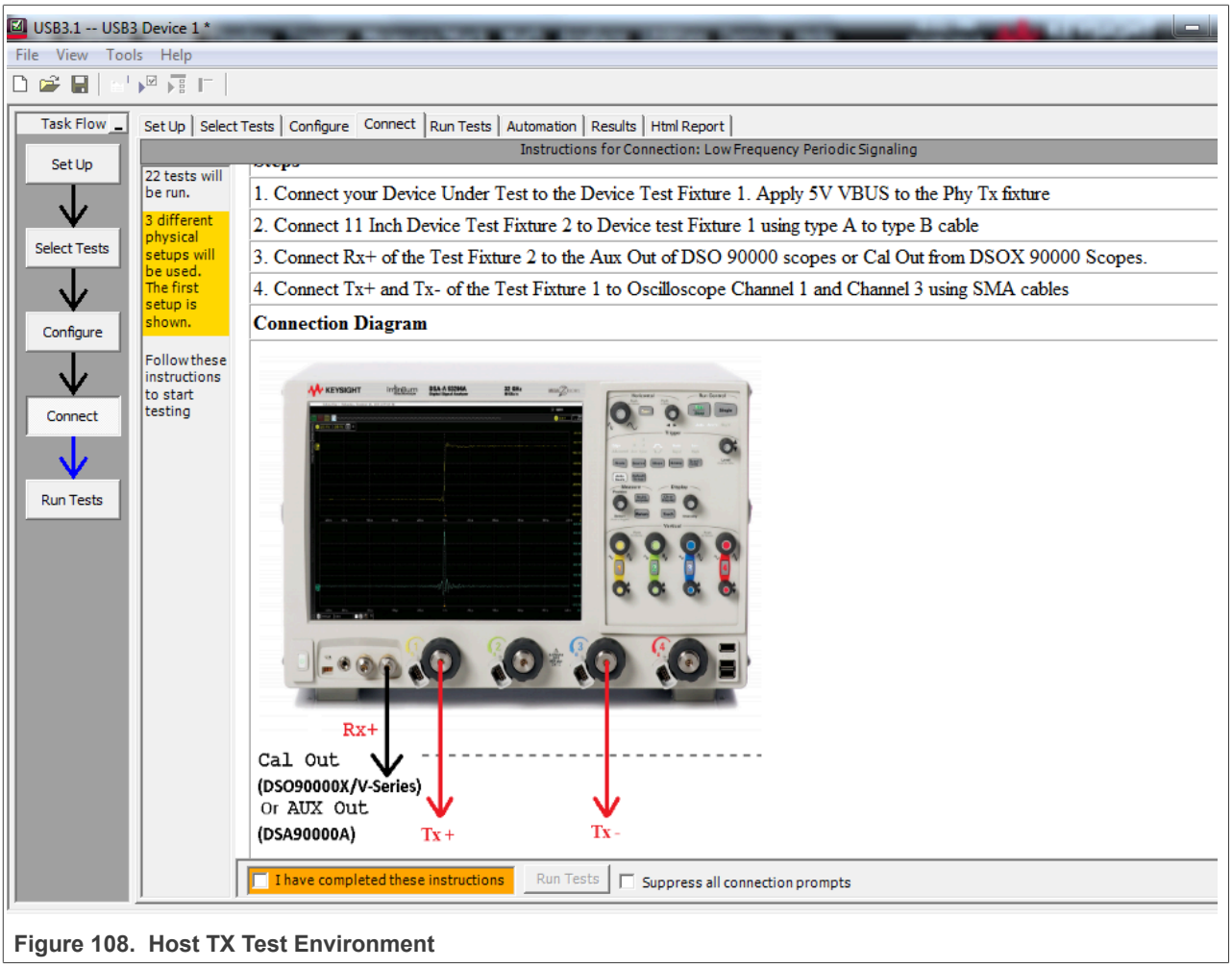

Figure 108. Host TX Test Environment

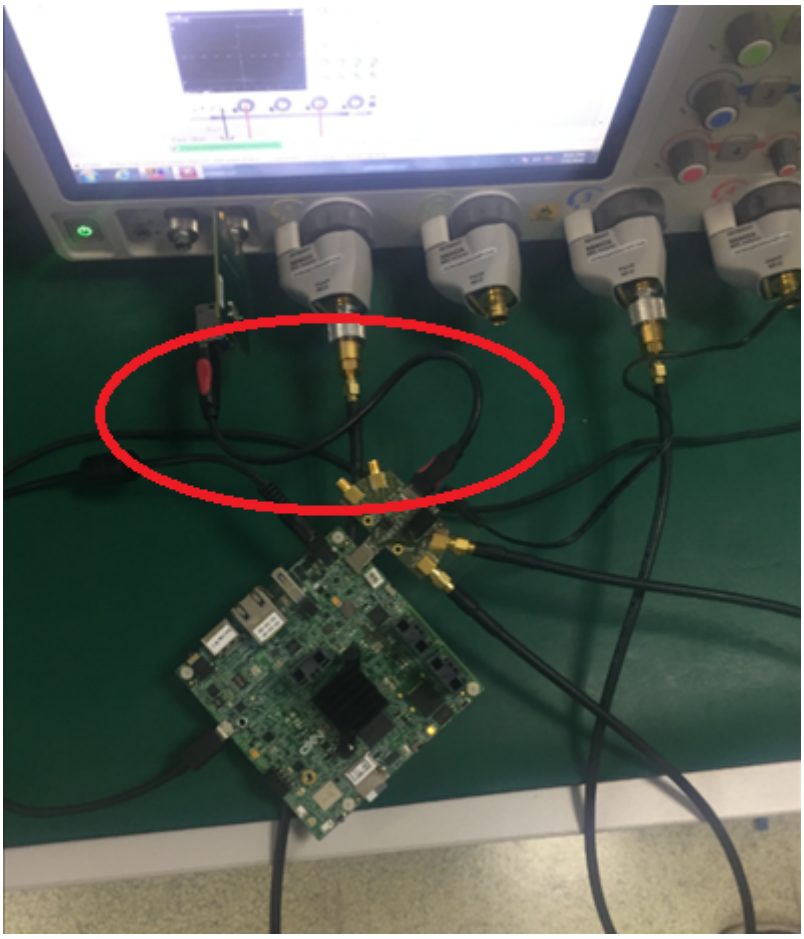

Figure 109. Full Connection Diagram of Host RX Test Topology with Type-C Port

9. In test execution, the test software will pop up the right image in Figure 109. Disconnect the DUT and USB test fixture, then **restart DUT**, and click **OK**.
   When the dialog information appears again, power on DUT normally, then connect DUT to USB test fixture, and make sure that the LFPS signal is captured at the same time. If the captured waveform is the same with the reference, click **"OK"** in Figure 110.
10. The software will automatically complete the test in Figure 111 and Figure 112.

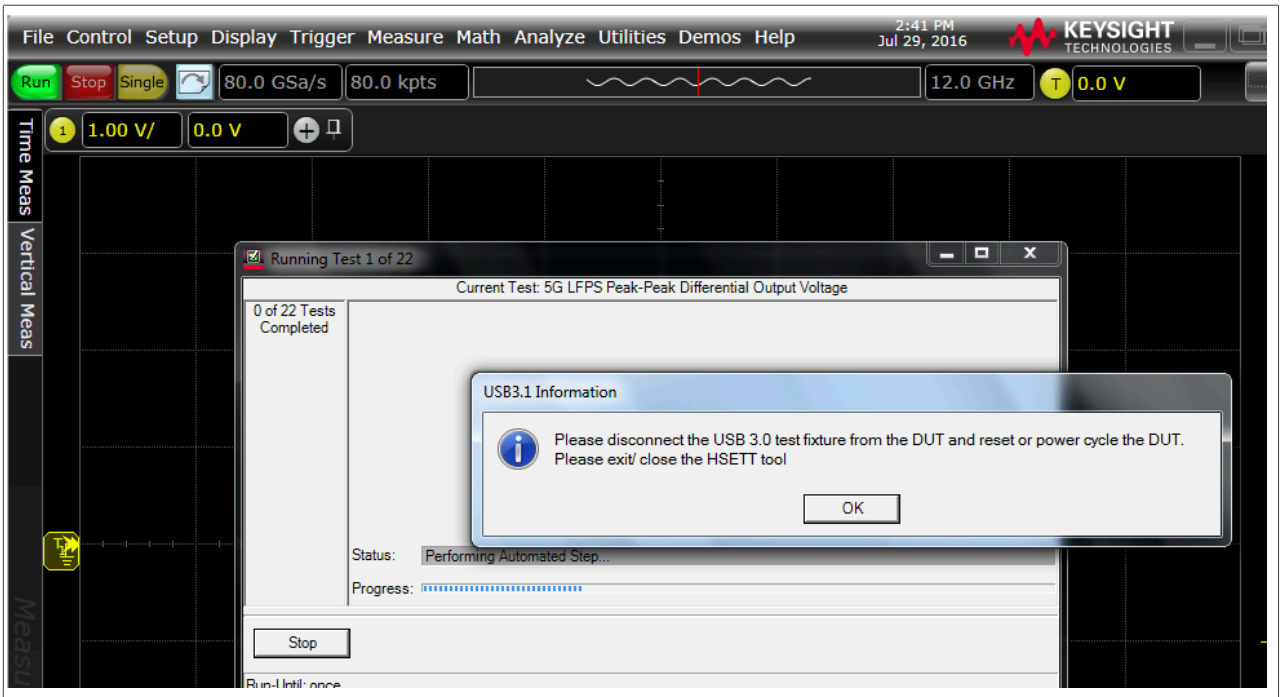

Figure 110. Prompt Box in Test

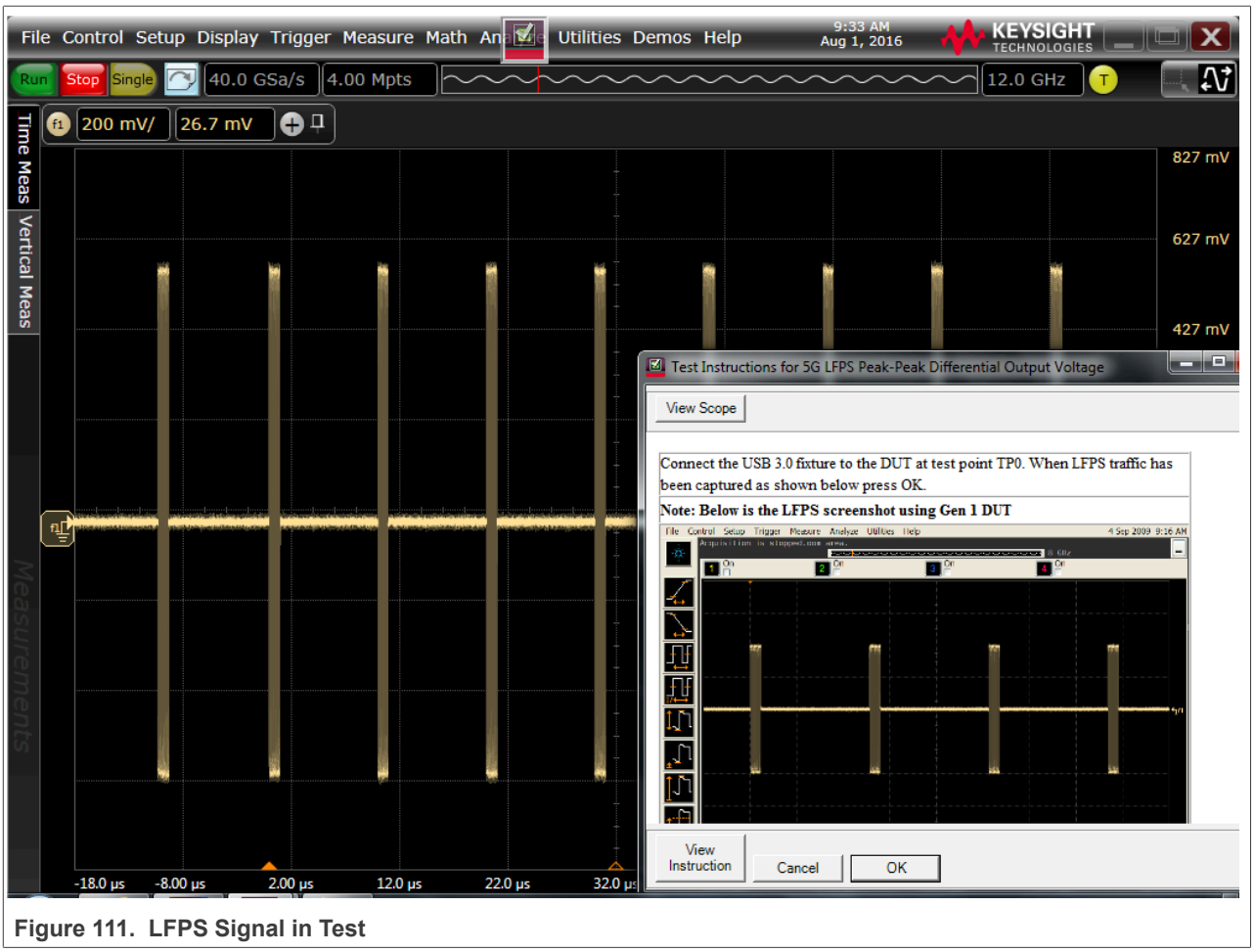

Figure 111. LFPS Signal in Test

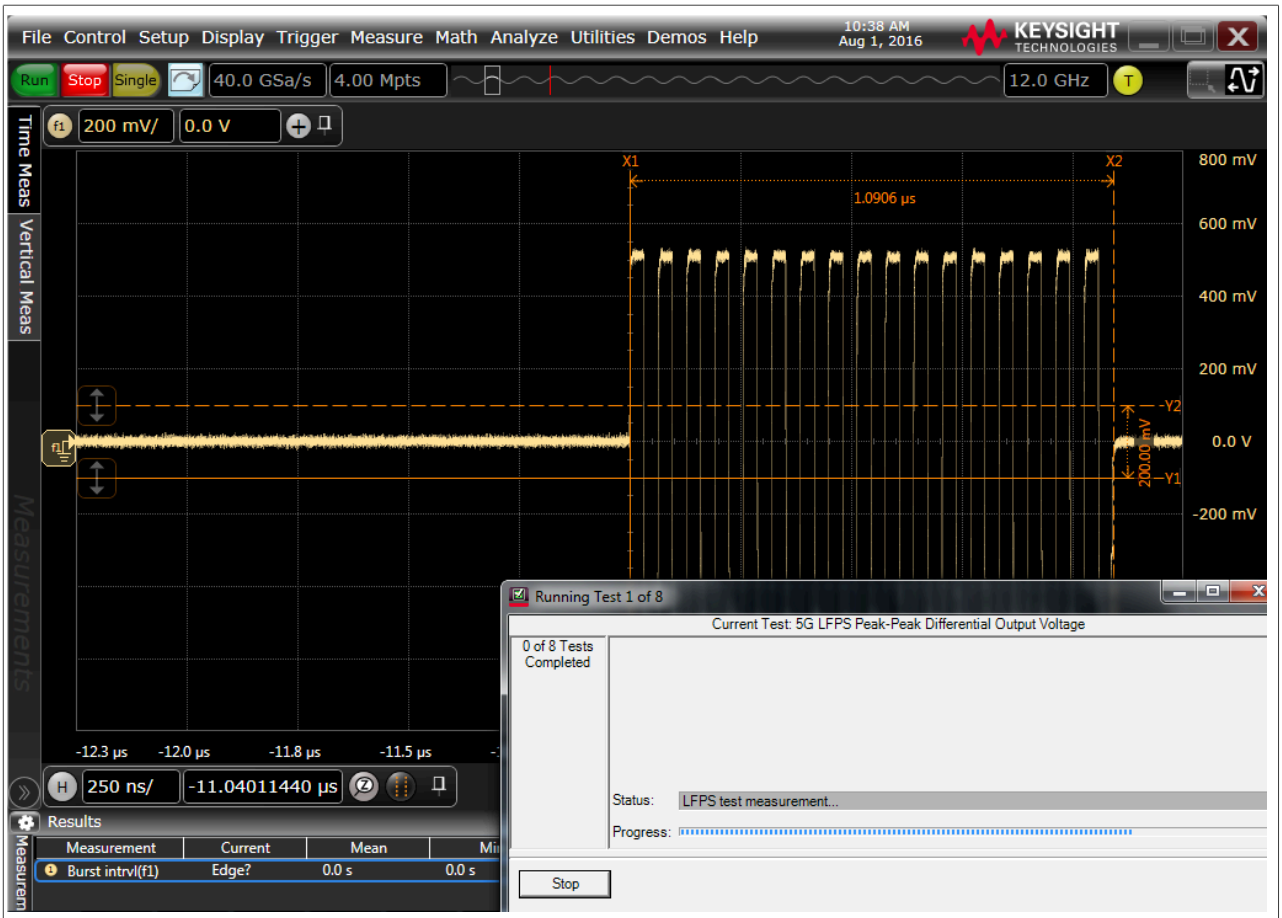

Figure 112. LFPS Signal in Test

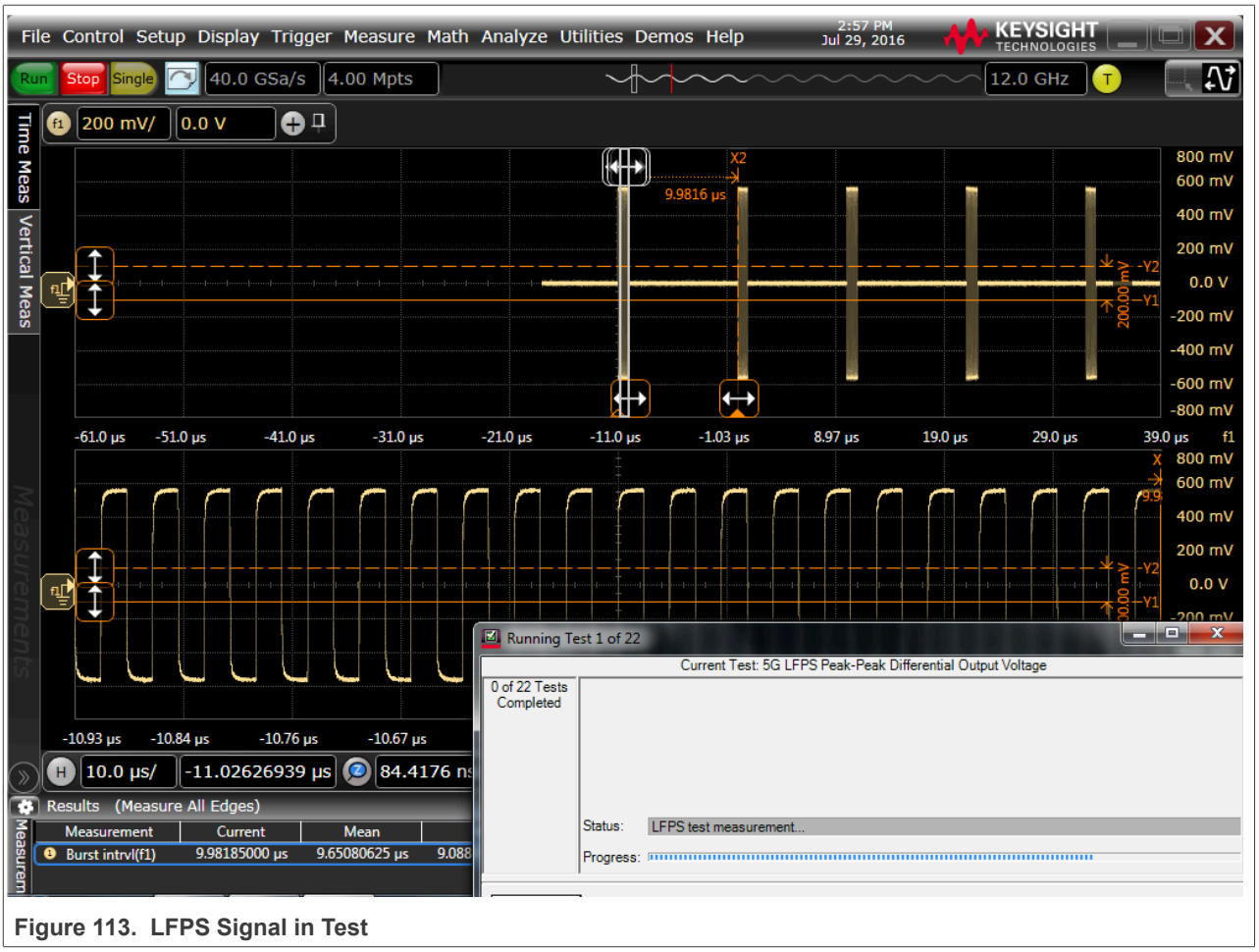

Figure 113. LFPS Signal in Test

3.4.5 Device transmitted SSC/ Eye short / Eye far end tests

Transmitted SSC test verifies that the transmitter meets SSC profile requirements when measured at the compliance test port with spec required TX equalization. In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Transmitted Eye Test at 5 GT/s verifies that the transmitter meets the eye width, deterministic jitter, and random jitter requirements when measured at the compliance test port with nominal transmitter equalization and after processing with the appropriate channels and post-processing as shown in Table 17.

In order to comprehend noise effects, such as crosstalk, it is up to the DUT manufacturer to make sure that any other links are active for the various DUT types.

Table 17. Channels and Reference Equalizer for Testing Device Types

Connector Type	Channel	Reference Equalizer
Std-A	3 m Cable + 5” PCB	Long Channel
Std-B	3 m Cable + 11” PCB	Long Channel
Type-C(Host)	Device Under Test >> USB 3.1 Host Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB)	Long Channel

Table 17. Channels and Reference Equalizer for Testing Device Types*...continued*

Connector Type	Channel	Reference Equalizer
	SSGen1_TxComp12p7dB_Embedding.s4p	
Type-C(Device)	Device Under Test >> USB 3.1 Device Fixture 1C >> SCOPE (Embed 7 dB Cable + Host/Device PCB) SSGen1_TxComp12p7dB_Embedding.s4p	Long Channel
Micro-B	1 m Cable + 11” PCB	Long Channel
Micro-AB (Host only)	1 m Cable + 5” PCB + Micro-A to Std-A Receptacle adapter	Long Channel
Micro-AB(DRD)	1 m Cable + 11” PCB (device mode) 1 m Cable + 5” PCB + Micro-A to Std-A Receptacle adapter (host mode) Both tests are required	Long Channel
Tethered (Standard A Plug)	11” PCB	Long Channel
All Types	No Channel (break-out fixture only)	Short Channel

Note:

Note: Refer to http://www.usb.orgusb.kavi.com/developers/estoreinfo/SuperSpeedTestTopologies.pdf

Test Instructions:

1. The connection remains unchanged in Figure 113. After the **"I have completed these instructions"** is directly checked, click **"Next"**. After LFPS TX test is over, continue to start **“SSC Test”** automatically.
2. In the stage of automatic test, if below dialog in Figure 114 appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP1 test pattern** manually.
   Make sure that the Cal output channel is connected to the SSRX port of fixture, then click “Toggle” button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click “OK” and continue to do next test.
3. if below dialog in Figure 115 appears, it is to say that the captured waveform does not match to the reference waveform, and it is not the required test pattern. Trig **CP0 test pattern** manually.
   Make sure that the Cal output channel is connected to the SSRX port of fixture, then click **toggle** button to switch to the proper test pattern until the captured waveform is the same with the reference waveform, click **“OK”** and continue to do next test.
4. After SSC test is over, then continue to start **“Transmitter Eye Short Channel Test”** automatically in Figure 116.
   After each test item is over, the software shows change physical connection/setup dialog window, select **“I have completed these instructions”** and click **“Next”** to start new test in Figure 117.
5. After “Transmitter Eye Short Channel Test” is end, then begin to the **“Transmitter Eye Far End Test”** automatically. the software shows change physical connection/setup dialog window, select **“I have completed these instructions”** and click **“Next”** to next step in Figure 118
6. All the electrical compliance test is finished, save the test report from the menu **“File”->”Save Project A**s” in Figure 119. And export results.

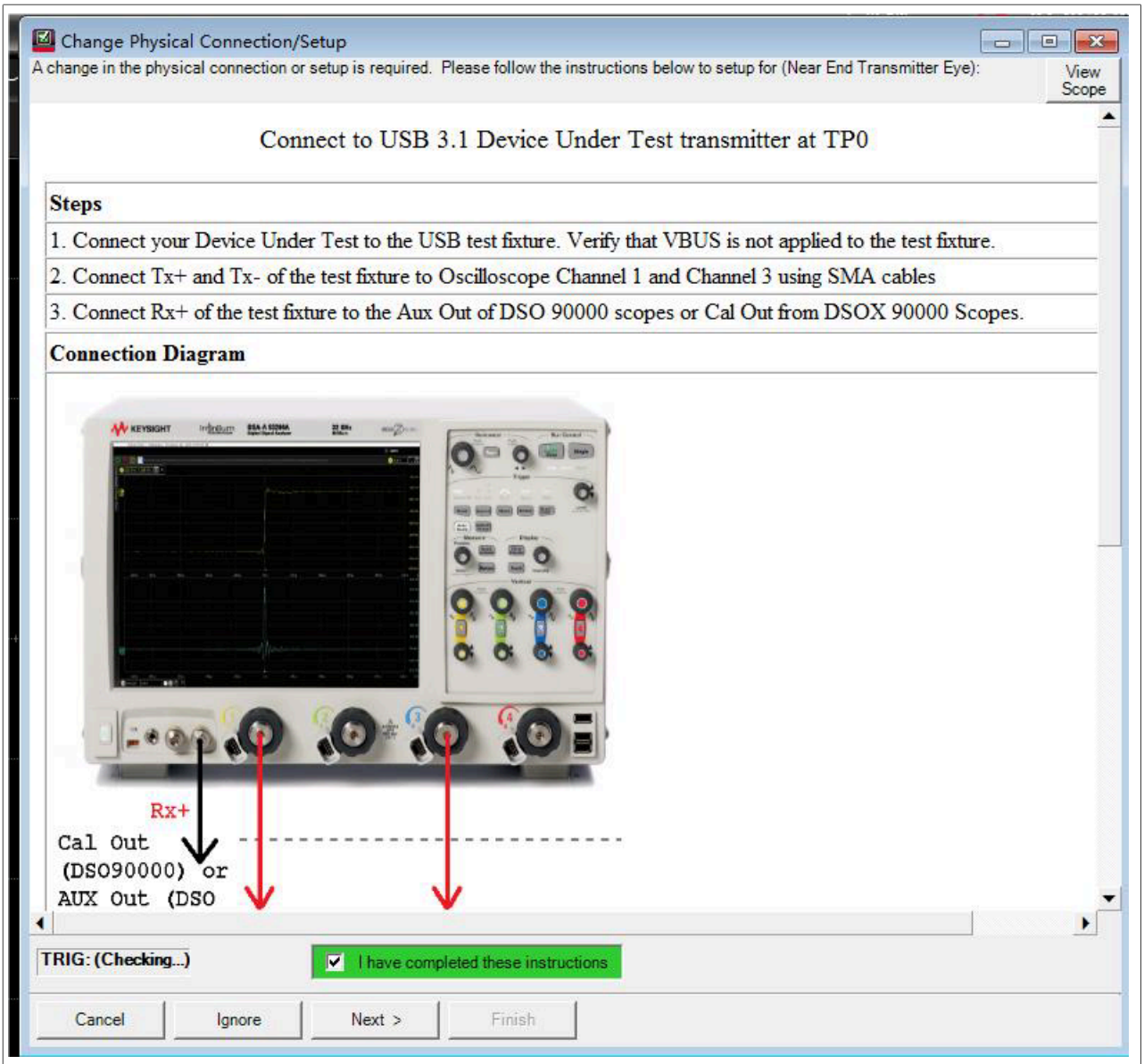

Figure 114. SSC Test

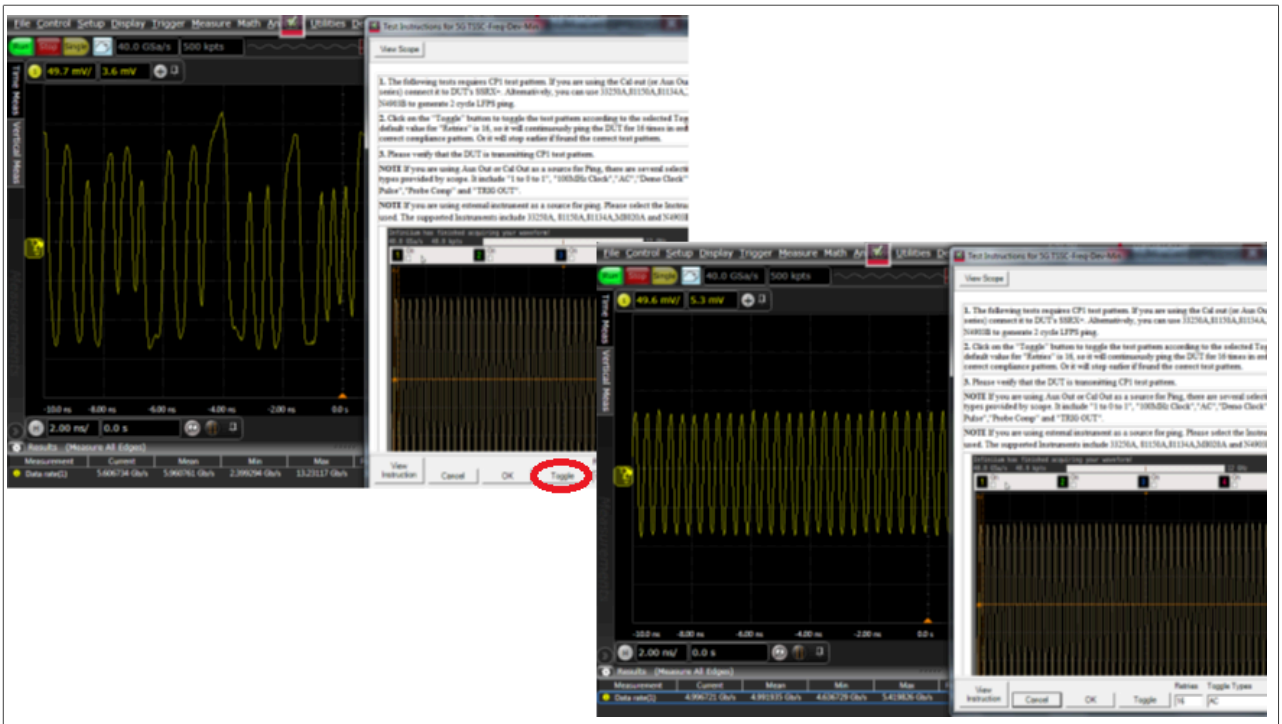

Figure 115. SSC Test procedure

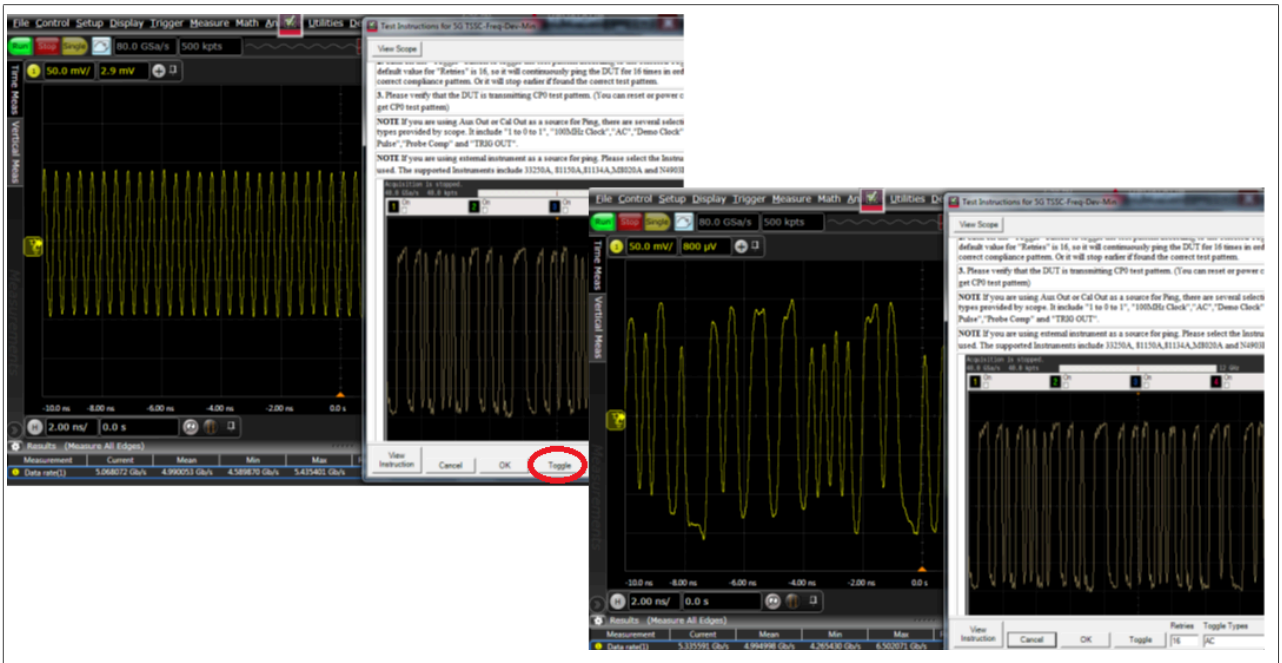

Figure 116. SSC Test procedure

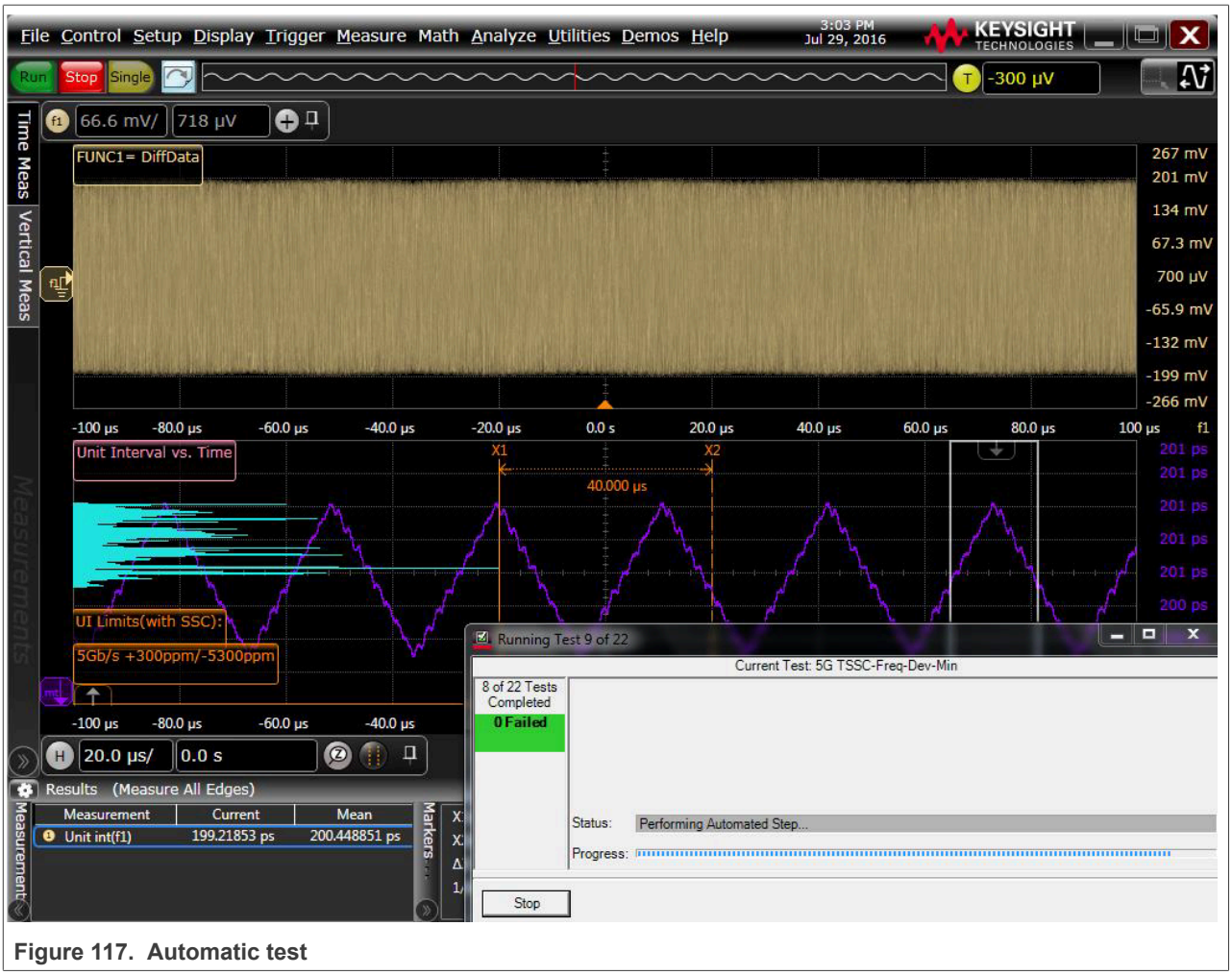

Figure 117. Automatic test

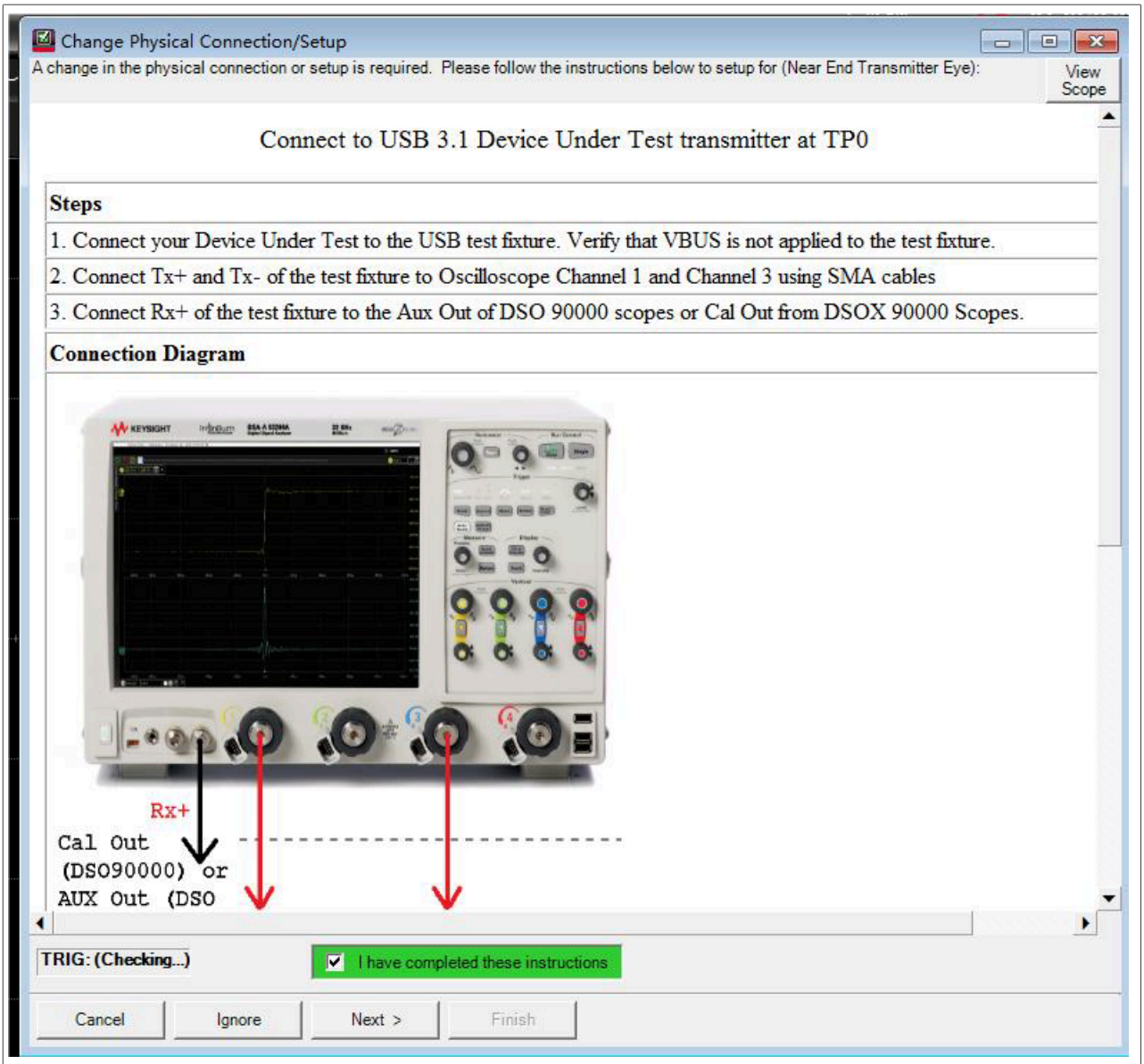

Figure 118. Transmitter Eye Short Channel/Far End Test

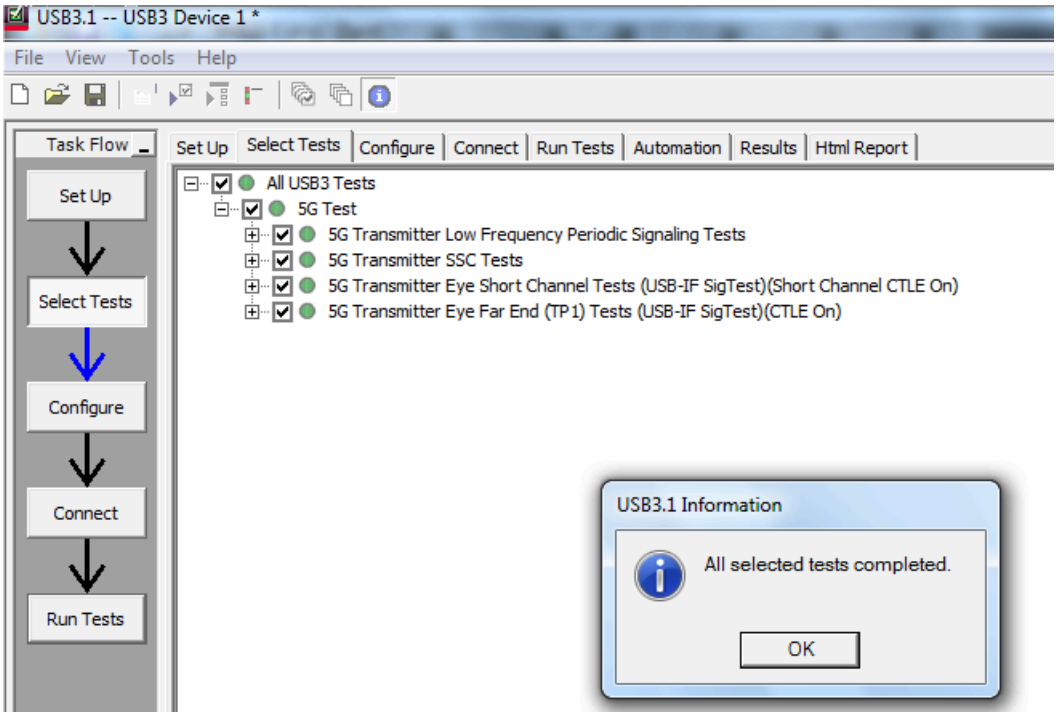

Figure 119. Test Completed

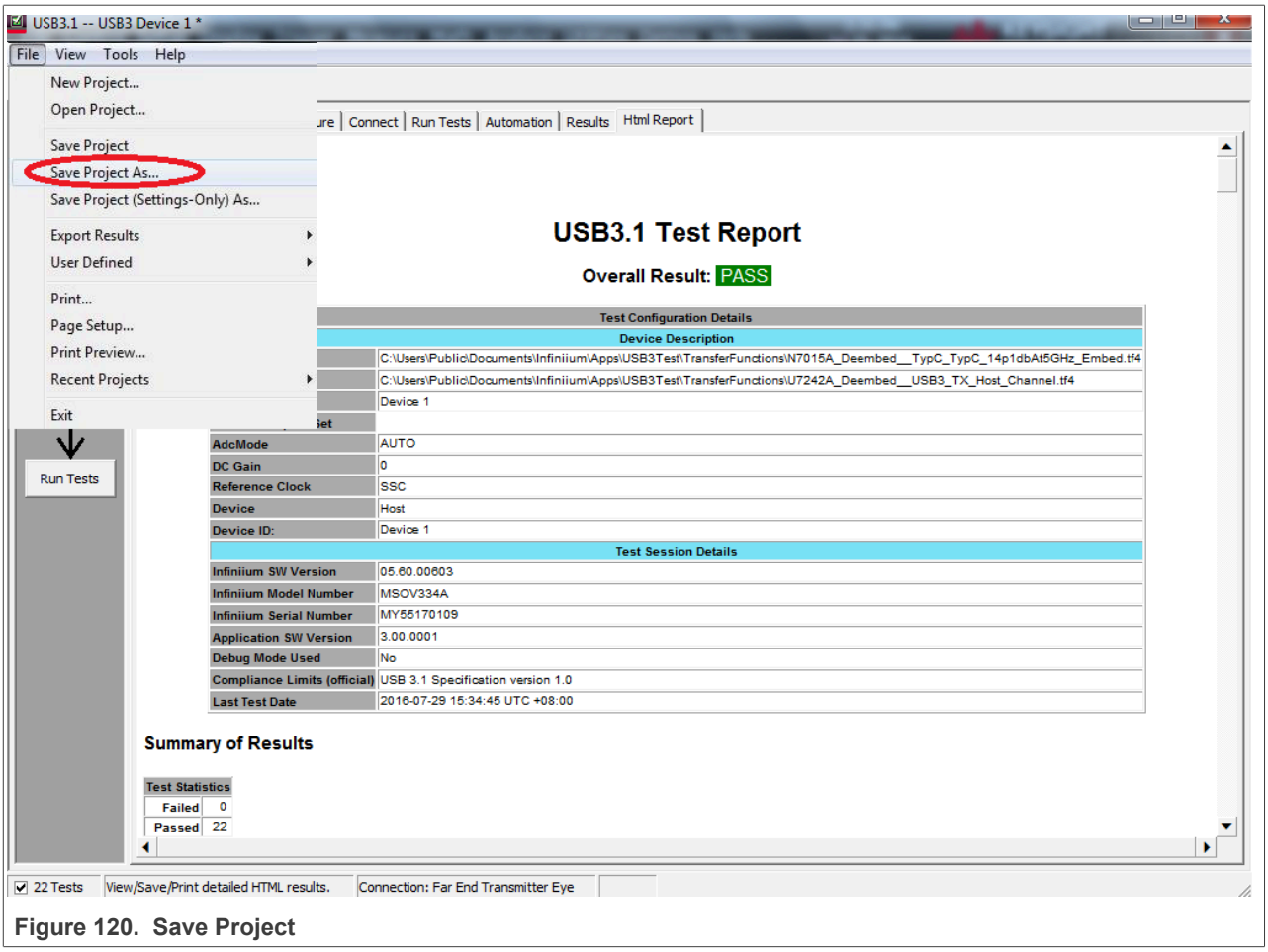

Figure 120. Save Project

3.5 USB3.0 super speed receiver compliance tests

TBD

4 Device framework test

4.1 Introduction of device framework test

When testing a USB device or hub, you should at least test USBCV (Command Verifier). It automatically tests the device framework and descriptor. All USB 2.0 peripherals seeking certification are required to demonstrate enumeration on the USB 3.0 PDK. So both USB20CV and USB30CV tests are required. These test tools are available on the USB.ORG, http://www.usb.org/developers/tools/. Read the installation guide carefully before you start testing.

For Hi-speed peripherals, the Chapter 9 tests must be executed twice – once in Full-speed mode, and once in Hi-speed mode. It is not necessary to run HID, Mass-Storage (MSC), Video Class (UVC) at both speeds.

Download the *Company List* and save as “usb.if” in the same directory where USBCV is installed. You can find the company ID from this list. Remember this list changes almost every day, be sure to get a fresh copy when you use the tools.

Test Items:

- USBCV Chapter 9
- USBCV Class Test
- USBCV Current Measurement Test

4.2 USBCV Chapter 9 test

The Chapter 9 tests cover the device support of the commands set in Chapter 9 of the USB specification.

To see the detailed description of test items, refer the documents ***#Universal Serial Bus Revision 2.0 USB Command Verifier Compliance Test Specification Revision 1.2*** *and* ***# Universal Serial Bus Revision 3.1 USB Command Verifier Compliance Test Specification Revision 0.7.***

Test Items:

- TD 9.1: Device Descriptor Test
- TD 9.2: Configuration Descriptor Test
- TD 9.3: Interface Association Descriptor Test
- TD 9.4: Interface Descriptor Test
- TD 9.5: Endpoint Descriptor Test
- TD 9.7: BOS Descriptor Test
- TD 9.9: Halt Endpoint Test
- TD 9.12: Remote Wake-up Test
- TD 9.13: Set Configuration Test
- TD 9.14: Suspend/Resume Test
- TD 9.16: Enumeration Test
- TD 9.17: Other Speed Configuration Descriptor Test
- TD 9.18: Device Qualifier Descriptor Test
- TD 9.21: LPM L 1 Suspend Resume Test

Test Instructions:

1. Install USB20CV on the Test Bed Computer with USB2.0 ports, and USB30CV on the Test Bed Computer with USB3.0 ports.
2. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the **gold-tree20** HS Hub.
3. Run USB20CV 21 on Computer, select **Chapter 9 Tests**, and then click **Run** button to launch the tests.
4. Select the DUT device in the list, click Ok as shown in Figure 121 below.
5. After Chapter 9 tests are finished, USB20CV will pop out a window shows which other tests must be done, as shown in Figure 122 below. i.MX series acts as Mass Storage in Device Mode, so if the pop-out box asks you to do tests more than MSC, you should check your configuration of supported Device Class.
6. Click **Launch Report Viewer** to view the test report. From the basic Chapter 9 Tests, you can get **VID, PID,** and other information of DUT, check that the VID should be your company **VID.** Remember **MSC** Serial number characters must be “0-9” or “A-F”, in ASCII 0x0030-0x0039 or 0x0041-0x0046. For self-powered devices, verify that the “Device is currently **SELF POWERED22**”, for bus-powered devices, verify that the “Device is currently **BUS POWERED**”.
7. Change the HS hub to a gold-tree FS Hub, then run the test again in Full-speed mode.
8. Run USB30CV on Computer, do the **Chapter 9 Tests** again, both in Hi-speed and Full-speed modes

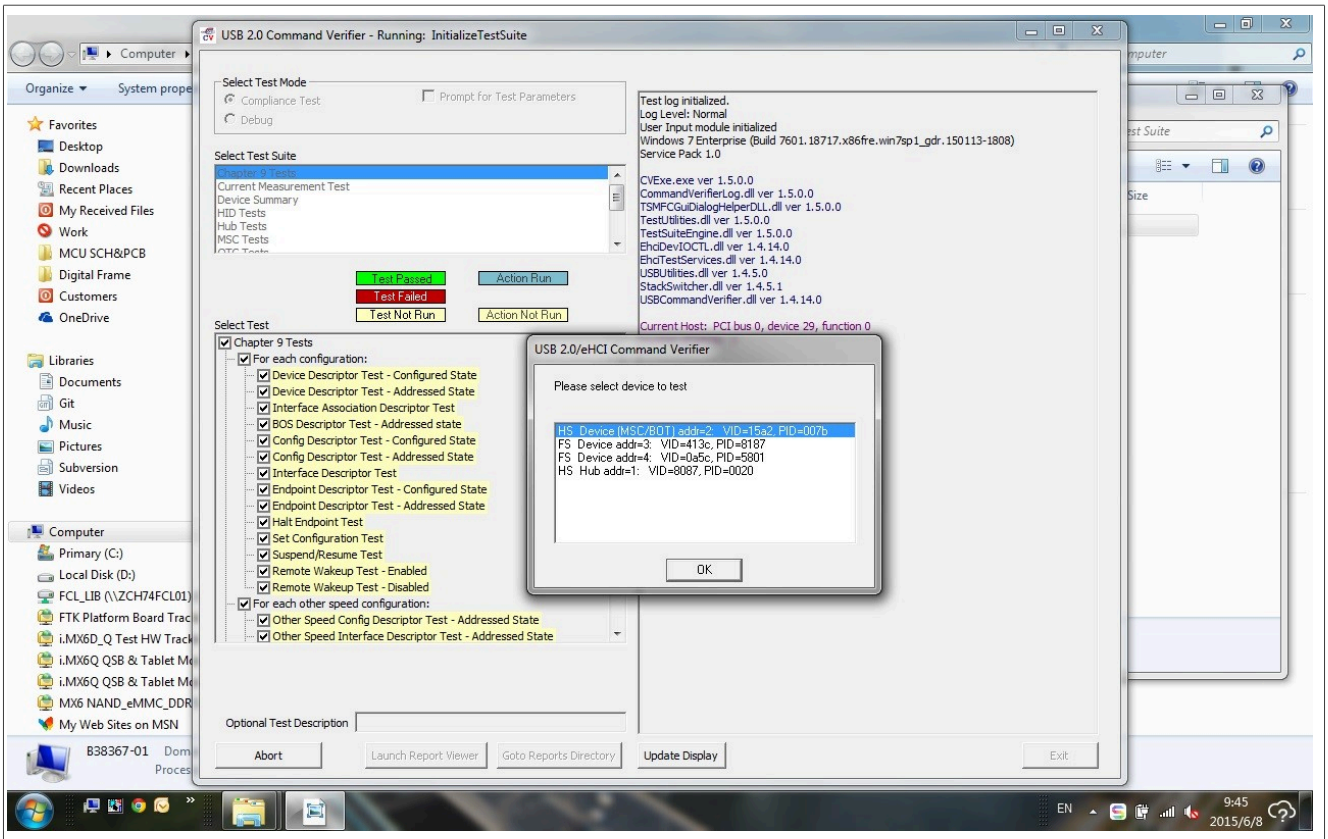

Figure 121. Select USB20CV Chapter 9 Tests

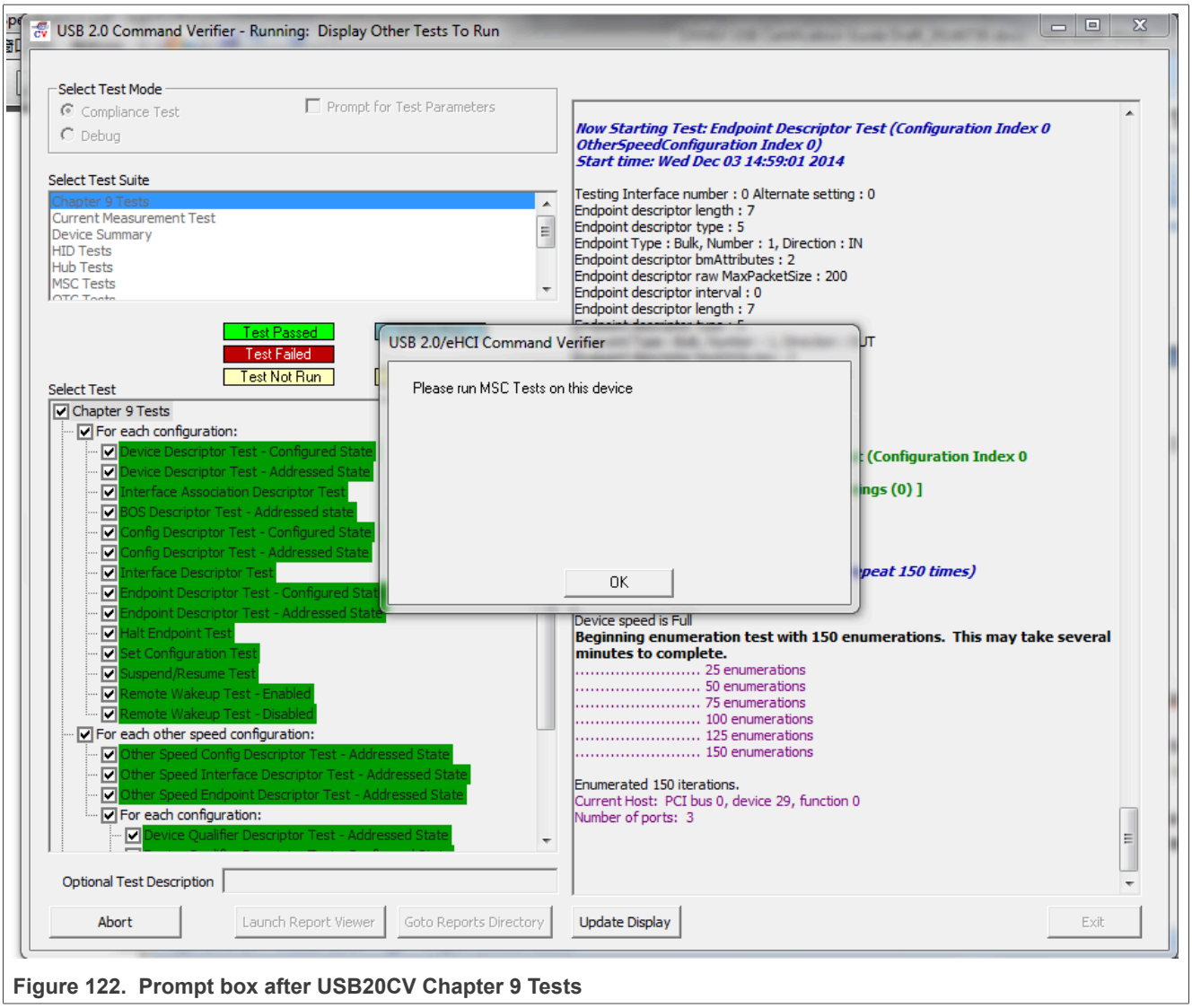

Figure 122. Prompt box after USB20CV Chapter 9 Tests

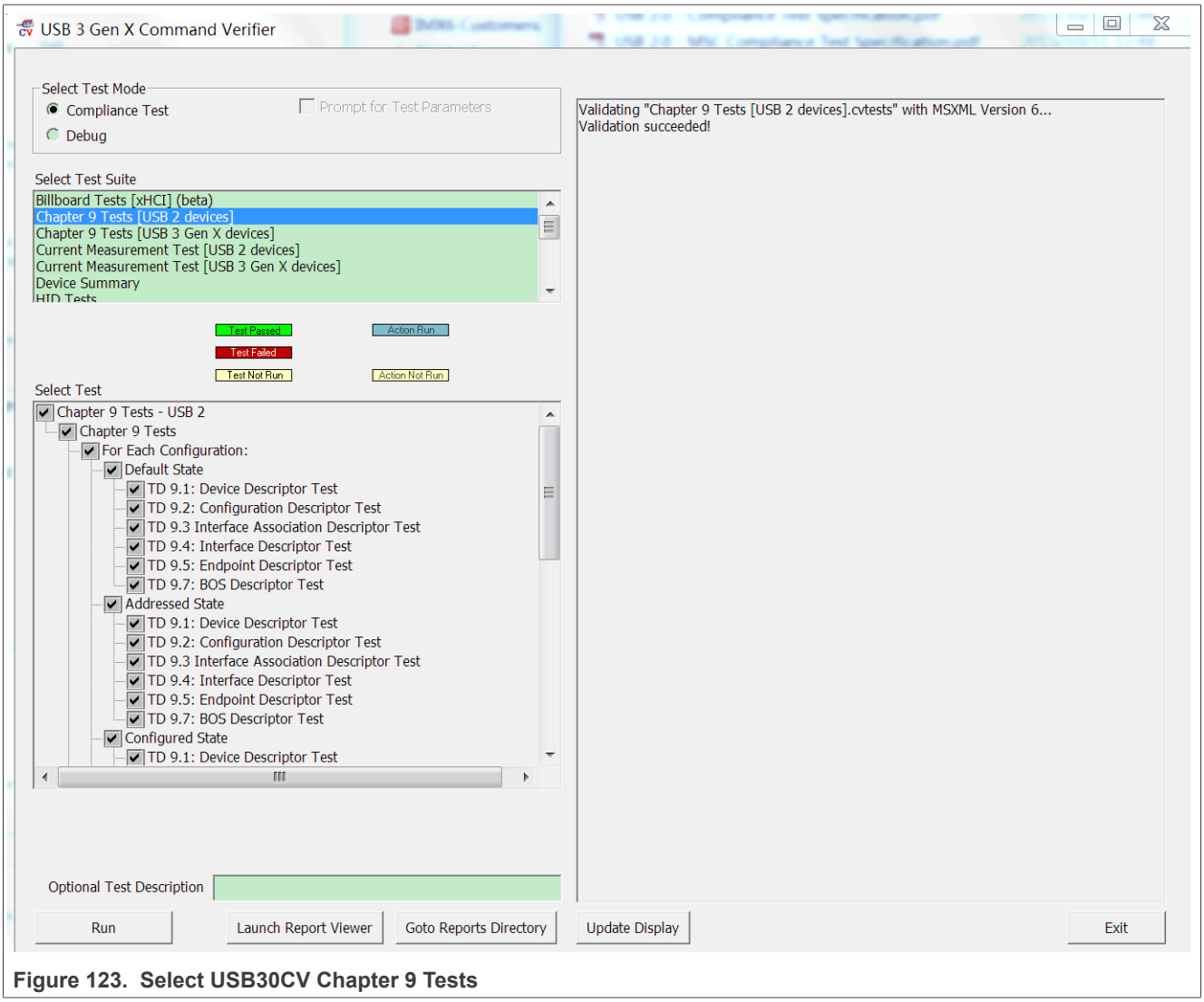

Figure 123. Select USB30CV Chapter 9 Tests

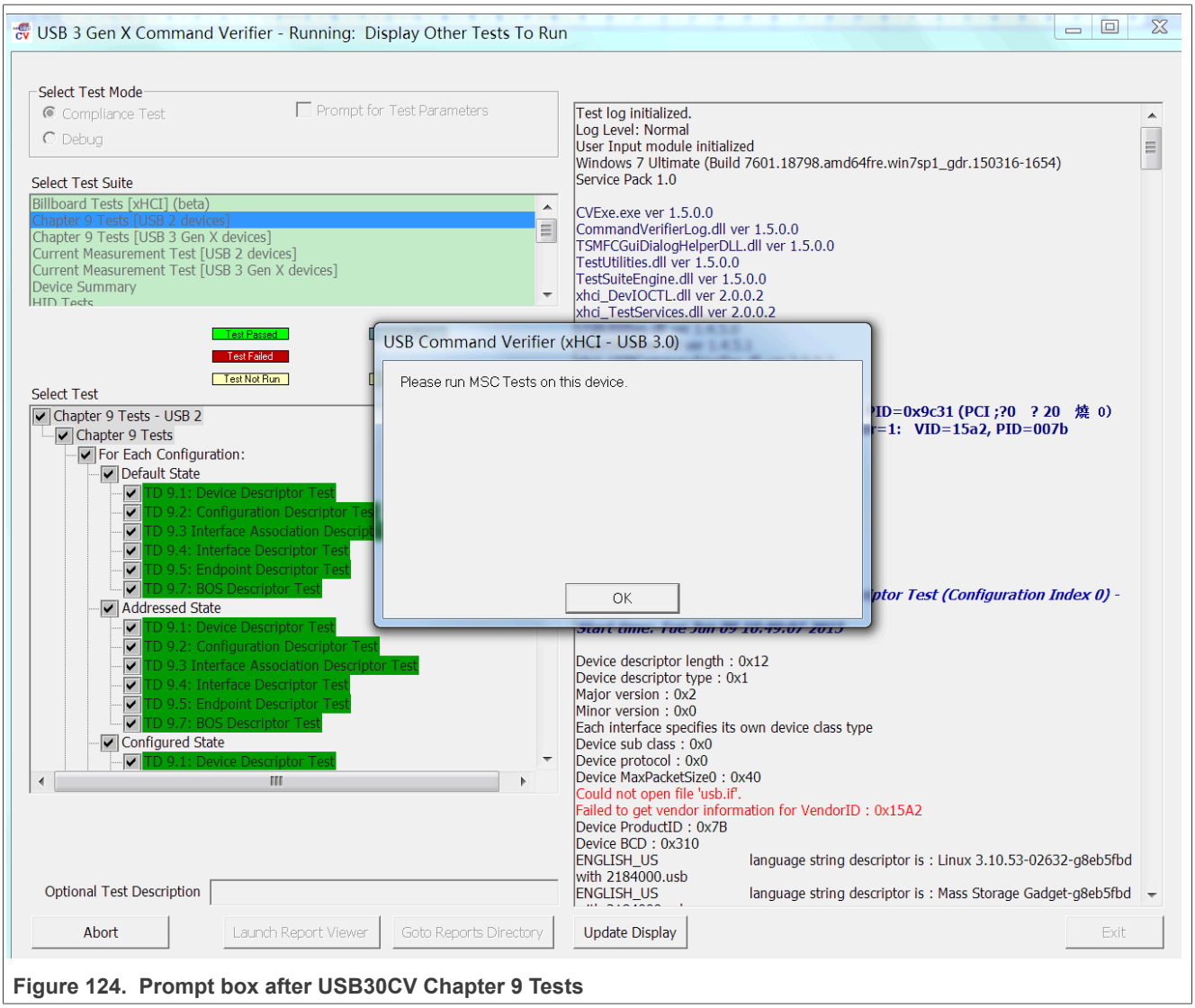

Figure 124. Prompt box after USB30CV Chapter 9 Tests

Note:

- *See gold-tree devices list in Chapter 4.*
- *When you run USBCV, it replaces the standard Microsoft EHCI host driver with its own test stack driver, so all standard peripherals on computer, such as mouse, U-disk are invalid at this moment.*
- *i.MX series acts as Self-Powered Device in device mode.*

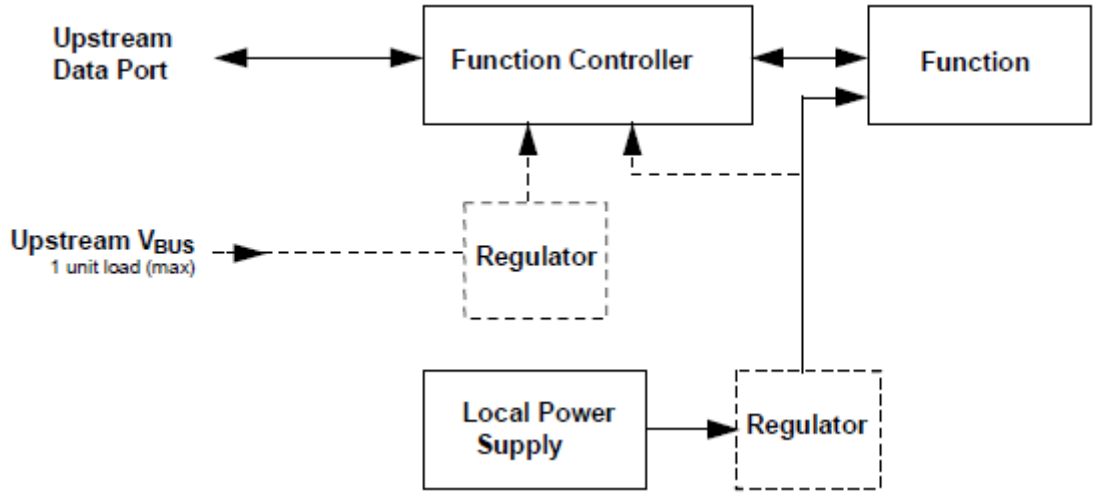

Figure 125. Self-Powered Function

4.3 USBCV class test

Appropriate class tests (HID, HUB, MSC, UVC, PHDC, and so on,…) should be done according to the prompt of Chapter 9 Tests, as shown in Figure 122 above.

To see the detailed description of test items, refer the documents ***#Universal Serial Bus Revision 2.0 USB Command Verifier Compliance Test Specification Revision 1.2*** *and* ***# Universal Serial Bus Mass Storage Class Compliance Test Specification Revision 1.1.***

Note: *i.MX series is enumerated as Mass Storage in device mode, so only must implement MSC Test.*

4.3.1 MSC test

It is intended that all devices which report a Mass Storage Class interface is required to pass this test in order to receive logo certification. The tests described herein shall be run on all interfaces that report themselves as MSC.

Test Items:

- TD 1.1: Interface Descriptor Test
- TD 1.2: Serial Number Test
- TD 1.3: Class-Specific Request Test
- TD 1.3: Error Recovery Test
- TD 1.5: Case 1 Test
- TD 1.6: Case 2 Test
- TD 1.7: Case 3 Test
- TD 1.8: Case 4 Test
- TD 1.9: Case 5 Test
- TD 1.10: Case 6 Test
- TD 1.11: Case 7 Test
- TD 1.12: Case 8 Test
- TD 1.13: Case 9 Test
- TD 1.14: Case 10 Test

- TD 1.15: Case 11 Test
- TD 1.16: Case 12 Test
- TD 1.17: Case 13 Test
- TD 1.18: Power-Up Test
- TD 1.19: CB Length Test
- TD 1.19: CB Length Test
- TD 2.1: Required Commands Test
- TD 2.2: Optional Commands Test

Test Instructions:

1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
2. Run USB20CV on Computer, select **MSC Tests,** and then click **Run** button to launch the tests.
3. Select the DUT device in the list, click Ok as shown in Figure 126 below.
4. During the test, a pop-out dialog asks you to disconnect and power off DUT, and then repower it, as shown in Figure 127 below.
5. After the test is done, click **Launch Report Viewer** to view the test report.
6. Change the HS hub to a gold-tree FS Hub, then run the test again in Full-speed mode
7. Run USB30CV on Computer, do the **MSC Tests** again.

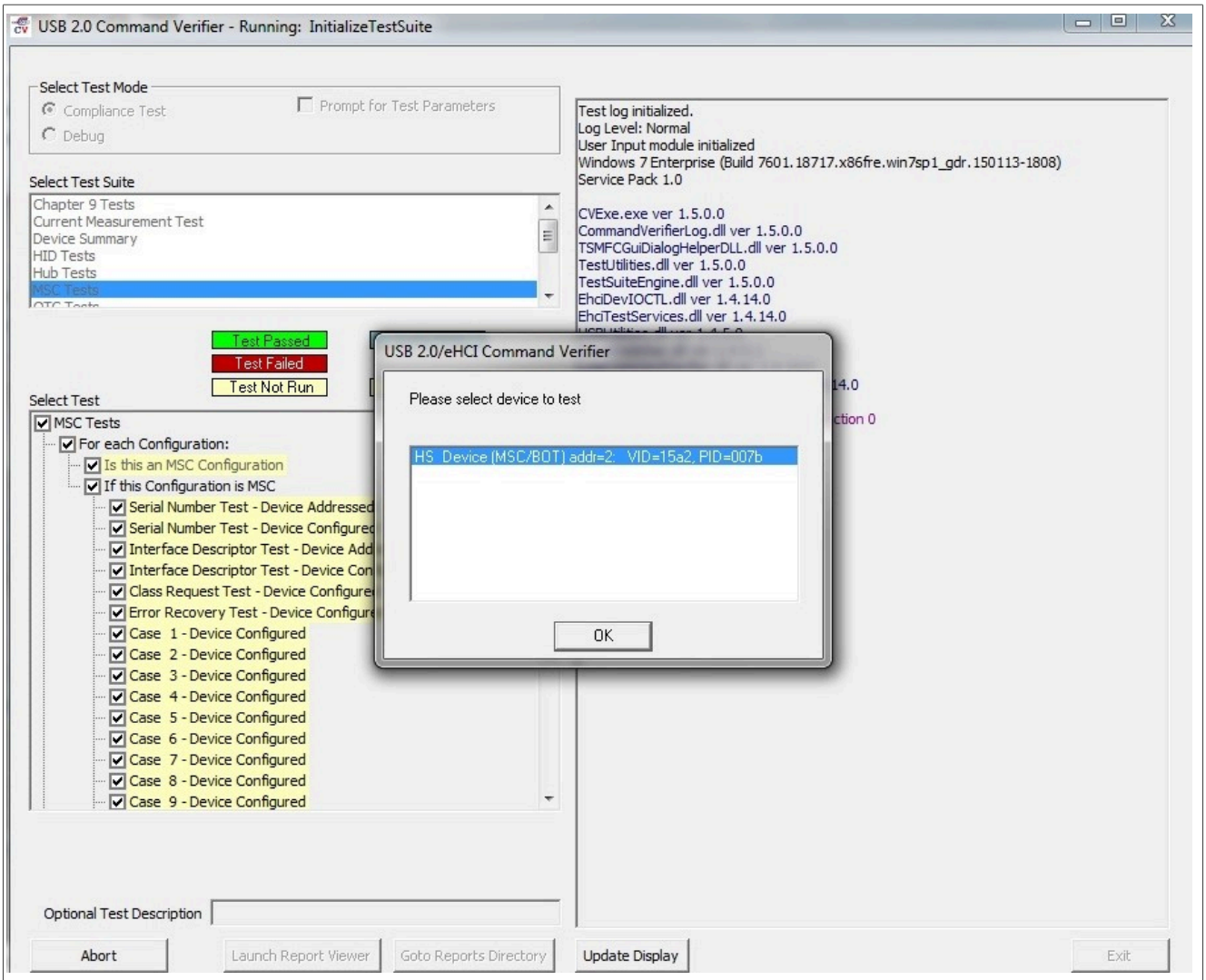

Figure 126. USB20CV MSC Tests

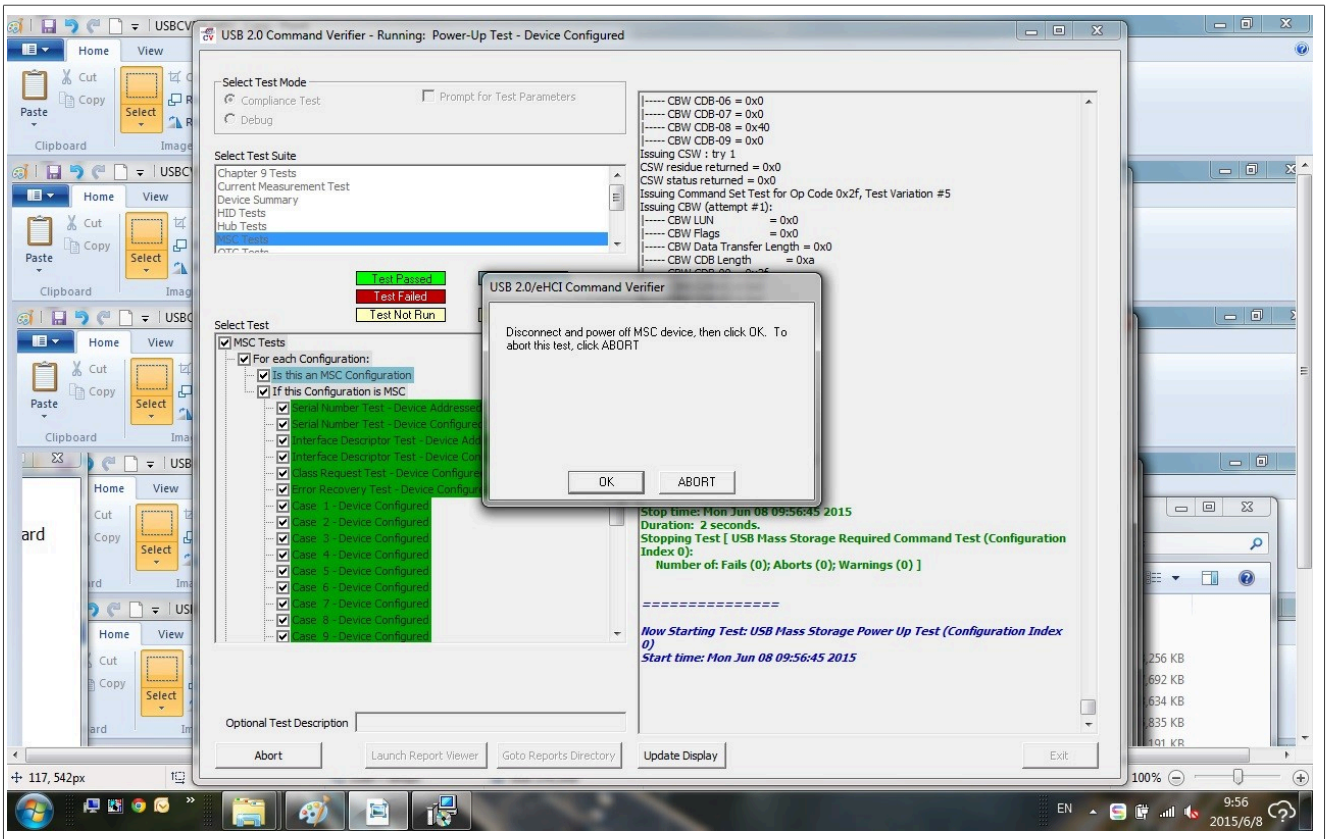

Figure 127. USBCV MSC Tests_Repower Device

Note: *Not necessary to run these tests at both High Speed and Full Speed once, basing on the explanation in USB-IF Compliance Updates.*

4.3.2 HID test

It is intended that all devices which report a Human Interface Device interface is required to pass this test in order to receive logo certification. The tests described herein shall be run on all interfaces that report themselves as HID.

Test Items:

- HID Descriptor Test
- HID Get/Set Idle Test
- HID Get/Set Protocol Test
- HID Report Descriptor Test

HID Specification Version Test **Test Items:**

- HID Descriptor Test
- HID Get/Set Idle Test
- HID Get/Set Protocol Test
- HID Report Descriptor Test
- HID Specification Version Test

Test Instructions:

1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
2. Run USB20CV on Computer, select **HID Tests,** and then click **Run** button to launch the tests.
3. Select the DUT device in the list, click Ok as shown in Fig4-8 below.
4. After the test is done, click **Launch Report Viewer** to view the test report.
5. Change the HS hub to a gold-tree FS Hub, then run the test again in Full-speed mode 25.
6. Run USB30CV on Computer, do the **HID Tests** again.

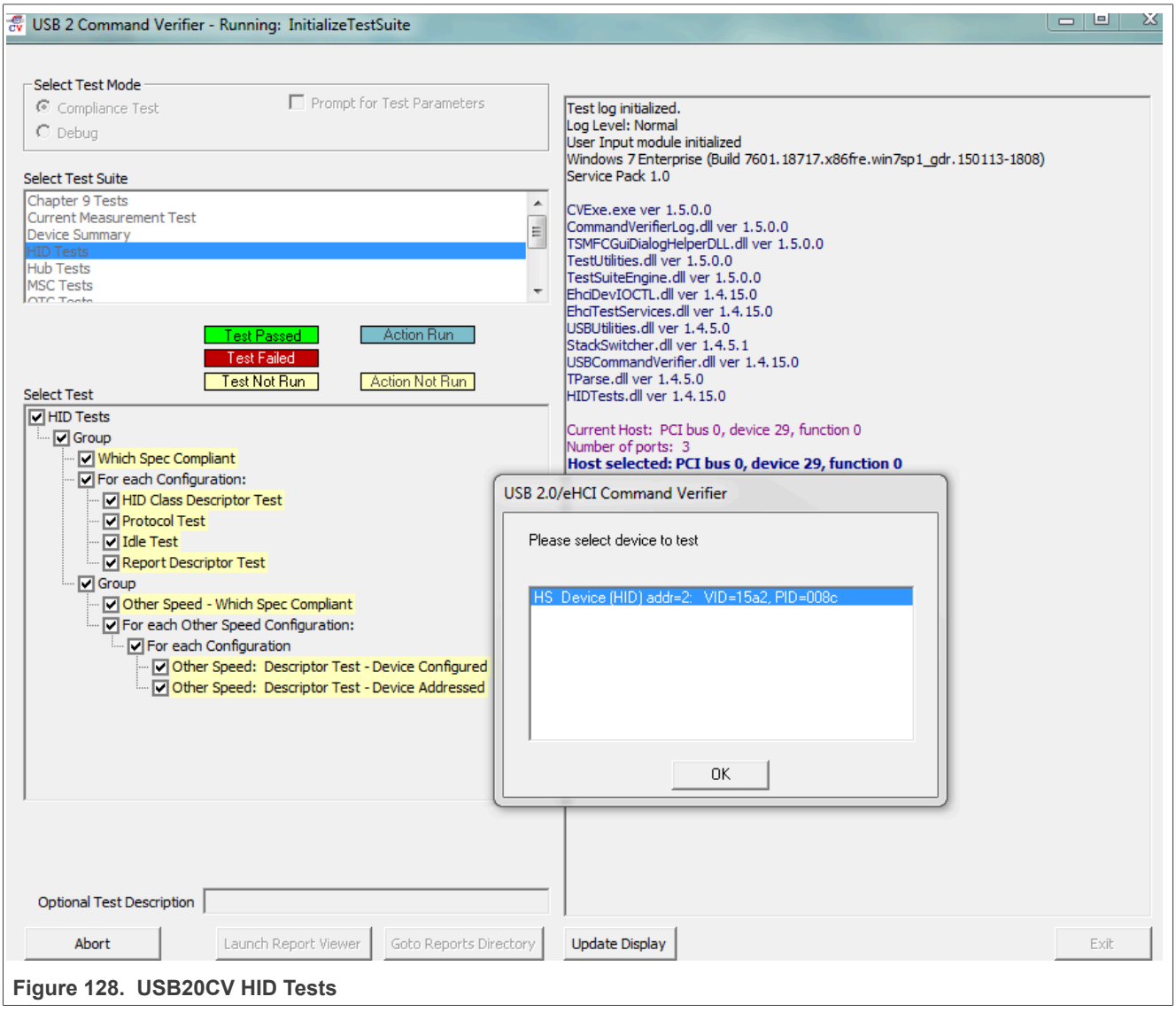

Figure 128. USB20CV HID Tests

Note: *Not necessary to run these tests at both High Speed and Full Speed once, basing on the explanation in USB-IF Compliance Updates.*

4.4 USBCV current measurement test

In order to measure the power distribution of a USB device, the average current is measured during **unconfigured**, **configured**, **active,** and **suspend** state with a digital multimeter and fixture to measure the

VBUS current. The circumstances for measuring the average current are dependent on the speed of the device and the power mode the device is in (for example, self-powered, bus-powered).

For a Hi-Speed device, the average current is measured in Hi- Speed and Full-Speed mode. All Hi-Speed measurements are performed by connecting the DUT after one self-powered Hi-Speed hub. A Full-Speed self-powered hub is connected to the first Hi-Speed hub in order to force a Hi-Speed DUT to enter its Full-Speed mode.

A device must also be measured using the supported power mode in the following circumstances:

1. When a device is only capable of operating in self-powered mode, all measurements are performed in self-powered mode. It means that the device is unable to enumerate without being connected to an external power.
2. When a device is capable in operating in bus-powered mode, all measurements are performed in bus-powered mode even when the device claims to be self-powered (in its device descriptor).
3. When a device has battery-charging capabilities over USB, the power measurements are performed in worst case scenario, most probably it is when the product has a dead battery.

Test Items:

- Unconfigured Current
- Configured Current
- Active Current
- Suspend Current

Test Requirements:

Table 18. USBCV Current requirements

Device State	Measurement Current	Requirement	Device Feature
Unconfigured	**0.17 mA**	**<=100 mA**	**All peripheral devices**
Configured		<=bMaxPower 26 <=100 mA	Low-power Bus-powered Device
	0.17 mA	**<=bMaxPower<=100 mA**	Self-powered Device
		<=bMaxPower<=500 mA	High-power Bus-powered Device
Active		<=100 mA	Low-power Bus-powered Device
		<=500 mA	High-power Bus-powered Device
	0.17 mA	**<=100 mA**	**Self-powered Device**
Suspend		<0.5 mA	Remote Wake-up Unsupported Device
	0.17 mA	**<2.5 mA**	**Remote Wake-up Supported Device**
Powered' State Suspend	**0.17 mA**	**<2.5 mA**	**Battery Charging Not supported Device**
		<100 mA	Battery Charging supported Device

Note:

- *bMaxPower is defined as the maximum power consumption of the USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units.*
- *i.MX series acts as a Self-powered device in Device Mode.*

4.4.1 Unconfigured/Configured current test

The USB 2.0 DUT is set in unconfigured/configured state by using the tool USB20CV. For a USB 3.0 device, the unconfigured/configured state can be forced by using USB30CV.

Test Instructions:

1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, as shown in Figure 129 below, be sure to use the gold-tree HS Hub.

2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
3. Run USB20CV on Computer, select **Current Measurement Test,** and then click **Run** button to launch the tests.
4. Select the DUT in the list, click OK.
5. A pop-out dialog asks you to measure the **Unconfigured Current,** as shown in the figure below. After recording the maximum current value, click OK.
6. Another pop-out dialog asks you to measure the **Configured Current,** as shown in the figure below.
7. Record the maximum current value, then click OK to finish the test.

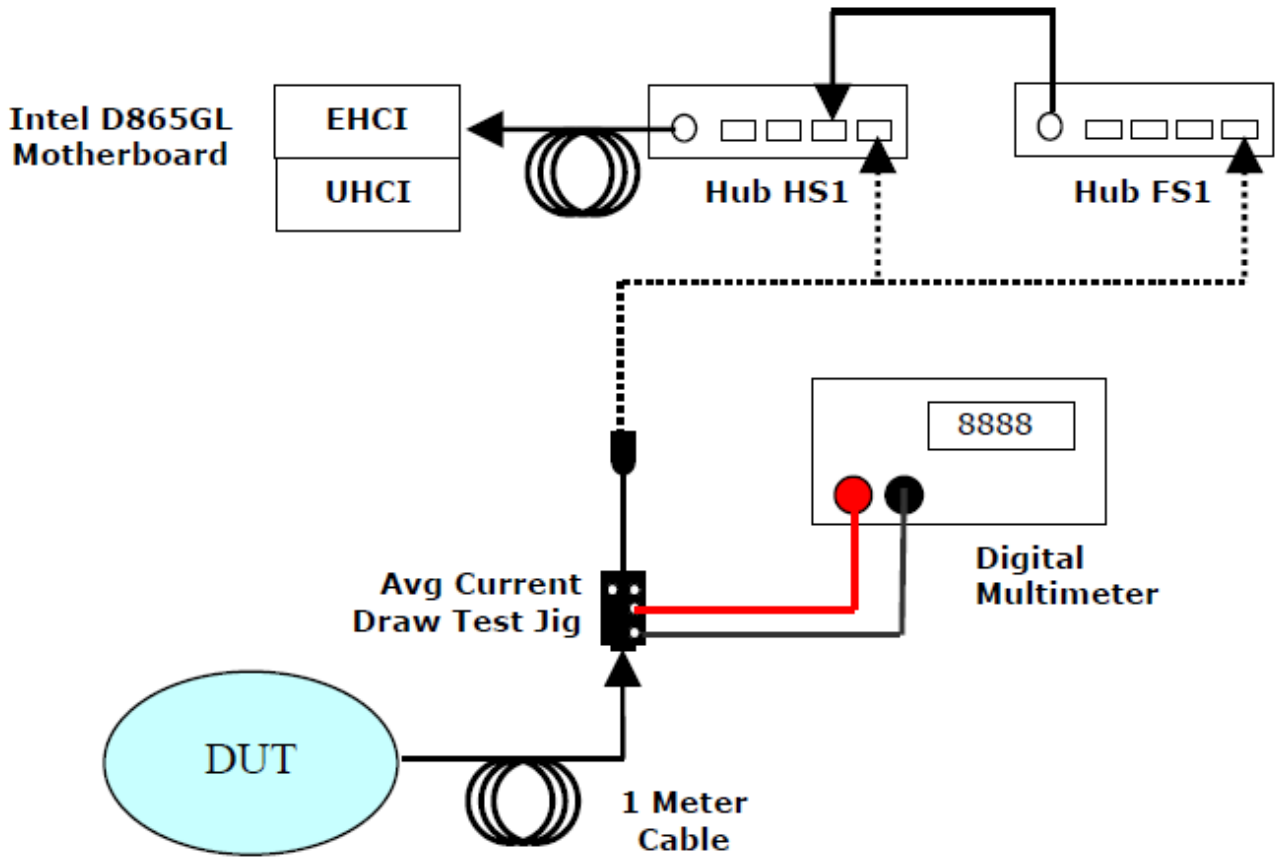

Figure 129. Current Measurement Environment

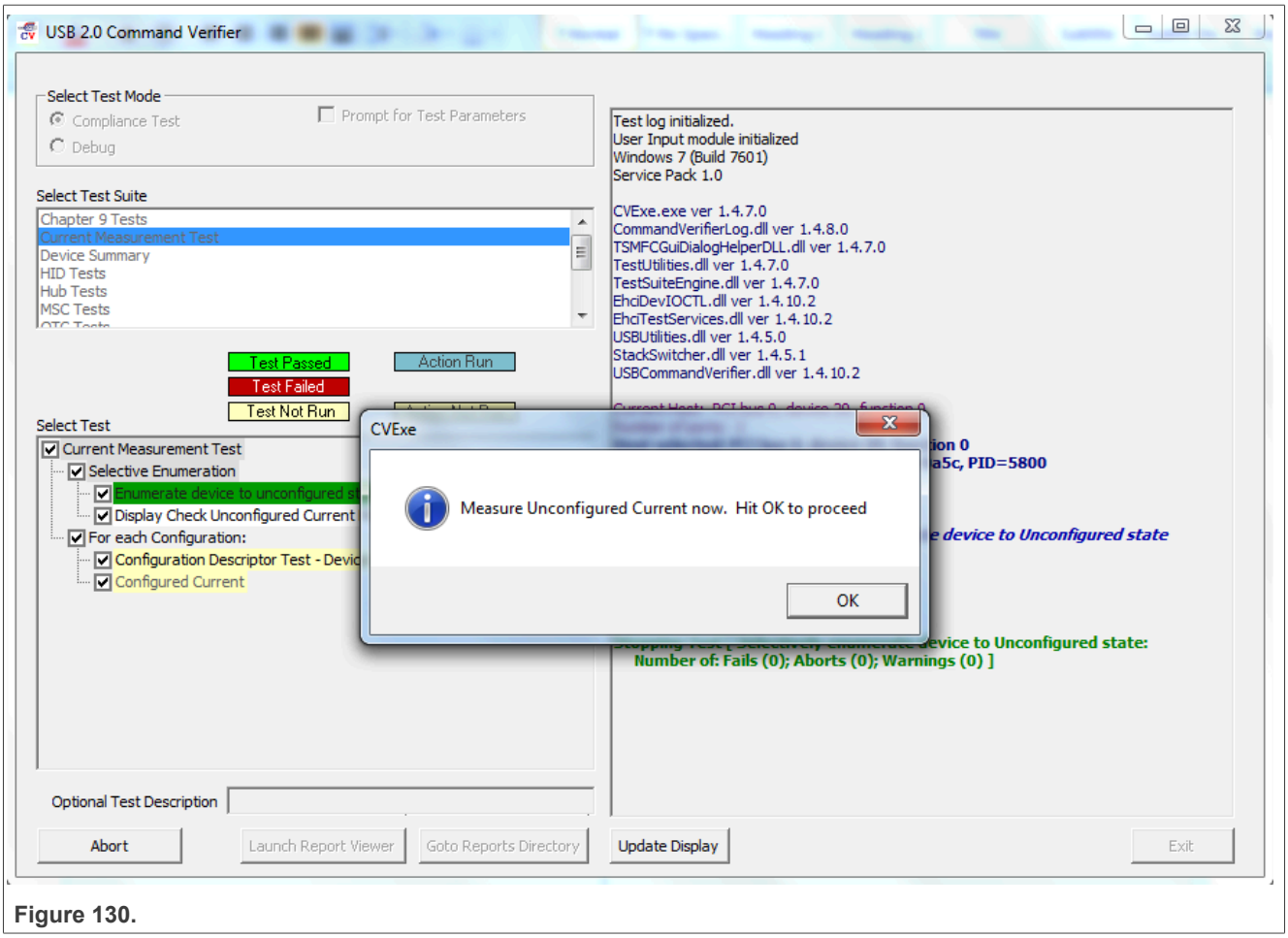

Figure 130.

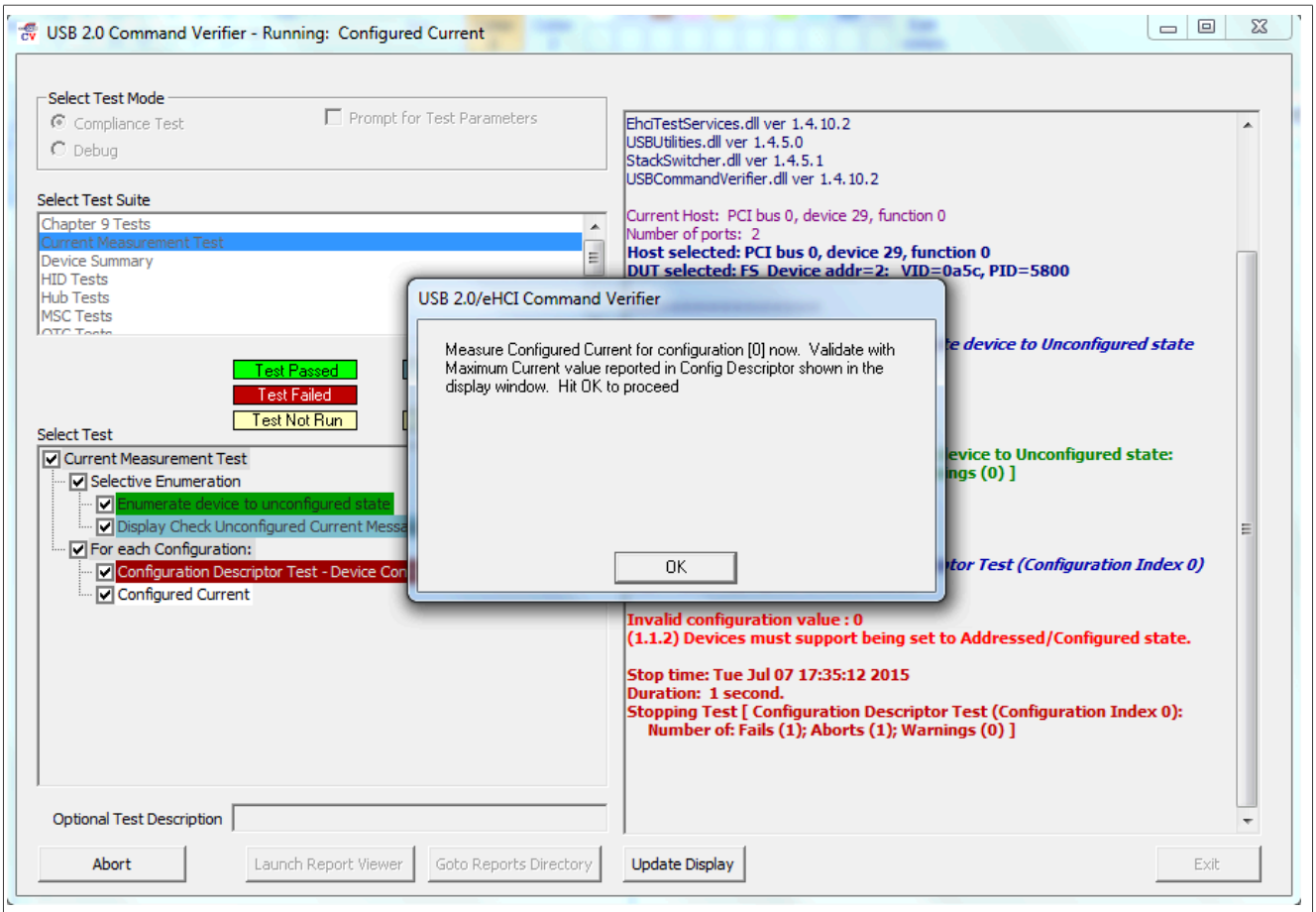

Figure 131. USB20CV Configured Current Measurement Test

4.4.2 Active current test

The USB 2.0 DUT is operating correctly and during operation, the device current is measured in worst-case power consumption mode. The active current must remain below the value defined in the bMaxPower field of the descriptor.

Test Instructions:

1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
3. Operation the DUT, for example: Copy a file from computer to DUT which is enumerated as MSC Device, after the copy is finished, recopy the file to computer, in the meantime, copy another file from computer to DUT.
4. Record the maximum current value during the bi-direction copying period.

4.4.3 Suspend current test

The USB 2.0 DUT is suspended after it is correctly enumerated by the host system. If the device supports remote wake-up, this feature must be enabled during measurement.

Test Instructions:

1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
3. After DUT is enumerated as MSC device, enter following command in Linux console to force DUT into suspend mode.
   echo mem > /sys/power/state
4. Record the maximum current value.

4.4.4 Suspend current powered state

Peripherals are required to support the suspend state whenever VBUS is powered, even if bus reset has not occurred.

This measurement is not the regular suspend current measurement as described above. Do not forget it!

Test Instructions:

1. Connect the downstream port of an HS hub to DUT, and the upstream port to the Test Bed Computer, be sure to use the gold-tree HS Hub.
2. Insert a Multimeter in series of the VBUS line, make sure that the connection is for current test, and the switch is in right range.
3. Run USB20CV on Computer, select **Current Measurement Test,** and then click **Run** button to launch the tests.
4. Select the DUT in the list, click OK.
5. After the unconfigured and configured states are ended, do not switch off USBCV, deattach, and reattach the device and then measure the current.
6. Record the maximum current value, then click OK to finish the test.

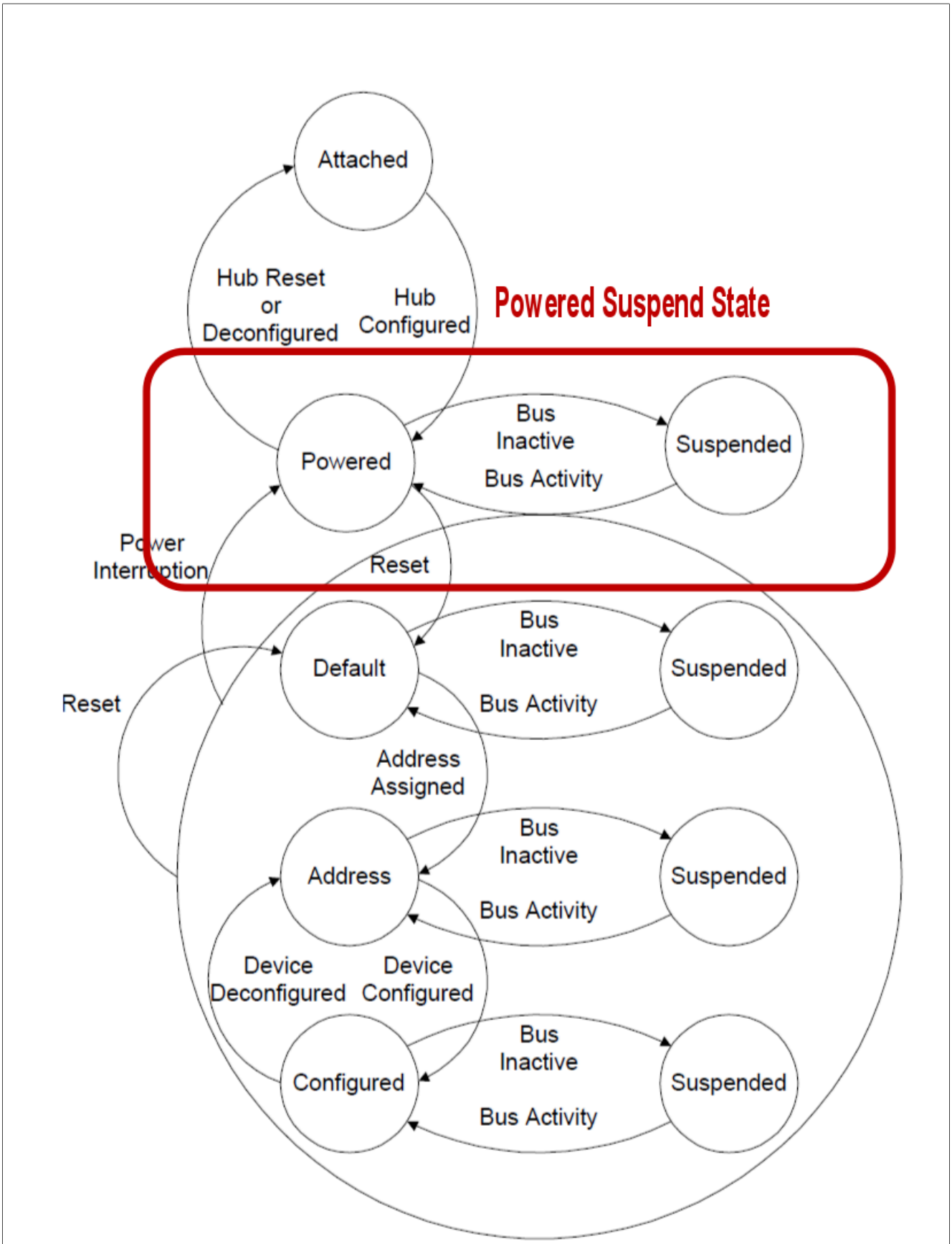

Figure 132. Powered Suspend State

5 Interoperability tests

5.1 Device interoperability test

Device Interoperability test evaluates the device's ability to interoperate with the host system and coexist with other USB devices. It also provides some insight into usability issues of the device and associated software. See the detailed description of Embedded Host Interoperability Test, you can refer "**Interoperability**"part of "***Gold Suite Summary Test Procedure V1.35 Draft***".

Interoperability makes use of an arrangement of USB peripherals known as the "Gold Tree". The Gold Tree consists of these characteristics:

- Provides isochronous, bulk, interrupt, and control traffic
- Tests the device behind 5 levels of nested hubs – the maximum allowed
- Tests the device up to 30 meters from the host – the maximum allowed
- Contains a high-speed branch and full-speed speed branch
- EHCI, UHCI, and OHCI controllers available for testing

The Gold Tree is supposed to consist of USB-IF certified consumer devices that are widely available in the market. Unfortunately, the shelf-life of consumer products is limited and some items become difficult to find as time goes by. So if a specific gold tree device cannot be obtained, it may be substituted with a similar, certified device.

Table 19. Gold Tree Device List

Item	Class	Description	Example Product	Qty
USB Host System		Multicore processor Certified USB EHCI with integrated UHCI Certified USB xHCI	DELL XPS8700 (example)	1
EHCI / OHCI		PCI Host Adapter using certified USB EHCI with integrated OHCI	Adaptec, model AUA 4000 PCI adapter	1
xHCI (SuperSpeed host adapter)		PCI Host Adapter using certified USB xHCI	USB-IF SuperSpeed PDK	1
HS Hub (Self-powered)	Hub	Hi-speed hub. Minimum of 4 exposed downstream ports	Belkin F5U233	6
FS Hub (bus-powered)	Hub	Full-speed hub. Minimum of 2 exposed downstream ports (Likely to be a compound device)	Targus Numeric Keypad with 2-port Hub, model PAUK10U	1
USB mouse	HID	Low-speed using interrupt transport	Microsoft Basic Optical Mouse	1
HS Mass Storage	MSC	Hi-speed using bulk transport	Memorex TravelDrive model 3 2509051	2
PC Camera	UVC	Hi-speed using isochronous transport	Logitech QuickCam Ultra Vision P/N: 961471-0403	1
average current draw test jig		Fixture to measure current consumed from VBus	http://www.usb.org/developers/adapters/	1
one meter (or shorter) USB cable		any listed on USB-IF Cables and Connectors Integrators List		1
4.5 meter USB cable with mini B-plug		any listed on USB-IF Cables and Connectors Integrators List		1

Table 19. Gold Tree Device List*...continued*

Item	Class	Description	Example Product	Qty
2 meter USB cable with micro USB B-plug		any listed on USB-IF Cables and Connectors Integrators List		1
five meter USB cables		any listed on USB-IF Cables and Connectors Integrators List		8

Test Items:

- Enumeration and driver installation
- Operation with default drivers
- Interoperability
- Hot Detach and Reattach
- Warm boot
- Remote wake-up Test 28
- S3 Active Suspend Test
- S3 Active Suspend Resume Test
- Root Port Test
- S4 Active Hibernate Test
- S4 Active Hibernate Resume Test
- Topology change UHCI 2 9
- Topology change OHCI 29
- Topology change XHCI

Test Report:

Table 20. Device Interoperability Test Report

Num	Test Item	Result
1	Enumeration and driver installation	Pass
2	Operation with default drivers	Pass
3	Interoperability	Pass
4	Hot Detach and Reattach	Pass
5	Warm boot	Pass
6	Remote wake-up Test	***N/A***
7	S3 Active Suspend Test	Pass
8	S3 Active Suspend Resume Test	Pass
9	Root Port Test	Pass
10	S4 Active Hibernate Test	Pass
11	S4 Active Hibernate Resume Test	Pass
12	Topology change UHCI	Pass
13	Topology change OHCI	Pass
14	Topology change XHCI	Pass

Note:

- *If the DUT supports Remote Wake-up, enable it to wake the system. If not, this test could be dismissed. i.MX is enumerated as MSC Device, so it does not support Remote Wake-up.*
- *Interoperability test on OHCI or UHCI is informational only and not required for the purposes of certification.*

5.1.1 Enumeration and driver installation

Test Instructions:

1. Construct a tree of USB devices as shown in **Fig5-1 below**. Attach Hub HS1 to a root port on the **EHCI** motherboard. Attach the gold tree, via Hub HS2, to Hub HS1.
2. Plug in the DUT into the open port on the multi-TT Hub HS5.
   - Do NOT install any drivers or software prior to attaching the device
   - Use a 5 meter cable if the device does not have a captive cable
3. If OS does not possess a native driver, follow OS instructions to install the driver. If driver still does not load – install software as directed by vendor.
   - If driver loads, PASS with waiver and recommend the driver load via .INF file
   - If reboot is requested or required as a result of driver (or application) installation – PASS with waiver and recommend removing reboot requirement
4. Check if DUT and other devices are enumerated.
5. **Pass** is considered when all following items meet:
   - DUT enumerates behind HS5 using a 5 meter cable or its own captive cable.
   - Driver installs with an *.INF* file (provided on a floppy or a CD) or is enumerated automatically by the system (class driver).
   - DUT does not require a reboot
   - DUT is correctly identified by Device Manager and no yellow exclamation point is shown for any device.
6. **Fail** is considered when any of the following items meets:
   - DUT cannot be installed because it requires driver installation or application software before DUT is ever plugged in.
   - DUT does not enumerate below hub #5.
   - Driver blue screens during enumeration.
   - DUT requires reboot.
   - DUT is incorrectly identified by Device Manager or a device is flagged as not operational (yellow exclamation point).

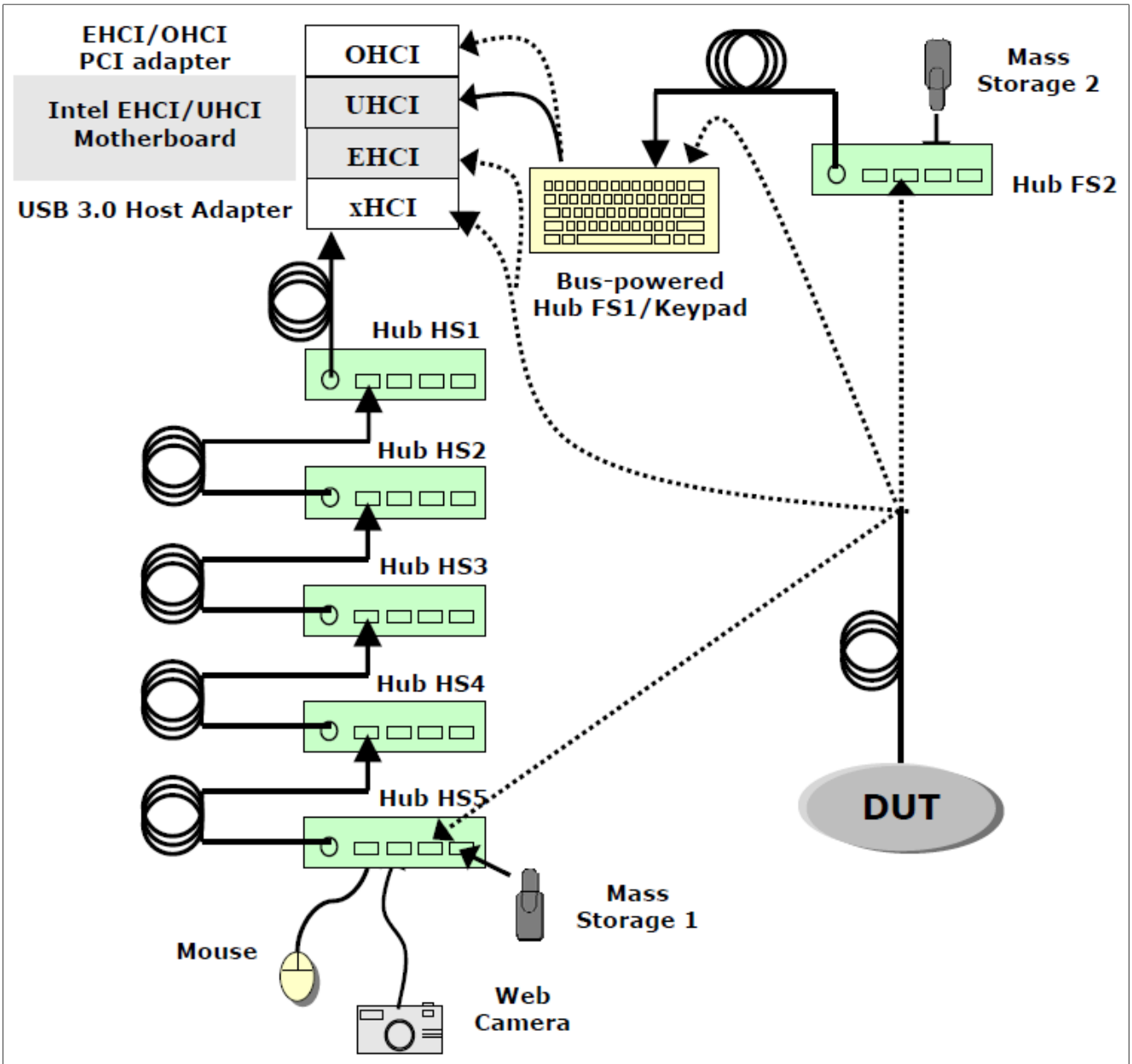

Figure 133. Interoperability Test Environment

5.1.2 Operation with default drivers

Test Instructions:

1. DUT demonstrates correct operation using default driver connected to Hub #5 with the 5 meter cable (if cable not captive).
2. Check if DUT and other devices are enumerated.
3. **Pass** is considered when all following items meet:
   - DUT operates as expected with the 5 meter cable (if cable not captive).
4. **Fail** is considered when any of the following items meets:
   - DUT cannot be installed because it requires driver installation or application software before DUT is ever plugged in.

- DUT fails to operate.
- Device/ Application blue screens or crashes system.
- Device fails to operate as expected below Hub #5.

5.1.3 Interoperability

Test Instructions:

1. Operate all the devices in Gold Tree. Verify that the DUT functions correctly while all other devices are operating concurrently.
   - Operate the device under test
   - View live video from the Veo camera
   - Transfer a large file between the Maxtor drive and the JumpDrive Pro
   - Strike keys on the Logitech keyboard
   - Disconnect and reconnect the Logitech mouse in the same port on Hub FS3
   - Move the Logitech Mouse verifying it still works
2. **Pass** is considered when all following items meet:
   - DUT operates as expected.
   - Gold Tree all devices operate well.
3. **Fail** is considered when any of the following items meets:
   - DUT fails to operate as expected.
   - One or more Gold Tree devices fail to operate.

5.1.4 Hot Detach and Reattach

Test Instructions:

1. Stop DUT operation!
2. Detach and reattach DUT to same hub port.
3. Test functionality of DUT only.
4. **Pass** is considered when all following items meet:
   - DUT operates as expected.
5. **Fail** is considered when any of the following items meets:
   - DUT fails to operate as expected.

5.1.5 Warm boot

Test Instructions:

- Stop operation of all devices!
- Restart the computer.
- Check operation of all USB devices including DUT.
- **Pass** is considered when all following items meet:
  - DUT operates as expected.
- **Fail** is considered when any of the following items meets:
  - Device fails to operate as expected.
  - One or more Gold Tree devices fail to operate.

5.1.6 Remote wake-up test

Test Instructions:

1. If the [DUT] supports remote wake-up, enable the DUT to wake the system (Computer->Manage->Device Manager->DUT->Power Management); otherwise, go to S3 Active Suspend Tests.
2. While device under test is actively operating, suspend the system. (Start->Shutdown->Sleep, wait 5 – 10 seconds after monitor is dark)
3. If the system does not go into suspend, then a message must appear saying that the active DUT will not allow suspend to occur.
4. Use DUT to wake the system, check operation of all USB devices including DUT.
5. **Pass** is considered when all following items meet:
   - System suspends and wakes up well.
   - All devices including DUT operate as expected.
6. **Fail** is considered when any of the following items meets:
   - System blue screens or locks up.
   - System can't suspend and wake up.
   - DUT fails to operate as expected.
   - One or more Gold Tree devices fail to operate.

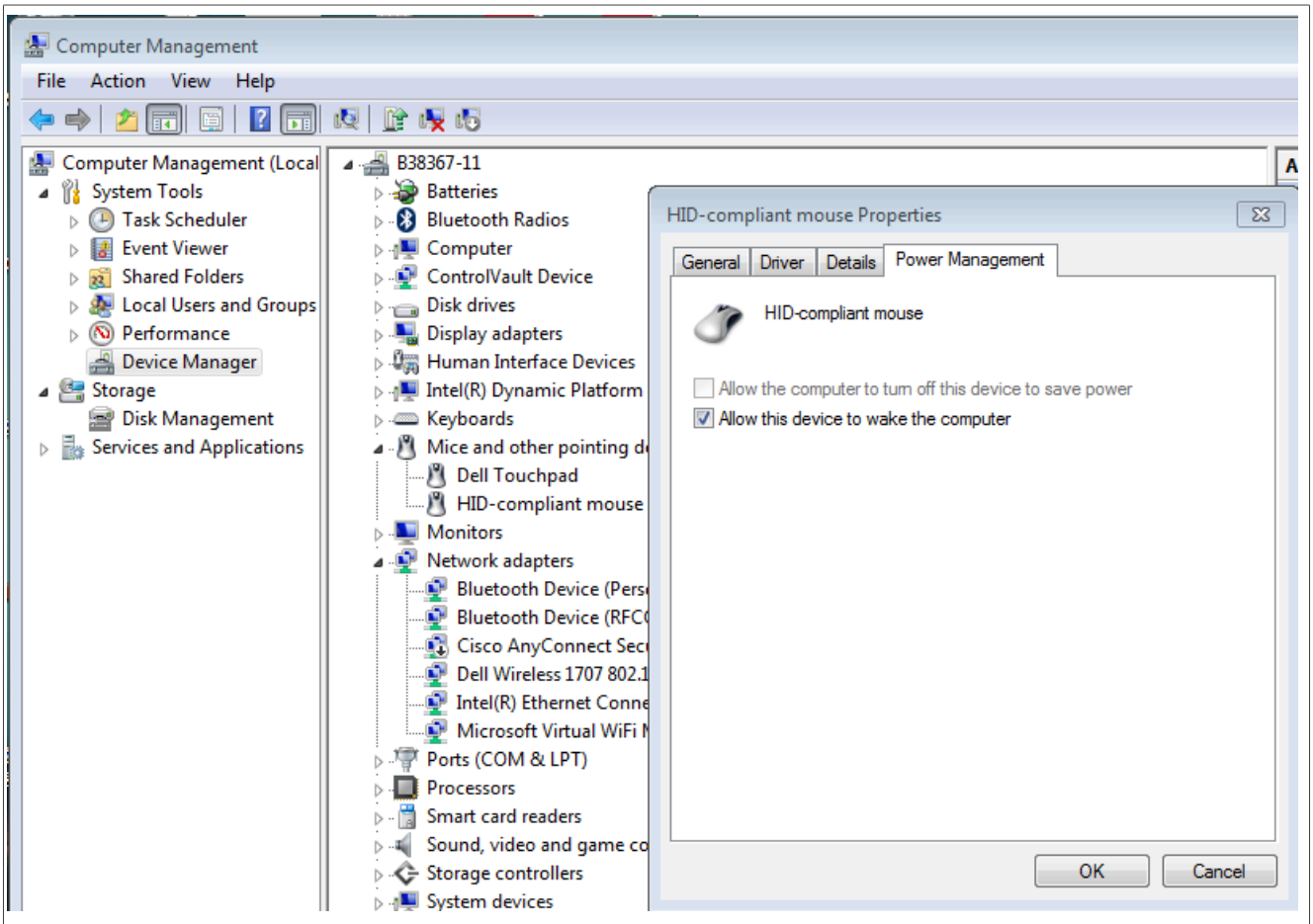

Figure 134. Enable Device to wake up the Computer

5.1.7 S3 active suspend test

Test Instructions:

1. Disable remote wake-up on all USB devices, including DUT.

2. Operate the DUT while placing the system in suspend. (Start->Shutdown->Sleep, wait 5 – 10 seconds after monitor is dark)
3. If the system does not go into suspend, then a message must appear saying that the active DUT will not allow suspend to occur.
4. **Pass** is considered when all following items meet:
   - System suspends well.
   - System notifies user that it can't go into suspend.
5. **Fail** is considered when either of the following items meets:
   - System does not enter suspend without notification.
   - System blue screens or locks up.

5.1.8 S3 active suspend resume test

Test Instructions:

1. Place the system in suspend as **5.1.7** describes.
2. Wake the system.
3. Check operation of the DUT.
4. **Pass** is considered when all following items meet:
   - System resumes well.
   - Active operation initiated in previous step continues without error.
5. **Fail** is considered when either of the following items meets:
   - System does not resume.
   - System blue screens or locks up.
   - DUT is not functional or does not continue operation in the previous step.

5.1.9 Root port test

5.1.10 S4 active hibernate test

Test Instructions:

1. Stop operation of all devices!
2. Plug DUT into a root port of the system's motherboard.
3. Operate the DUT while the system enters hibernation (Start->Shutdown->Hibernate, wait 5 – 10 seconds after monitor is dark)
4. **Pass** is considered when all following items meet:
   - System hibernates well.
5. **Fail** is considered when any of the following items meets:
   - System fails to hibernate.
   - System blue screens or locks up.

5.1.11 S4 active hibernate resume test

Test Instructions:

1. Place the system in hibernation as **5.1.10** describes.
2. Turn on the system.

3. Check operation of all USB devices including DUT.
4. **Pass** is considered when all following items meet:
   - System resumes well.
   - Active operation initiated in previous step continues without error.
5. **Fail** is considered when either of the following items meets:
   - System does not resume.
   - System blue screens or locks up.
   - DUT is not functional or does not continue operation in the previous step.

5.1.12 Topology change to UHCI

Test Instructions:

1. Change the **EHCI** motherboard to **UHCI** motherboard. Other connections are all the same. See Figure 133 above.
2. Run the whole tests from5.1.1 to 5.1.11.
3. Record the test result.

5.1.13 Topology change to OHCI

Test Instructions:

- Change the **EHCI** motherboard to **OHCI** motherboard. Other connections are all the same. See Figure 133 above.
- Run the whole tests from 5.1.1 to 5.1.11.
- Record the test result.

5.1.14 Topology change to XHCI

Test Instructions:

- Change the **EHCI** motherboard to **XHCI** motherboard. Other connections are all the same. See Figure 133 above.
- Run the whole tests from 5.1.1 to 5.1.11.
- Record the test result.

5.2 Embedded host interoperability test

Targeted Hosts or OTG acting as a Host, are tested for interoperability with peripherals from the device's own Targeted Peripheral List plus other retail USB products which could be attached to the Targeted Host.

Silent failures are not allowed and therefore a clear message shall be generated when any sort of error situation occurs. For example, where hubs are non-supported, a clear "Hub not supported" or similar error message appears and not a generic "not supported" or similar error message.

See the detailed description of Embedded Host Interoperability Test, you can refer **Chapter 7** of "***USB On-The-Go and Embedded Host Automated Compliance Plan***".

Test Items:

- A-UUT Functionality B-device
- A-UUT Category Functionality B-device
- A-UUT Boot Test
- 7A-UUT Legacy Speed Test

- A-UUT Concurrent and Independently Test
- A-UUT Unsupported device Message Test
- A-UUT Hub Error message Test
- A-UUT Hub Functionality Test
- A-UUT Hub maximum tier Test
- A-UUT Hub Concurrent and Independent Test
- A-UUT Bus powered hub power exceeded Test
- A-UUT Maximum concurrently device exceed message Test
- A-UUT Standby Test
- A-UUT Standby Disconnect Test
- A-UUT Standby Attach Test
- A-UUT Standby Remote Wake-up Test

Test Report:

Table 21. Embedded Host Interoperability Test Report

Num	Test Item	Result
1	7.3.1 A-UUT Functionality B-device 30	***N/A***
2	7.3.2 A-UUT Category Functionality B-device	Pass
3	7.3.3 A-UUT Boot test	Pass
4	7.3.4 A-UUT Legacy Speed test	Pass
5	7.3.5 A-UUT Concurrent and Independently test 31	***N/A***
6	7.3.6 A-UUT Unsupported device Message test	Pass
7	7.3.7 A-UUT Hub Error message test 3 2	***N/A***
8	7.3.8 A-UUT Hub Functionality test	Pass
9	7.3.9 A-UUT Hub maximum tier test	Pass
10	7.3.10 A-UUT Hub Concurrent and Independent test	Pass
11	7.3.11 A-UUT Bus powered hub power exceeded test	Pass
12	7.3.12 A-UUT Maximum concurrently device exceed message test	Pass
13	7.3.13 A-UUT Standby test	Pass
14	7.3.14 A-UUT Standby Disconnect test	Pass
15	7.3.15 A-UUT Standby Attach test	Pass
16	7.3.16 A-UUT Standby Topology Change test	Pass
17	7.3.17 A-UUT Standby Remote Wake-up test	Pass

Note:

- *i.MX does not support peripherals identified by their VID/PID, so this test is not needed.*
- *Concurrent and Independently test is only applied to EH with multi ports, i.MX6 EVK only have one downstream port, so this test is not needed.*
- *i.MX supports Hub, so this test is not needed.*

5.2.1 A-UUT functionality B-device

Table 22. A-UUT Functionality B-device

Purpose	Prove the functionality of an OTG A-device or EH
Applies to	OTG A-devices and EH's that perform VID/PID detection of TPL peripherals
Description	Test the functionality of the TPL peripherals
Test setup	At least one TPL device corresponding to each supported category
Preconditions	The A-UUT is powered ON

Table 22. A-UUT Functionality B-device*...continued*

	Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	TPL2-4, TPL7
Pass Criteria	Prove the functionality of all TPL B-devices in combination with the A-UUT

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a B-device taken from the TPL and prove functionality.
3. Detach the B-device and see if the device is disconnected correctly.
4. Attach the B-device and prove functionality.
5. Repeat the above steps for each of the different supported category.
6. End of test.

5.2.2 A-UUT category functionality B-device

Table 23. A-UUT Category Functionality B-device

Purpose	Prove the category functionality of an OTG A-device or EH
Applies to	OTG A-devices and EH's that support a certain category of device
Description	Test the functionality of each of the supported categories
Test setup	- One B-device of each supported category with 500 mA in their descriptor, if not available use a device with highest max power descriptor value. - If available one B-device of each supported category with an additional interface(s) (composite device). If not available use a device with one interface.
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	MSG2, MSG3, TPL2-4, TPL7
Pass Criteria	Prove the functionality of the B-devices in combination with A-UUT For the composite device, it is not mandatory to prove functionality however if the device does not operate a clear message shall be generated by the A-UUT. If a device does not work a clear error message shall be shown to the user.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a B-device taken and prove functionality.
3. Detach the B-device and see if the device is disconnected correctly.
4. Attach the B-device and prove functionality.
5. Repeat the above steps for each of the different supported category with five different peripherals.
6. End of test.

5.2.3 A-UUT boot test

Table 24. A-UUT Boot Test

Purpose	Prove the functionality of an OTG A-device or EH after boot

Table 24. A-UUT Boot Test*...continued*

Applies to	OTG A-devices and EH's
Description	Observe boot behavior while a B-device is attached
Test setup	One B-device of each supported category.
Preconditions	The A-UUT is powered OFF Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C3
Pass Criteria	Prove the functionality of the B-devices in combination with A-UUT For the composite device it is not mandatory to prove functionality however if the device does not operate a clear message shall be generated by the A-UUT. If a device does not work a clear error message shall be shown to the user.

Test Instructions:

1. Power OFF the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a B-device taken and prove functionality.
3. Power ON the A-UUT.
4. Prove functionality of the B-device.
5. Repeat the above steps for each of the different supported category.
6. End of test.

5.2.4 A-UUT legacy speed test

Table 25. A-UUT Legacy Speed Test

Purpose	Prove the functionality of the OTG A-device or EH in Full or Low-Speed
Applies to	High-Speed OTG A-devices and EH's that have a Full or Low-Speed device on their TPL. Perform this test only if it not has been performed in one of the previous tests.
Description	Test the functionality of the Full or Low-Speed TPL device
Test setup	One supported Full Speed (Full Speed support is mandatory) or Low-speed device
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	E15, E18
Pass Criteria	The functionality of the full or low-speed device is proven. If a device does not work a clear error message shall be shown to the user.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a Full Speed B-device and prove functionality.
3. End of test.

5.2.5 A-UUT concurrent and independently test

Table 26. A-UUT Concurrent and Independently Test

Purpose	Prove the functionality of all downstream ports

Table 26. A-UUT Concurrent and Independently Test *...continued*

Applies to	EH with multiple ports
Description	Test the concurrent and independent functioning of the TPL peripherals on each downstream port.
Test setup	For each downstream port, a similar device from the TPL. If detection is made using VID/PID and/or for category support the number of B-devices is equal to the number of ports. This test shall be performed on each supported category.
Preconditions	The A-UUT is powered ON
Checklist	E17
Pass Criteria	The A-UUT can operate the device concurrently and independently or a selection method is available for the end-user to select a device. An A-UUT is allowed to handle a limited number of concurrent peripherals

Test Instructions:

1. Power ON the A-UUT.
   - If the B-device requires external power, power on the B-device.
2. Attach a B-device to Port 1.
3. Attach another B-device of the same category to an available downstream port.
4. Continue attaching B-devices of the same category until all ports are full.
5. Prove functionality of each attached B-device.
   - Do they operate concurrently and independently.
   - Or is a selection method available such that the user can select the active B-device.
6. Remove one device and replace it with a device of another category if multiple categories are supported.
7. Remove all peripherals.
8. Repeat the above steps for each of the different supported category.
9. End of test.

5.2.6 A-UUT unsupported device message test

Table 27. A-UUT Unsupported device Message Test

Purpose	Prove that the OTG A-device or EH generates the correct error message when attaching an unsupported device
Applies to	OTG A-devices and EH's
Description	Observe error messages when attaching unsupported peripherals
Test setup	- One unsupported Low-speed device - One unsupported Full-speed device - One unsupported High-speed device - One unsupported Super-speed device - One unsupported composite device with more than 8 interfaces
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	E15, E18
Pass Criteria	The functionality of the full or low speed device is proven. If a device does not work a clear error message shall be shown to the user.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach one of the peripherals listed above.

3. Observe if a clear message is generated to the end-user.
4. Repeat the above steps for each of the peripherals listed in the Test setup.
5. End of test.
6. Note that an error message should be generated when attaching a device in a device class which is not already covered by a product on the TPL. It is not permitted to support device classes without listing corresponding products on your TPL.

5.2.7 A-UUT hub error message test

Table 28. A-UUT Hub Error message test

Purpose	Prove that the OTG A-device or EH generates the correct error message when attaching an unsupported device
Applies to	OTG A-devices and EH's
Description	Observe error messages when attaching unsupported peripherals
Test setup	- One unsupported Low-speed device - One unsupported Full-speed device - One unsupported High-speed device - One unsupported Super-speed device - One unsupported composite device with more than 8 interfaces
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	E15, E18
Pass Criteria	The functionality of the full or low speed device is proven. If a device does not work, a clear error message shall be shown to the user.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach the hub.
3. A clear hub not supported message should appear.
4. Attach a TPL device downstream from the hub.
5. Check that the device does not function downstream from the hub.
6. End of test.

5.2.8 A-UUT hub functionality test

Table 29. A-UUT Hub Functionality test

Purpose	Prove that a hub attached to an OTG A-device or EH hub either functions or causes a hub error message
Applies to	OTG A-devices and EH's which support hub(s)
Description	Test the hub functionality with TPL peripherals
Test setup	- One 4-port High-Speed Self-Powered Hub (If hub support is performed by VID/PID in TPL use this Hub) - At least one TPL device from each category - FS device if listed on TPL (for TT stress)
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	TPL4, MSG2, MSG3, MSG5
Pass Criteria	Prove the functionality of the all device categories listed in TPL attached downstream from one hub

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach the hub.
3. Attach one supported High-speed device downstream from the hub and prove its functionality.
4. Prove the functionality of each supported category downstream from one hub.
5. Detach the high-speed device.
6. Attach one supported Full speed device (if supported) downstream from the hub and prove its functionality.
7. Detach the full speed device.
8. End of test.

5.2.9 A-UUT hub maximum tier test

Table 30. A-UUT Hub maximum tier test

Purpose	Prove that a hub attached to an OTG A-device or EH hub either functions or causes a hub error message
Applies to	OTG A-devices and EH's which support hub(s)
Description	Test the hub functionality with TPL peripherals
Test setup	- One 4-port High-Speed Self-Powered Hub (If hub support is performed by VID/PID in TPL use this Hub) - At least one TPL device from each category - FS device if listed on TPL (for TT stress)
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	TPL4, MSG2, MSG3, MSG5
Pass Criteria	Prove the functionality of the all device categories listed in TPL attached downstream from one hub

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
2. Attach hubs up to the maximum tier.
3. Attach one TPL device downstream from the last hub and prove functionality.
4. Attach another hub downstream from the max tier of hubs.
5. Check that an appropriate error message is generated.
6. End of test.

5.2.10 A-UUT hub concurrent and independent test

Table 31. A-UUT Hub Concurrent and Independent test

Purpose	Prove that a hub attached to an OTG A-device or EH hub either functions or causes a hub error message
Applies to	OTG A-devices and EH's which support hub(s)
Description	Test the hub functionality with TPL peripherals
Test setup	- One 4-port High-Speed Self-Powered Hub (If hub support is performed by VID/PID in TPL use this Hub) - At least one TPL device from each category

Table 31. A-UUT Hub Concurrent and Independent test*...continued*

	- FS device if listed on TPL (for TT stress)
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	TPL4, MSG2, MSG3, MSG5
Pass Criteria	Prove the functionality of the all device categories listed in TPL attached downstream from one hub

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a B-device to the hub's downstream port 1.
3. Attach similar peripherals to available downstream hub ports.
4. Prove the functionality of each attached device.
   - Do they operate concurrently and independently
   - Or is a selection method available such that the user can select the active device?
5. Detach one device and replace it with a device of another category if multiple categories are supported.
6. Detach all peripherals.
7. Repeat the above steps for each of the different supported category.
8. End of test.

5.2.11 A-UUT bus-powered hub power exceeded test

Table 32. A-UUT Bus powered hub power exceeded test

Purpose	Prove that the host generates an appropriate error message when connecting a high-power device downstream from a bus-powered hub.
Applies to	OTG A-device and EH's which support bus powered hubs.
Description	Check that the A-UUT is able to detect and prevent an over current event on a bus-powered hub.
Test setup	A bus powered hub. High-power device from the TPL (Max power descriptor >100 mA). If no high-power device is available on TPL, use other high-power devices.
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C5
Pass Criteria	An appropriate error message was generated.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a bus powered Hub.
3. Attach a high-power device downstream from a bus powered hub.
4. Check that an appropriate error message is generated by the A-UUT.
5. End of test.

5.2.12 A-UUT maximum concurrently device exceed message test

Table 33. A-UUT Maximum concurrently device exceed message test

Purpose	OTG A-devices and EH's which support a limited number of peripherals concurrently
Applies to	Test the A-UUT for appropriate behavior when exceeding the maximum number of supported concurrent peripherals up to a maximum of four.
Description	May require hubs to be attached in order to exceed maximum number of peripherals. The number of similar peripherals that the A-UUT is able to handle concurrently plus one up to a maximum of four.
Test setup	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Preconditions	MSG1, MSG2, MSG7
Checklist	Prove that the specified maximum number of concurrent peripherals function correctly, and either that an error message is given when exceeding this number or that it is able to handle 4 peripherals.
Pass Criteria	An appropriate error message was generated.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a B-device and prove its functionality.
3. Keep increasing the number of similar peripherals attached until the maximum number is reached, proving their functionality each time.
4. Attach an additional similar peripherals.
5. Check that an appropriate error message is generated by the A-UUT or that it is able to handle 4 peripherals without error.
6. End of test.

5.2.13 A-UUT standby test

Table 34. A-UUT Standby test

Purpose	Prove that the host can handle standby correctly
Applies to	OTG A-devices and EH products which support standby
Description	With a B-device connected, verify standby operation of the A-UUT.
Test setup	At least one TPL device from each category
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a B-device and prove its functionality.
3. Place the A-UUT in standby (follow the A-UUT vendor guidelines to force the host into standby mode).
4. Take the A-UUT out of standby mode (A-UUT may also come out of standby automatically on detach).

5. Prove the functionality of the B-device.
6. Repeat the above steps for each of the different supported category.
7. End of test.

5.2.14 A-UUT standby disconnect test

Table 35. A-UUT Standby Disconnect test

Purpose	Prove the standby functionality of the OTG A-device or EH when a peripheral is detached during standby mode
Applies to	OTG A-devices and EH's which support standby
Description	Detach TPL peripheral while A-UUT is in standby mode. Verify that the A-UUT operates correctly after the A-UUT leaves standby mode.
Test setup	At least one TPL peripheral
Preconditions	The A-UUT is powered ON Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a peripheral and prove its functionality.
3. Place A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
4. Detach Peripheral.
5. Take the A-UUT out of standby (A-UUT may also come out of standby automatically on detach).
6. Verify that A-UUT operates correctly.
7. If different types of standby modes are supported repeat the test until all modes have been tested.
8. End of test.

5.2.15 A-UUT standby attach test

Table 36. A-UUT Standby Attach test

Purpose	Prove the standby functionality of the OTG A-device or EH when a peripheral is attached during standby mode
Applies to	OTG A-devices and EH's which support standby
Description	Attach a TPL peripheral while the A-UUT is in standby mode. Verify that A-UUT operates correctly after the A-UUT leaves standby mode
Test setup	At least one TPL peripheral
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.

2. Place the A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
3. Attach Peripheral.
4. Take the A-UUT out of standby mode (A-UUT may also come out of standby automatically on attach).
5. Verify that A-UUT behaves normally.
6. Prove the functionality of the peripheral.
7. If different types of standby modes are supported repeat the test until all modes have been tested.
8. End of test.

5.2.16 A-UUT standby topology change test

Table 37. A-UUT Standby Topology Change test

Purpose	Prove the standby functionality of the OTG A-device or EH when the topology changes during standby.
Applies to	OTG A-devices and EH's which support standby
Description	Switch the topology of TPL peripherals while the A-UUT is in standby, verify that the A-UUT does not behave abnormally after the A-UUT leaves standby mode
Test setup	At least one TPL peripheral
Preconditions	The A-UUT is powered ON. Use a Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2
Pass Criteria	Compliant standby behavior is observed.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach a hub (if necessary)
3. Attach the B-device and prove functionality.
4. Place the A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
5. Detach the B-device and attach it to another EH port or another downstream hub port.
6. Take the A-UUT out of standby mode standby (A-UUT may also come out of standby automatically on attach).
7. Verify that A-UUT behaves normally.
8. Prove functionality of the B-device.
9. If different types of standby modes are supported repeat the test until all modes have been tested.
10. End of test.

5.2.17 A-UUT standby remote wake-up test

Table 38. A-UUT Standby Remote Wake-up test

Purpose	Prove the remote wake-up functionality of an OTG A-device or EH
Applies to	OTG A-devices or EH's which support standby and remote wake-up.
Description	Perform a USB remote wake-up event and verify that the A-UUT operates correctly after the A-UUT leaves standby mode.
Test setup	At least one TPL peripheral which supports remote wake-up.
Preconditions	The A-UUT is powered ON. Use Micro-A plug to Standard-A Receptacle adapter if the product is an OTG device.
Checklist	C2

Table 38. A-UUT Standby Remote Wake-up test*...continued*

Pass Criteria	Compliant standby behavior is observed when a remote wake-up event is performed during standby.

Test Instructions:

1. Power ON the A-UUT.
   - If the product is an OTG device with a Micro-AB receptacle, attach a Micro-A plug to Standard-A Receptacle adapter.
   - If the B-device requires external power, power on the B-device.
2. Attach the B-device.
3. Prove the functionality of the A-UUT with the B-device.
4. Put the A-UUT into standby (follow A-UUT vendor guidelines to force the host in standby mode).
5. Perform a USB remote wake-up event from the B-device.
6. Prove the functionality of the A-UUT with the B-device.
7. End of test.

6 Auto PET tests

6.1 Introduction of PET

The PET (Protocol and Electrical Tester) is a unit, designed to perform compliance testing or assist with development work leading toward compliance testing on On-the-Go, Battery Charging and other general USB applications.

The tests in this section test only a partial list of all the possible parameters and compliant behavior. The tests should not be considered as a full validation test plan. See the detailed description of PET Test, you can refer **Chapter 6** of "***USB On-The-Go and Embedded Host Automated Compliance Plan***".

The Packet-Master USB-PET is used by most of the Compliance Test Labs, which is delivered complete with MQP's Windows application ***GraphicUSB*** for generating the test reports, and also analyzer-style captures.

Figure 135. Packet-Master USB-PET

6.2 Test environment

6.2.1 Test cables required

The cables required by the PET tester are described below.

Each cable should be labeled, and specify the lead loop resistance value, required to be entered into the test dialog, if the cable is replaced. The tester application contains a checkbox to specify whether the UUT has a captive cable, as in this case the captive test cable is deemed to be part of the unit under test.

Table 39. Special Test Cable A

Micro-B plug to Micro-B plug		
Micro-B plug (PET)	**Micro-B plug (UUT)**	**Purpose**
1	1	VBUS
2	2	D-
3	3	D+
4	4	ID
5	5	GND

Table 40. Special Test Cable B

Micro-B plug to Standard-A plug		
Micro-B plug (PET)	**Standard-A plug (UUT)**	**Purpose**
1	1	VBUS
2	2	D-
3	3	D+
nc		
5	4	GND

6.2.2 Test setups

The cables required by the PET tester are described below.

Each cable should be labeled, and specify the lead loop resistance value, required to be entered into the test dialog, if the cable is replaced. The tester application contains a checkbox to specify whether the UUT has a captive cable, as in this case the captive test cable is deemed to be part of the unit under test.

OTG device as Unit-Under-Test

When running a test-suite relating to an OTG device, the first test prompts you to attach it to the PET using ‘Special Cable A’.

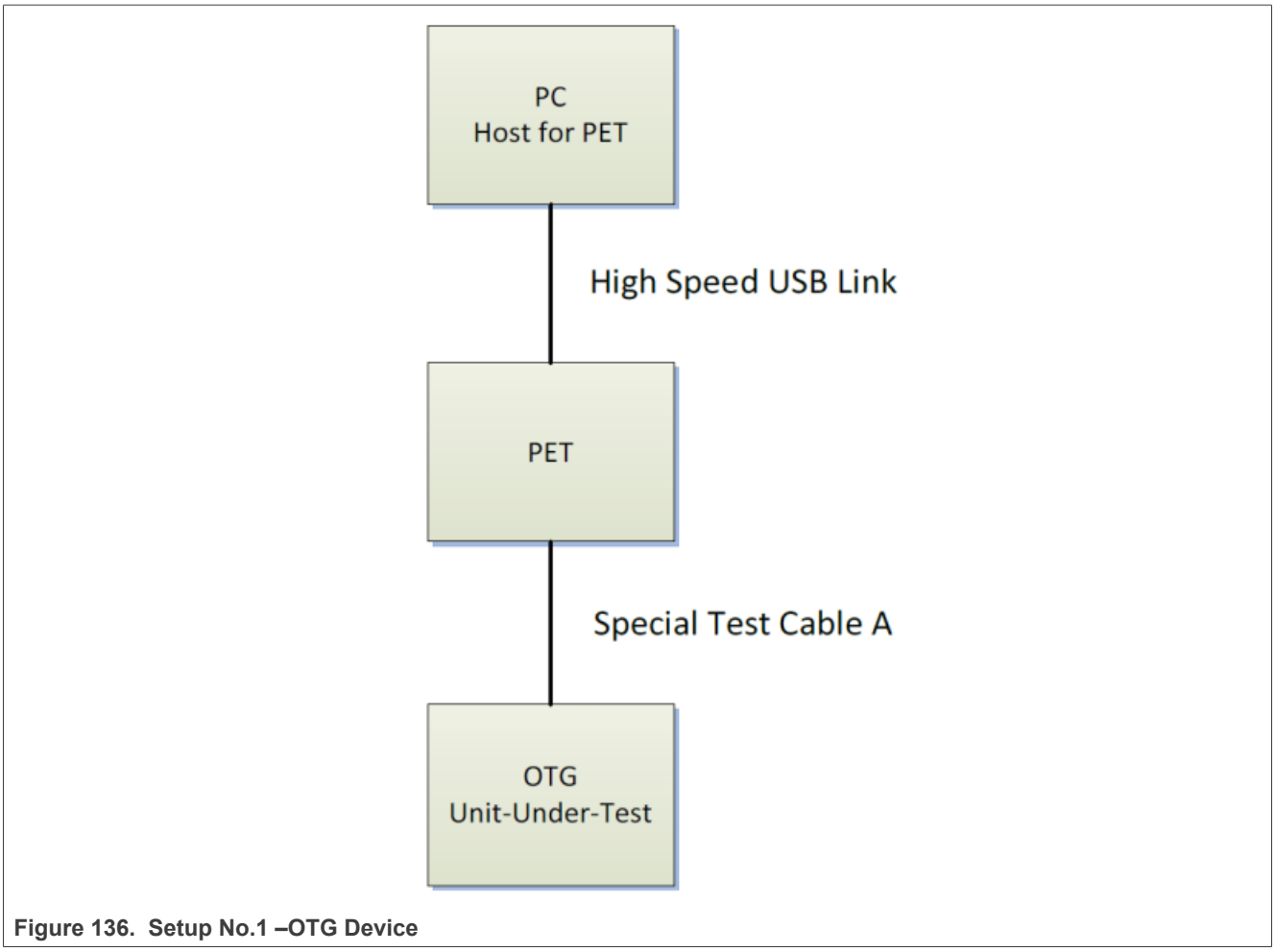

Figure 136. Setup No.1 –OTG Device

Embedded Host as Unit-Under-Test

When running a test-suite relating to an Embedded Host using a Standard-A receptacle, the first test prompts you to attach it to the PET using ‘Special Cable B’.

When running a test-suite relating to an Embedded Host using a Micro-AB receptacle, the first test prompts you to attach it to the PET using ‘Special Cable A’.

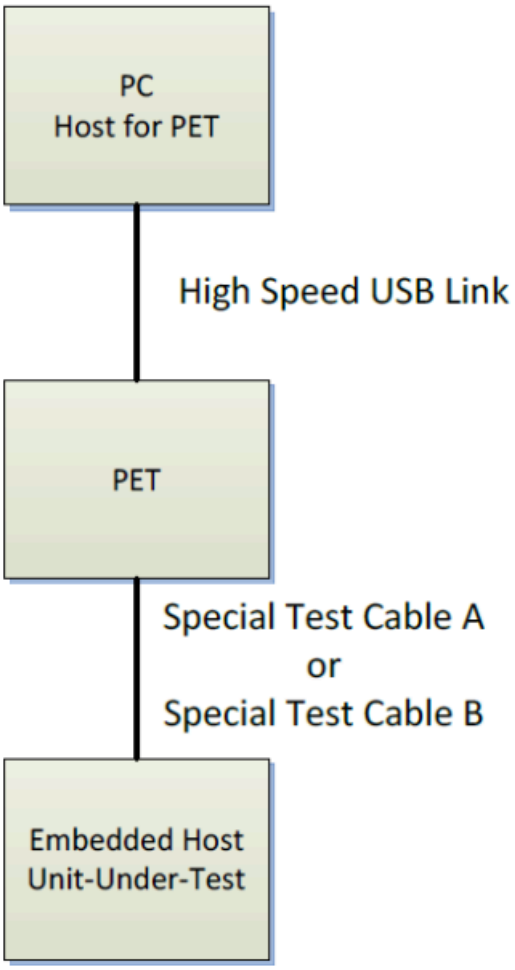

Figure 137. Setup No.2 –Embedded Host

Peripheral Only as Unit-Under-Test

When running a test-suite relating to a Peripheral-Only OTG device, the first test prompts you to attach it to the PET using ‘Special Cable A’.

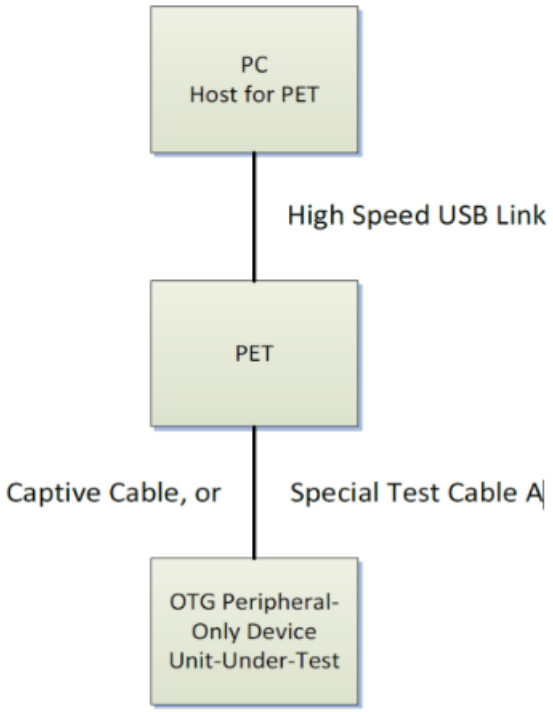

Figure 138. Setup No.3 –Peripheral Only

6.2.3 User input before test runs

Before running any test suite, the PET must be informed of a number of parameters by the test operator. Most of the information should be available from the Checklist supplied by the vendor. The following tables describe the information required. Typically, PET software would modify the available options to the ones applying to the currently chosen device type.

Table 41. Information Obtained From Checklist

Input	Type	Purpose	Checklist Ref
OTG Device	Mutually exclusive check boxes	Automatically selected by UUT items OTG-A or OTG-B.	PI2
Embedded Host		Automatically selected by UUT item Embedded Host.	
Peripheral Only		Automatically selected by UUT item Peripheral Only.	
Uses Micro-AB	Checkbox	Check this box for an EH which uses a Micro-AB receptacle instead of a Standard-A receptacle. It is automatically selected for OTG devices.	PI5a
Supports Sessions	Checkbox	Check this box if the OTG A-UUT or EH with Micro-AB receptacle does not keep VBUS enabled all the time that the ID pin is held low. Check this box for an EH with Standard-A receptacle which does not keep VBUS high all the time it is powered up. In either case, it is assumed that SRP or ADP is available to detect the presence of a device.	PI10
SRP as A-device	Checkbox	Check this box if the UUT, as an A-device, supports detecting, and acting on, an SRP pulse generated by a connected device.	PI13
HNP as A-device	Checkbox	Check this box if the UUT, as an A-device, supports HNP to enable the connected B-device to become host if it so requires.	PI13
HNP Polling as A-device	Checkbox	Check this box if the UUT, as an A-device, supports HNP polling. If it does, it is allowed to remain as host, for as long as the other device does not set its Host Request Flag.	PI13

Table 41. Information Obtained From Checklist*...continued*

Input	Type	Purpose	Checklist Ref
ADP as A-device	Checkbox	Check this box if the UUT, as an A-device, supports ADP probing to detect the presence or otherwise of a connected device.	PI13
SRP as B-device	Checkbox	Check this box if the UUT, as a B-device, supports generating an SRP pulse in order to start a session (cause the connected A-device to turn on VBUS).	PI20
HNP as B-device	Checkbox	Check this box if the UUT, as a B-device, supports HNP to allow it to become host if it so requires.	PI20
ADP as B-device	Checkbox	Check this box if the UUT, as a B-device, supports ADP sensing and probing to detect the presence or otherwise of a connected device.	PI20
FS Not Available	Checkbox	Check this box if UUT does not fully support full-speed operation. This is not permitted for an OTG device, but may be for an Embedded Host.	PI11, PI18
IA_VBUS_RATED	Edit box	The rated output current of an A-device in mA units.	PI8
bMaxPower	Edit box	bMaxPower (sic) is the highest current, in mA, declared in any of the device's Configuration Descriptors. This value ignores current drawn under the Battery Charging provisions.	PI17
TPWRUP_RDY	Edit box	Maximum time, in seconds, specified by vendor from powering on the UUT until it is ready to perform USB functionality. By default it is set to 30 seconds, but a vendor is permitted to specify a longer time.	PI24
TA_WAIT_BCON max	Edit box	The maximum time, in seconds, that VBUS is left on for by an A-device, in the absence of a B-device connecting. The default value is 30 seconds. A vendor is permitted to specify a longer time, but should be aware that this will have an impact on the time taken for, and therefore possibly the cost of, compliance testing.	PI10
Unknown Dev (No HNP)	Edit boxes	The test uses the VID/PID combination specified during tests for error messages, when an unknown B-device, not capable of HNP, is connected. A default value (1A0A/0201) is used, but any other device not on the UUT's TPL may be defined here.	-
Unknown Dev (HNP)	Edit boxes	The test uses the VID/PID combination specified during tests for error messages, when an unknown B-device, capable of HNP, is connected. A default value (1A0A/0202) is used, but any other device not on the UUT's TPL may be defined here.	-

6.3 A-UUT tests

Test Items:

- A-UUT VBUS Voltage and Current Measurements
- A-UUT Bypass Capacitance
- A-UUT SRP
- A-UUT ADP
- A-UUT Leakage
- EH, Capable of ADP and SRP, State Transition Test (Standard-A)
- EH, Capable of ADP but not SRP, State Transition Test (Standard-A)
- EH, Capable of SRP but not ADP, State Transition Test (Standard-A)
- EH with no Session Support State Transition Test (Standard-A)
- EH, Capable of ADP and SRP, (Micro-AB) or OTG-A , Capable of ADP and SRP but not HNP, State Transition Test
- EH, Capable of ADP but not SRP, (Micro-AB) or OTG-A , Capable of ADP but not SRP or HNP, State Transition Test
- EH, Capable of SRP but not ADP, (Micro-AB) or OTG-A , Capable of SRP but not ADP or HNP, State Transition Test

- EH with no Session Support State Transition Test (Micro-AB), or OTG-A with no Session or HNP Support
- A-UUT “Device No Response” for connection timeout
- A-UUT “Unsupported Device” Message
- A-UUT “Device No Response” for HNP enable
- EH using Micro-AB “Incorrect Connection”

Test Report:

Table 42. PET A-UUT Test Report

Num	Test Item	Result
1	6.7.2 A-UUT Initial Power-up Test	Pass
2	6.7.4 A-UUT VBUS Voltage and Current Measurements	Pass
3	6.7.5 A-UUT Bypass Capacitance	Pass
4	6.7.6 A-UUT SRP	Pass
5	6.7.8 A-UUT ADP	Pass
6	6.7.9 A-UUT Leakage	Pass
7	6.7.14 EH, Capable of ADP and SRP, State Transition Test (Standard-A)	**N/A**
8	6.7.15 EH, Capable of ADP but not SRP, State Transition Test (Standard-A)	**N/A**
9	6.7.16 EH, Capable of SRP but not ADP, State Transition Test (Standard-A)	**N/A**
10	6.7.17 EH with no Session Support State Transition Test (Standard-A) 33	Pass
11	6.7.18 EH, Capable of ADP and SRP, (Micro-AB) or OTG-A , Capable of ADP and SRP but not HNP, State Transition Test	**N/A**
12	6.7.19 EH, Capable of ADP but not SRP, (Micro-AB) or OTG-A , Capable of ADP but not SRP or HNP, State Transition Test	**N/A**
13	6.7.20 EH, Capable of SRP but not ADP, (Micro-AB) or OTG-A , Capable of SRP but not ADP or HNP, State Transition Test	**N/A**
14	6.7.21 EH with no Session Support State Transition Test (Micro-AB), or OTG-A with no Session or HNP Support	**N/A**
15	6.7.22 A-UUT “Device No Response” for connection timeout	Pass
16	6.7.23 A-UUT “Unsupported Device” Message	Pass
17	6.7.24 A-UUT “Device No Response” for HNP enable	**N/A**
18	6.7.25 EH using Micro-AB “Incorrect Connection” 34	**N/A**

Note:

- *i.MX Embedded Host contains a standard Type A receptacle, and it does not support ADP, SRP, HNP, session. So, only 6.7.17 should be test.*
- *Only Embedded Host using Micro-AB receptacle must run this test.*

Test Instructions:

- Install and run ***GraphicUSB*** on computer.
- Click **Operation** -> **Compliance Tester** on the menu bar. The Test Suite dialog appears as shown in Figure 139 below.
- Select the type of unit 1 to be tested using the **Unit Under Test** combo box.
- Then refer to the completed Compliance Checklist, and ensure that the other **Unit Under Test** checkboxes and parameters are correctly entered.
- The appropriate tests are loaded into the 'Selected Tests' list box. These tests are now ready to automatically run in sequence.
- Specify a Product name so that the reports can be saved into an appropriate folder.
- Click **Run** to start the test suite.
- A text report file is created, into which the test results are written, as shown in **Fig6-5** below.

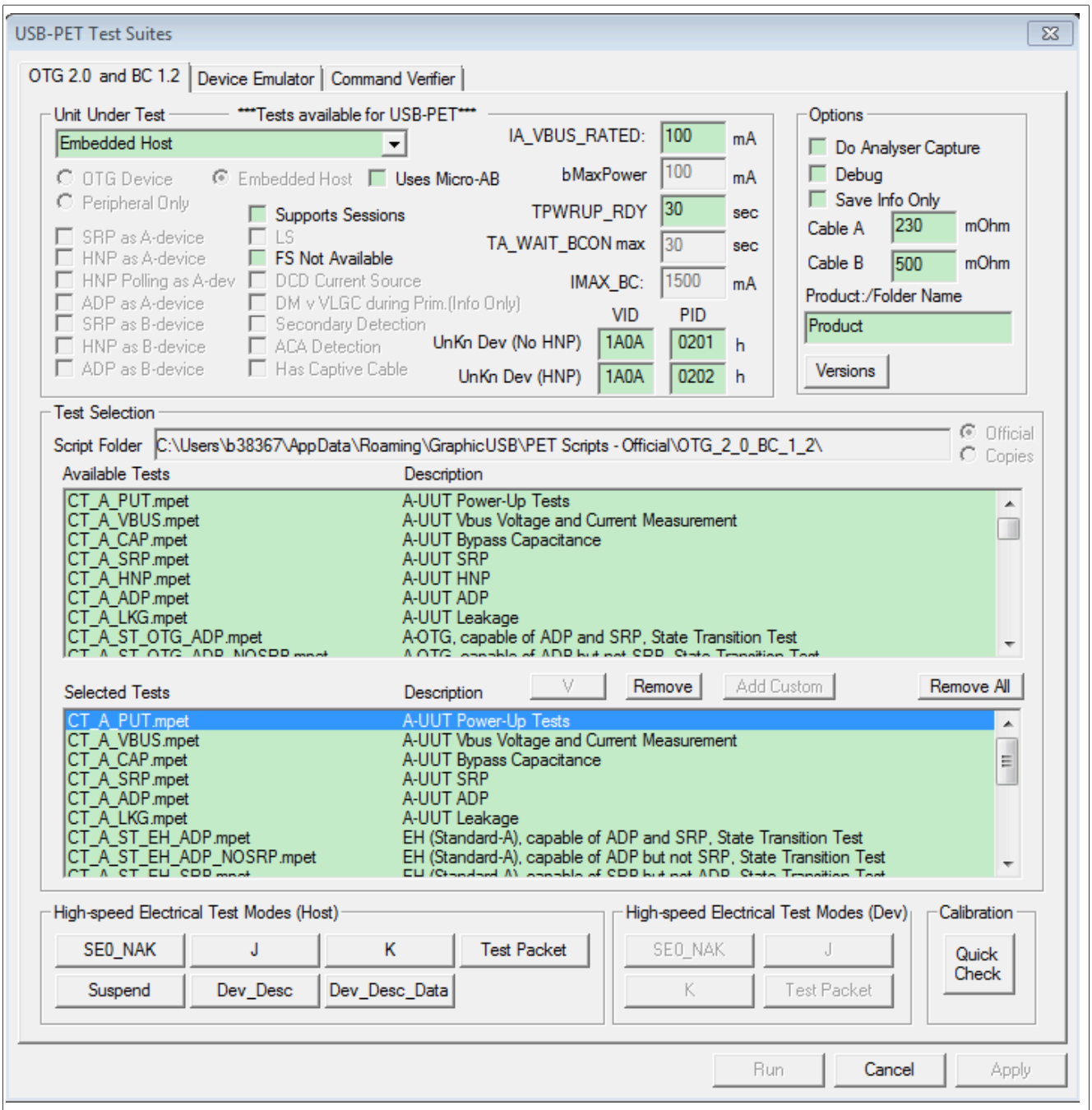

Figure 139. USB-PET Test Suites

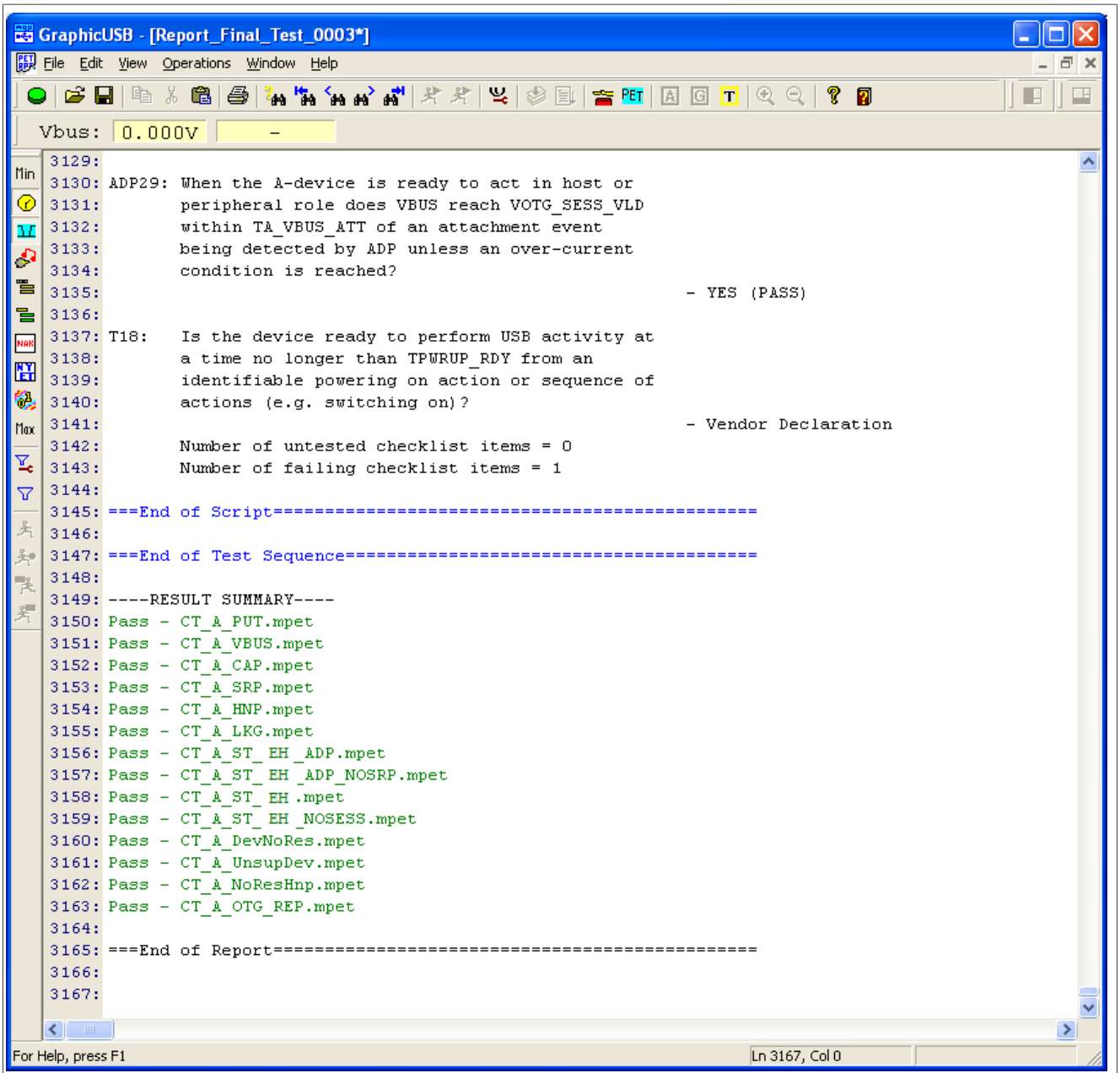

Figure 140. USB-PET Test Report

7 Type-C function/PD

TBD

8 Registers and operation guide

8.1 i.MX 6 USB PHY registers and software configurations

USB signal integrity depends on many factors, such as circuit design, PCB layout, Stack-up, Impedance. Each product might be different from another, so customers must fine-tune the parameters in order to obtain the best signal quality.

The test board has routed out two USB Ports: one OTG 33, one Host. Each of the port has several registers to adjust the signal voltage level, slew rate. See the detailed description of the registers in Freescale app note ***AN4589:*** *Configuring USB on i.MX 6 Series*.

Compared to standard Linux/Android release, you may need to do below software changes to implement the certification tests, i.MX 6 Series is applicable from imx_3.10.31_1.1.0 Linux BSP GA release, for the release before that, user may need to apply the related patches before doing below things, and some examples may be different for former releases, the user must change accordingly. See the detailed information in this document "How to do USB Compliance Test for 3.10.y kernel", you may download it from NXP community.

8.1.1 USBPHYx_TXn

The USB PHY Transmitter Control Register handles the transmit controls. Bit fields TXCAL45DP, TXCAL45DM, D_CAL are usually to adjust the output voltage amplitude.

```
Command samples:
/unit_tests/memtool 0x20c9010 1 // OTG Port Read register data35
/unit_tests/memtool 0x20cA010 1 // Host Port Read register data
/unit_tests/memtool 0x20c9010=0x1c060607 //write OTG_PHY_TX36
/unit_tests/memtool 0x20cA010=0x1c060607 //write HOST_PHY_TX
```

Note:

- *Software does not support full feature OTG currently, this port is used as Device or Embedded Host, selected by USB_ID.*
- *Remember connecting DUT to corresponding Host/Device before adjusting the registers, otherwise the operation might be invalid or cause system crash.*

Table 43. USBPHYx_TXn Register Settings

Name	USBPHYx_TXn															
Description	The USB PHY Transmitter Control Register handles the transmit controls.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
Field definitions	RSVD5			TX_EDGECTRL			TX_SYNC_INVERT	TX_SYNC_MUX	RSVD4		TXENCAL45DP	RSVD3	**TXCAL45DP**			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	RSVD2		TXENCAL45DN	RSVD1	**TXCAL45DN**				RSVD0			**D_CAL**				
Signal Names	**Description**															
TXCAL45DP	Bit fields TXCAL45DP and TXCAL45DM allow for changing the resistance of the high-speed termination. Increasing the termination resistor value will increase the DM/DP signals level. Decode to select a 45-Ohm resistance to the USB_DP output pin. Maximum resistance = 0000.															
TXCAL45DN	Decode to select a 45-Ohm resistance to the USB_DN output pin. Maximum resistance = 0000.															
D_CAL	This field allows for trimming the current reference for the high-speed driver. Reducing the resistance increases the driver current and therefore the amplitude of the transmitted signal will increase. Resistor Trimming Code: 0000 = 0.16 % 0111 = Nominal 1111 = +25 %															

8.1.2 PMU_REG_3P0

This register defines the control and status bits for the internal LDO_USB module, which is powered by either of the two USB VBUS pins. This regulator supplies only low-speed and full speed transceivers of USB PHYs, so it only impacts the voltage level of Full-speed and Low-speed transmission, but not the Hi-speed.

```
Command samples:
     /unit_tests/memtool 0x20c8120 1 //Read register data
     /unit_tests/memtool 0x20c8120=0x00011771 //write LDO_USB 3.2 V
     /unit_tests/memtool 0x20c8120=0x00010F71 // write LDO_USB 3.0 V
     /unit_tests/memtool 0x20c8120=0x00010071 // write LDO_USB 2.65 V
```

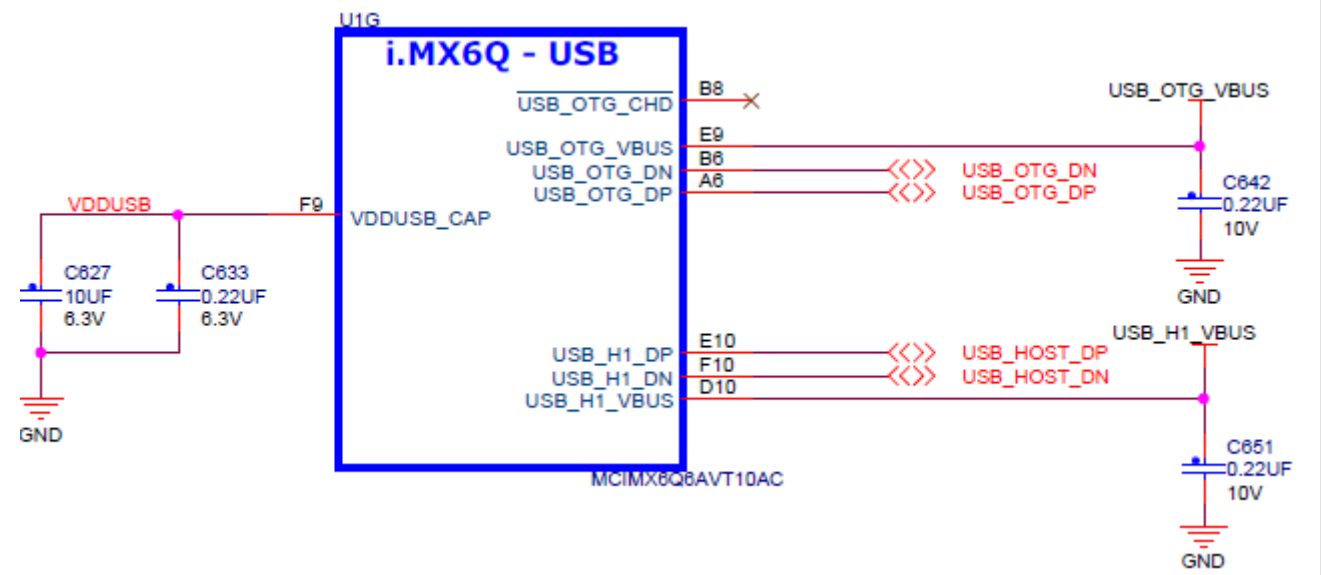

Figure 141. i.MX6 USB Ports

Table 44. USBPHYx_TXn Register Settings

Name	PMU_REG_3P0															
Description	This register defines the control and status bits for the 3.0 V regulator powered by the host USB VBUS pins.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved														OK_VDD3P0	BO_VDD3P0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	1	1	1	1	0	1	1	1	0	1	1	0
Field definitions	Reserved			**OUTPUT_TRG**					REG_3P0_VBUS_SEL	BO_OFFSET			Reserved	ENABLE_ILIMIT	ENABLE_BO	**ENABLE_LIN REG**
Signal Names	Description															
OUTPUT_TRG	Control bits to adjust the regulator output voltage in 25 mV steps. 0x1F - 3.4 V 0x0F - 3.0 V 0x00 - 2.625 V The chip functionality may be limited and not guaranteed near the extremes of the programming range.															
ENABLE_LIN REG	Control bit to enable the regulator output															

8.1.3 USBC_n_PORTSC1

Port control is used for status port reset, suspend, and current connect status. It is also used to initiate test mode or force signaling and allows software to put the PHY into low power suspend mode and disable the PHY clock.

```
Command samples:
     /unit_tests/memtool 0x2184184 1 //OTG Port Read register data
     /unit_tests/memtool 0x2184184=0x18441205 //OTG Port Test packet
     /unit_tests/memtool 0x2184184=0x18411205 //OTG Port J_STATE
     /unit_tests/memtool 0x2184184=0x18421205 //OTG Port K_STATE
     /unit_tests/memtool 0x2184184=0x18431205 //OTG Port SE0 (host) /
 NAK(device)
     /unit_tests/memtool 0x2184184=0x18401305 //OTG Port Reset
     /unit_tests/memtool 0x2184184=0x18401285 //OTG Port Suspend
     /unit_tests/memtool 0x2184184=0x18401245 //OTG Port Resume
     /unit_tests/memtool 0x2184384 1 //Host Port Read register data
     /unit_tests/memtool 0x2184384=0x18441205 //Host Port Test packet
     /unit_tests/memtool 0x2184384=0x18411205 //Host Port J_STATE
     /unit_tests/memtool 0x2184384=0x18421205 //Host Port K_STATE
     /unit_tests/memtool 0x2184384=0x18431205 //Host Port SE0 (host) /
 NAK(device)
     /unit_tests/memtool 0x2184384=0x18401305 //Host Port Reset
     /unit_tests/memtool 0x2184384=0x18401285 //Host Port Suspend
     /unit_tests/memtool 0x2184384=0x18401245 //Host Port Resume
```

Table 45. USBC_n_PORTSC1 Register Settings

Name	USBC_n_PORTSC1															
Description	This register defines the control and status bits for the 3.0 V regulator powered by the host USB VBUS pin. It is also used to initiate test mode or force signaling and allows software to put the PHY into low power suspend mode and disable the PHY clock.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1		STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	**PTC**			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PIC		PO	PP	LS		HSP	**PR**	**SUSP**	**FPR**	OCC	OCA	PEC	PE	CSC	CCS
Field	**Description**															
PTC	Port Test Control - Read/Write. Default = 0000b. Refer to Port Test Mode for the operational model for using these test modes and the USB Specification Revision 2.0, Chapter 7 for details on each test mode. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. NOTE: Low-speed operations are not supported as a peripheral device. Any other value than zero indicates that the port is operating in test mode. Value Specific Test: 0000 TEST_MODE_DISABLE 0001 J_STATE 0010 K_STATE 0011 SE0 (host) / NAK (device) 0100 Packet 0101 FORCE_ENABLE_HS 0110 FORCE_ENABLE_FS 0111 FORCE_ENABLE_LS 1000-1111 Reserved															
PR	Port Reset - Read/Write or Read Only. Default = 0b. In Host Mode: Read/Write. 1=Port is in Reset. 0=Port is not in Reset. Default 0. When software writes a one to this bit the bus-reset sequence as defined in the USB Specification Revision 2.0 is started. This bit will automatically change to zero after the reset sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the reset duration is timed in the driver. In Device Mode: This bit is a read-only status bit. Device reset from the USB bus is also indicated in the USBSTS register.															
SUSP	Suspend - Read/Write or Read Only. Default = 0b.															

Table 45. USBC_n_PORTSC1 Register Settings*...continued*

Name	USBC_n_PORTSC1
	1=Port in suspend state. 0=Port not in suspend state. In Host Mode: Read/Write. Port Enabled Bit and Suspend bit of this register define the port states as follows: Bits [Port Enabled, Suspend] Port State 0x Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the host controller will unconditionally set this bit to zero when software sets the Force Port Resume bit to zero. The host controller ignores a write of zero to this bit. If host software sets this bit to a one when the port is not enabled (that is, Port enabled bit is a zero) the results are undefined.
FPR	Force Port Resume -Read/Write. 1= Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. Default = 0. In Host Mode: Software sets this bit to one to drive resume signaling. The Host Controller sets this bit to one if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J to K transition is detected, the Port Change Detect bit in the USBSTS register is also set to one. This bit will automatically change to zero after the resume sequence is complete. This behavior is different from EHCI where the host controller driver is required to set this bit to a zero after the resume duration is timed in the driver. In Device mode: After the device has been in Suspend State for 5 ms or more, software must set this bit to one to drive resume signaling before clearing. The Device Controller sets this bit to one if a J-to-K transition is detected while the port is in the Suspend state. The bit is cleared when the device returns to normal operation. Also, when this bit is cleared because a K-to-J transition detected, the Port Change Detect bit in the USBSTS register is also set to one.

8.1.4 Other useful commands and scripts

```
Command samples:
# Let the system enter suspend (standby) mode
echo mem > /sys/power/state
#Set Console as the system wakeup source
echo enabled > /sys/class/tty/ttymxc0/power/wakeup
#USB remote wakeup (as system wakeup source) is not enabled by default, user can
 enable this feature by using this script, after plugging in the USB device
for i in $(find /sys -name wakeup | grep usb);do echo enabled  > $i;echo "echo
 enabled > $i";done;
```

8.2 i.MX 7ULP USB PHY registers and software configurations

The test board has routed out two USB Ports: one Type-C, one Debug. Only the Type-C port has several registers to adjust the signal voltage level, slow rate.

8.2.1 USBPHY_TXn

The USB PHY Transmitter Control Register handles the transmit controls. Bit fields TXCAL45DP, TXCAL45DM, D_CAL are usually to adjust the output voltage amplitude.

```
Command samples:
/unit_tests/memtool 0x40350010 1      // Read register data
/unit_tests/memtool 0x 40350010=0x1c060607     //write USBPHY_TX
```

Table 46. USBPHYx_TXn Register Settings

Name	USBPHYx_TXn															
Description	The USB PHY Transmitter Control Register handles the transmit controls.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
Field definitions	Reserved			Reserved			Reserved	Reserved	Reserved		TXEN CAL 45DP	Reserved	**TXCAL45DP**			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 46. USBPHYx_TXn Register Settings ***...continued***

Name	USBPHYx_TXn															
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	Reserved		TXEN CAL 45DN	Reserved	**TXCAL45DM**				Reserved				**D_CAL**			
Signal Names	**Description**															
TXCAL45 DP	Decode to trim the nominal 45 Ω series termination resistance to the USB_DP output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.															
TXCAL45 DM	Decode to trim the nominal 45 Ω series termination resistance to the USB_DM output pin. Maximumresistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.															
D_CAL	Decode to trim the nominal 17.78 mA current source for the High-Speed TX drivers on USB_DP andUSB_DM. This current is directly proportional to the amplitude of the High-Speed TX eye diagram. 0000 Maximum current, approximately 19 % above nominal. 0111 Nominal 1111 Minimum current, approximately 19 % below nominal.															

8.2.2 Other useful commands and scripts

```
Command samples:
# Let the system enter suspend (standby) mode
echo mem > /sys/power/state
#Set Console as the system wakeup source
echo enabled > /sys/class/tty/ttymxc0/power/wakeup
#USB remote wakeup (as system wakeup source) is not enabled by default, user can
 enable this feature by using this script, after plugging in the USB device
for i in $(find /sys -name wakeup | grep usb);do echo enabled  > $i;echo "echo
 enabled > $i";done;
```

8.3 i.MX 8QXP/8QM USB PHY registers and software configurations

The test board has routed out two USB Ports: one Type-C, one Micro-AB.

8.3.1 Operation steps

8.3.1.1 Type C host mode

1. Power up board
2. At uboot console（When displaying 3, 2, 1, press the enter key to enter the uboot mode), input as shown in Figure 142.

```
                        >setenv fdt_file fsl-imx8qxp-mek-host.dtb
```

Note: *fsl-imx8qxp-mek-host.dtb*
For DRP application, the test fixture works abnormal if we configure controller as dual-role. So, the user must use host-only mode to pass signal test. Below are change for dts:

```
diff--git a/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
b/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
index d340e7065f6d..049c161d8974 100755
--- a/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
+++ b/arch/arm64/boot/dts/freescale/fsl-imx8qxp-mek.dtsi
@@ -909,7 +909,7 @@
 };
 & usbotg3 {
-       dr_mode = "otg";
```

```
+        dr_mode = "host";
         extcon = < & typec_ptn5110>;
         status = "okay";
 };
```

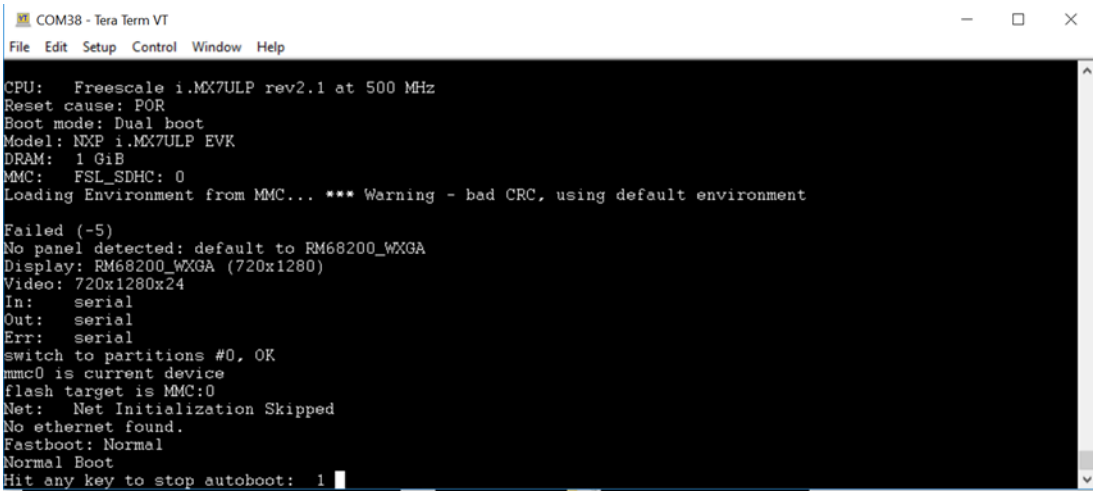

Figure 142. Uboot

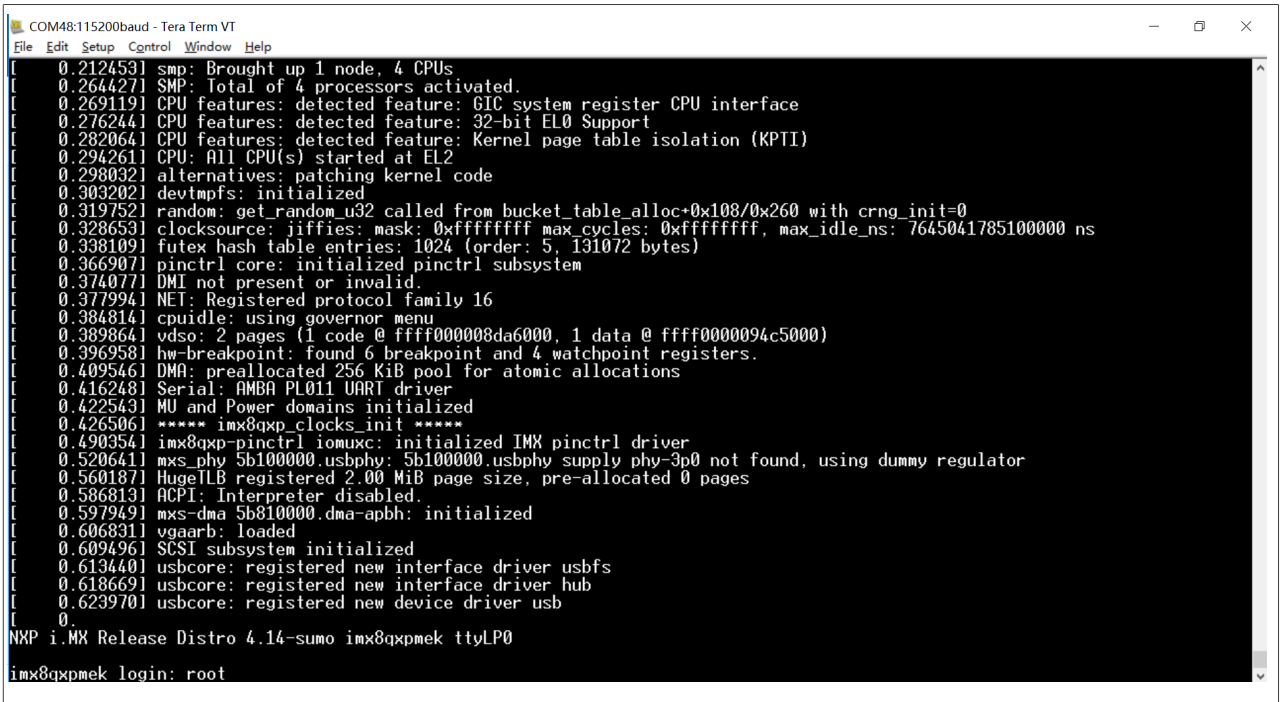

Figure 143. Root

3. boots up and log in （ When the board boots up, type root, as shown in Figure 143 ）: root
4. then, input below commands:

Note: *write the command and then connect the test fixture.*

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on
 > $i";done;
```

```
#For usb3.0 enter compliance mode/loopback mode.
/unit_tests/memtool 0x5b130490=0x0a000340
```

Note: *echo -1 > /sys/module/usbcore/parameters/autosuspend*
Disable USB bus enters suspend state
Note: *For i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on > $i";done;*
Disable USB runtime suspend, in that case, the controller, and PHY will not enter low-power mode, and we can visit the register even there is no device on the port.
Note: *(/unit_tests/memtool 0x5b130490=0x0a000340)*
Set Link is in the Compliance Mode State
Search PORTSC1USB3. Refer to Adjust USB3.0 to compliance mode registers--PORTSC1USB3（offset: 1_0490h）

8.3.1.2 Type C device mode

1. Power up board,
2. Boots up and login (When the board boots up, type root, as shown in Figure 4): root
3. Input below commands:

```
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on >
$i";done;
./configfs.sh
```

Note: *(./configfs.sh)*

Refer to Software Configuration to complete .configfs.sh.

8.3.1.3 Micro-AB host mode

1. Power up board,
2. Boots up and login: root

8.3.1.4 Micro-AB device mode

1. power up board,
2. boots up and login: root
3. then, input below commands:

```
./configfs.sh “” ci
```

8.3.2 Update image

8.3.2.1 Download the uuu tool and software

Download the uuu tool from https://github.com/NXPmicro/mfgtools/releases

You can find the released SW on the Official website.

For example,(8QM Linux)

From the official website https://www.nxp.com/, choose your selected product, then select “Software & tools”, find the Linux version for the board, select” Embedded Linux for i.MX Applications Processors”, and you can find the SW for your board.

The final link for 8QM Linux is https://www.nxp.com/webapp/sps/download/preDownload.jsp , you can find what you want here.

8.3.2.2 Burn release image into SD card

1. Dial code switch to Serial download mode, plug in Type C wire and serial port wire, open serial port.
2. Copy the two files: .sdcard and .bin file to mfgtools\uuu\Windows:

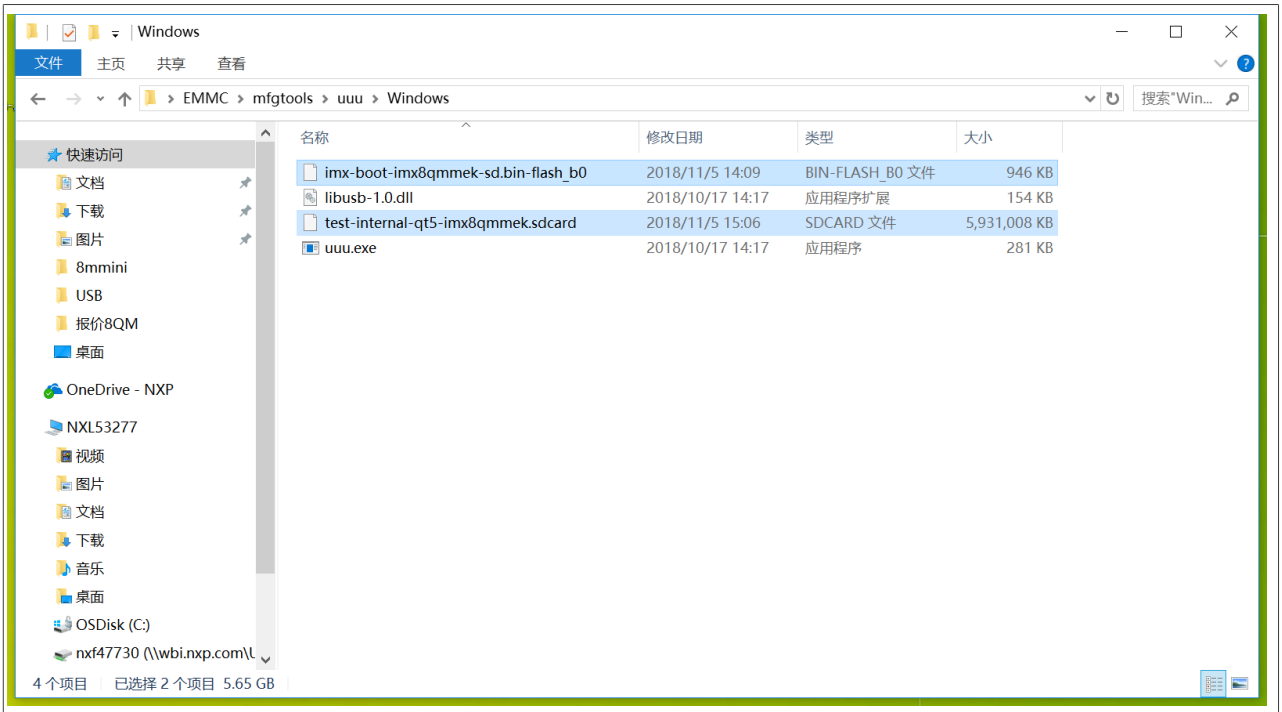

Figure 144. UUU Guide

3.
```
Open cmd, input:
c: cd C:\Users\nxf47730\Desktop\EMMC\mfgtools\uuu (The path is where the uuu
 tool at)
uuu      ////uuu user guide in command
uuu -b sd_all imx-boot-imx8qxpmek-sd.bin test-internal-qt5-imx8qxpmek.sdcard
```

4. Wait for the downloading over.

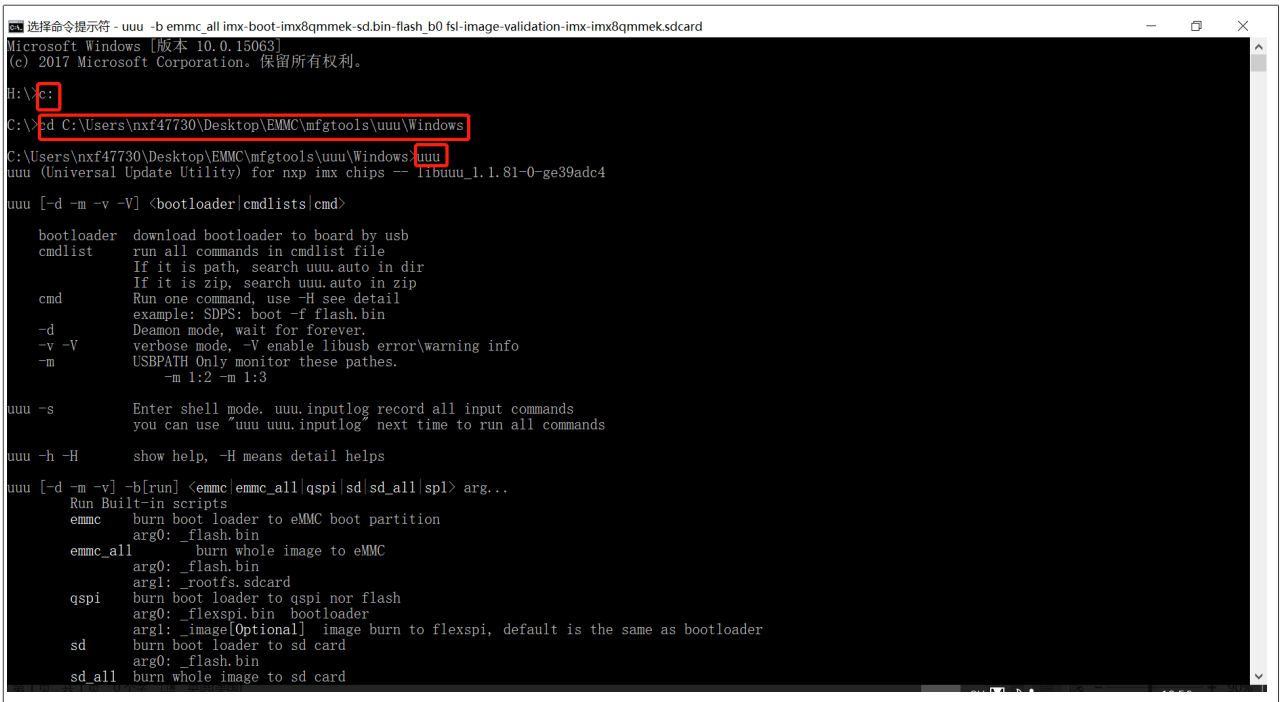

Figure 145. UUU Guide

8.3.3 Software configuration

1. After the board boots up, input the following commands:

```
nano configfs.sh
Example configfs.sh
if [ "$1" == "" ]; then
export FUNC="mass_storage"
else
export FUNC=$1
fi
#38100000.dwc3 for imx850D Synopsys USB3 IP
#gadget-cdns3 for imx8qm and imx8qxp Cadence USB3 IP
#ci_hdrc.0 for Legacy NXP USB2 IP
if [ "$2" == "" ]; then
export CONTROLLER="gadget-cdns3"
else
export CONTROLLER="ci_hdrc.0"
fi
if ! mount|grep -sq '/sys/kernel/config'; then
mount -t configfs none /sys/kernel/config
fi
cd /sys/kernel/config/usb_gadget
mkdir g1
cd g1
echo "0x1fc9" > idVendor
echo "0x0200" > idProduct
mkdir strings/0x409
echo "12345678ABCD" > strings/0x409/serialnumber
echo "NXP Semiconductors" > strings/0x409/manufacturer
echo "i.MX Reference Board" > strings/0x409/product
```

```
mkdir configs/c.1
mkdir functions/$FUNC".0"
ln -s functions/$FUNC".0" configs/c.1
if [ "$FUNC" == "mass_storage" ]; then
echo "/home/root/storage.img" > functions/mass_storage.0/lun.0/file
echo 1 > functions/mass_storage.0/lun.0/removable
echo 0xc0 > configs/c.1/bmAttributes
fi
if [ "$FUNC" == "ncm" ]; then
echo 10 > functions/ncm.0/qmult
fi
echo $CONTROLLER > /sys/kernel/config/usb_gadget/g1/UDC
```

2. Quit and save when finish typing. Input:

```
chmod +x configfs.sh
dd if=/dev/zero of=/home/root/storage.img bs=1M count=256
mkfs.vfat /home/root/storage.img
reboot
```

8.3.4 8QXP/8QM register

```
Type-C port base address: USB3_PHY3P0（5B16_0000）
                          USB3 (5B12_0000)
                          USB2PHY(5B19_8000)
Micro-AB port base address: USBOH_OTG(5B0D_0000)
Register address: base address+offset
```

8.3.4.1 Register to adjust the Type-C eye pattern--AFE_TX_REG1

Offset: 04h

```
#Read register data
/unit_tests/memtool 0x5b198004 1
# Write AFE_TX_REG1 register data
/unit_tests/memtool 0x5b198004=0x3f
```

Table 47. HS TX Amplitude Tune bits control Register

Register Name	Register Address (offset)	Register Bit	Description FastChar	Value
AFE_TX_REG1	0x 0004	<7:6>	UNUSED	00
		<5>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<4>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<3>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<2>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<1>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<0>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0

Table 47. HS TX Amplitude Tune bits control Register*...continued*

Register Name	Register Address (offset)	Register Bit	Description FastChar	Value
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
AFE_TX_REG12	0x 0030	<7:2>	UNUSED	000000
		<1>	HSTX DEEMP AMPLITUDE TRIM - TURN OFF	0
			HSTX DEEMP AMPLITUDE TRIM - TURN ON	1
		<0>	HSTX DEEMP AMPLITUDE CANNOT BE CONTROLLED BY ANALOG TEST BITS IN AFE_TX_REG1	0
			HSTX DEEMP AMPLITUDE CAN BE CONTROLLED BY ANALOG TEST BITS IN AFE_TX_REG1	1

Table 48. HS TX Slew Rate control Register

Register Name	Register Address	Register Bit	Description FastChar	Value
AFE_TX_REG5	0x00 14	<7>	Reserved	0
AFE_TX_REG5	0x00 14	<6:1>	HSTX Slew Rate control code	<000000> to <111111> 64 steps
AFE_TX_REG5	0x00 14	<0>	HSTX Slew control set to default code<111000>	0
			HSTX Slew control Set by control code AFE_TX_REG<6:1> value	1

For USBOTG2 (type C port) of imx8QXP/IMX8QM, the default disconnection threshold is 575 mv when AFE_RX_REG0[7:6] == 0. For customers who are using a cable or daughter card on this USB port, it is recommended to increase 35 mv by setting `AFE_RX_REG0[7:6]` to 2'b10 or 2'b01.

Table 49. Adjust the trip point for the disconnect detector

Register Name	Register Address	Register Bit	Description	Value
AFE_RX_REG0	0x5B198034	[7:6]	By default, the threshold is 575 mv	00
			Increase threshold by ~35 mv	01.10
			Increase threshold by ~70 mv	11

8.3.4.2 Register to adjust micro-AB eye pattern --USBPHY_TX /USBPHY_RX

```
#Offset:10h
/unit_tests/memtool 0x5b0d0010 1
#Write USBPHY_TX
/unit_tests/memtool 0x5b0d0010=0x10080803
```

Table 50. USBPHYx_TXn Register Settings

Name	USBPHYx_TXn															
Description	The USB PHY Transmitter Control Register handles the transmit controls.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
Field definitions	Reserved			Reserved			Reserved	Reserved	Reserved		TXEN CAL 45DP	Reserved	**TXCAL45DP**			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1

Table 50. USBPHYx_TXn Register Settings*...continued*

Name	USBPHYx_TXn					
Field definitions	Reserved	TXEN CAL 45DN	Reserved	**TXCAL45DM**	Reserved	**D_CAL**
Signal Names	**Description**					
TXCAL45 DP	Decode to trim the nominal 45 Ω series termination resistance to the USB_DP output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.					
TXCAL45 DM	Decode to trim the nominal 45 Ω series termination resistance to the USB_DM output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.					
D_CAL	Decode to trim the nominal 17.78 mA current source for the High-Speed TX drivers on USB_DP andUSB_DM. This current is directly proportional to the amplitude of the High-Speed TX eye diagram. 0000 Maximum current, approximately 19 % above nominal. 0111 Nominal 1111 Minimum current, approximately 19 % below nominal.					

Table 51. Table3-1. USBPHYx_RXn Register Setting

Name	USBPHYx_RXn															
Description	The USB PHY Receiver Control Register handles the receive controls.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved									RX_RXD BYPASS	Reserved					
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved									RX_DISCONADJ			reserved	RX_ENVADJ		
Signal Names	Description															
RX_ DIS CONADJ	Adjust threshold of disconnection detector 000 = Trip-Level Voltage is 0.57500 V 001 = Trip-Level Voltage is 0.55000 V 010 = Trip-Level Voltage is 0.58750 V 011 = Trip-Level Voltage is 0.60000 V 1XX = Reserved															

Note: *The default value is "000", "011" is recommended to get the maximum margin for the disconnection detection for customer with a long cable on USB controller.*

8.3.4.3 Registers that entry into USB2.0 test mode for MicroAB --USB_x_PORTSC1

```
#Offset:184h
memtool 0x5b0d0184 1
# Force to output Test Packet for Eye Diagram Test
memtool 0x5b0d0184=0x18441205
#Force to output J_STATE
memtool 0x5b0d0184=0x18411205
#Force to output K_STATE
memtool 0x5b0d0184=0x18421205
#Force to output SE0 (host) / NAK (device)
memtool 0x5b0d0184=0x18431205
# Force to output Reset
memtool 0x5b0d0184=0x18001305
#Force to output Suspend
memtool 0x5b0d0184=0x18001285
#Force to output Resume
memtool 0x5b0d0184=0x18001245
```

Table 52. USB_PORTSC1 field descriptions

Name	PORTSC1															
Description	Device Controller															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1		STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	PTC			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC		PO	PP	LS		HSP	PR	SUSP	FPR	OCC	OCA	PEC	PE	CSC	CCS
Signal Names	**Description**															
19–16 PTC	Port Test Control - Read/Write. Default = 0000b. Refer to Port Test Mode for the operational model for using these test modes and the USB Specification Revision 2.0, Chapter 7 for details on each test mode. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. NOTE: Low speed operations are not supported as a peripheral device. Any other value than zero indicates that the port is operating in test mode. Value Specific Test 0000 TEST_MODE_DISABLE 0001 J_STATE 0010 K_STATE 0011 SE0 (host) / NAK (device) 0100 Packet 0101 FORCE_ENABLE_HS 0110 FORCE_ENABLE_FS 0111 FORCE_ENABLE_LS 1000-1111 Reserved															

8.3.4.4 Registers that entry into USB2.0 test mode for TypeC

At uboot console:

```
setenv fdt_file fsl-imx8qxp-mek-host.dtb
boot
```

In kenel:

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo on >
$i";done;
```

Note: *For detailed settings, refer to Operation Steps*

.

```
#USB3:5B12_0000h
#PORTSC1USB2:1_0480h
/unit_tests/memtool 0x5b130480 1
/unit_tests/memtool 0x5b130480=0xa0
#PORTSC1USB3:1_0490h
/unit_tests/memtool 0x5b130490=0xa0
#USBCMD:1_0080h
/unit_tests/memtool 0x5b130080=0x804
#PORTPMSC1USB2:1_0484h
# enable Test mode
/unit_tests/memtool 0x5b130484=0x80000000
```

```
# Test Packet/ Test_J/ Test_K Mode/Test_Nek Mode
/unit_tests/memtool 0x5b130484=0x40000000
/unit_tests/memtool 0x5b130484=0x10000000
/unit_tests/memtool 0x5b130484=0x20000000
/unit_tests/memtool 0x5b130484=0x30000000
```

Table 53. PORTSC1USB2/ PORTSC1USB3 field descriptions

Name	PORTSC1USB2/ PORTSC1USB3															
Description	USB2/3 Port Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	WPR	DR	Reserved	Reserved	WOE	WOE	WOE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC		PortSpeed				PP	PLS				PR	OCA	Reserved	PED	CCS
Signal Names	Description															
9 PP	Port Power (PP), RWS. Default = '1'. This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report overcurrent conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it has reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. '0' = This port is in the Powered-off state. '1' = This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1'=on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port).															

Table 54. USBCMD field descriptions

Name	USBCMD															
Description	USB Command															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved															
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved				EU3S	EWE	CRS	CSC	LHCRST	Reserved			HSEE	INTE	HCRST	R_S
Signal Names	Description															
0 R_S	Run/Stop (R/S), RW. Default = '0'. '1' = Run. '0' = Stop. When set to a '1', the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. Refer to section 5.4.1.1 of xHCI specification for more information on how R/S shall be managed. The xHC shall halt within 16 ms after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (that is, HCH in the USBSTS register is '1'). Doing so may yield undefined results. Writing a '0' to this flag when the xHC is in the Running state (that is, HCH = '0') and any Event Rings are in the Event Ring Full state (refer to section 4.9.4 of xHCI specification) may result in lost events. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected VF. Refer to section 8 of xHCI specification for more information.															

Table 55. USBCMD field descriptions

Name	PORTPMSC1USB2															
Description	USB2 Port Power Management Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTC				Reserved											HLE
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 55. USBCMD field descriptions*...continued*

Field definitions	L1DS	BESL	RWE	L1S
Signal Names	**Description**			
9 **PP**	Port Test Control, RW. Default = '0'. When this field is '0', the port is NOT operating in a test mode. Anon-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encodings of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled 1: Test J_STATE 2: Test K_STATE 3: Test SE0_NAK 4: Test Packet 5: Test FORCE_ENABLE 6-14: Reserved. 15: Port Test Control Error.			

8.3.4.5 Adjust USB3.0 to compliance mode registers--PORTSC1USB3

```
#Offset: 1_0490h
/unit_tests/memtool 0x5b130490=0x0a000340
```

Table 56. PORTSC1USB3 field descriptions

Name	PORTSC1USB3															
Description	USB3 Port Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	WPR	DR	Reserved	Reserved	WOE	WOE	WOE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1
Field definitions	PIC		PortSpeed				PP	PLS				PR	OCA	Reserved	PED	CCS
Signal Names	**Description**															
8-5 **PLS**	Port Link State (PLS), RWS. Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Values: 0: The link shall transition to a U0 state from any of the U states. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: If the port is in the Disabled state (PLS = Disabled, PP = '1'), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1-2,4,6-15: Ignored. State Encoding: 0: Link is in the U0 State, 1: Link is in the U1 State, 2: Link is in the U2 State, 3: Link is in the U3 State (Device Suspended), 4: Link is in the Disabled State, 5: Link is in the RxDetect State, 6: Link is in the Inactive State, 7: Link is in the Polling State, 8: Link is in the Recovery State, 9: Link is in the Hot Reset State, 10: Link is in the Compliance Mode State, 11: Link is in the Test Mode State, 12-14: Reserved, 15: Link is in the Resume State. Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field. This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete. Refer to section 4.19 of xHCI specification for PLS transition conditions. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field															

8.4 i.MX 8M USB PHY Registers and Software Configurations

8.4.1 Operation steps

8.4.1.1 Type C port

8.4.1.1.1 USB3.0 Host mode

1. When the board boots up, press Enter, and then type: root.
2. Input below commands:
   a. RX Test
   Connect the test fixture, and then write the command.

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
echo "host" >>/sys/kernel/debug/38100000.dwc3/mode
/unit_tests/memtool -32 0x38100430=0x0A010340
```

   Note:
   - *Disable USB bus enters suspend state*
   - *Set Link is in the Compliance Mode State*
   - *Search PORTSC_30 at usb3_block_.guide (https://jira.sw.nxp.com/browse/MXEM-2?filter=27819&jql=project%20%3D%20MXEM) to find the register.*

   b. TX Test
   Write the command, and then connect the test fixture.

```
echo "host" >> /sys/kernel/debug/38100000.dwc3/mode
/unit_tests/memtool -32 0x38200430=0x0A010340
```

8.4.1.1.2 USB3.0 Device mode

1. Power up board,
2. Boots up and log in: root
3. Input below commands:

```
./configfs.sh
```

Note: *(./configfs.sh)*

Refer to Software Configuration to complete .configfs.sh.

8.4.1.1.3 USB2.0 Host mode

1.power up board

2.boots up and log in: root

8.4.1.1.4 USB2.0 Device mode

1. power up board,
2. boots up and log in: root
3. then, input below commands:

```
./configfs.sh
```

8.4.1.2 Type A port

8.4.1.2.1 USB3.0 Host mode

1. When the board boots up, press Enter, and then type: root.
2. Input below commands:
   a. RX Test
   Connect the test fixture, and then write the command.

```
echo -1 > /sys/module/usbcore/parameters/autosuspend
echo "host" >>/sys/kernel/debug/38100000.dwc3/mode
/unit_tests/memtool -32 0x38100430=0x0A010340
```

   Note:
   - *Disable USB bus enters suspend state*
   - *Set Link is in the Compliance Mode State*
   - *Search PORTSC_30 at usb3_block_.guide (https://jira.sw.nxp.com/browse/MXEM-2?filter=27819&jql=project%20%3D%20MXEM) to find the register.*

   b. TX Test
   Write the command, and then connect the test fixture.

```
echo "host" >> /sys/kernel/debug/38100000.dwc3/mode
/unit_tests/memtool -32 0x38200430=0x0A010340
```

8.4.1.2.2 USB3.0 Device mode

1. Power up board,
2. Boots up and log in: root
3. Input below commands:

```
./configfs.sh
```

Note: *(./configfs.sh)*

Refer to Software Configuration to complete .configfs.sh.

8.4.1.2.3 USB2.0 Host mode

1.power up board

2.boots up and log in: root

8.4.1.2.4 USB2.0 Device mode

1. power up board,
2. boots up and log in: root
3. then, input below commands:

```
./configfs.sh
```

8.4.2 Update image

8.4.2.1 Download the uuu tool and SW

1. Dial code switch to Serial Download mode, plug in Type C wire and serial port wire, open serial port.

2. Copy the two files: .sdcard and .bin file to mfgtools\uuu\Windows:

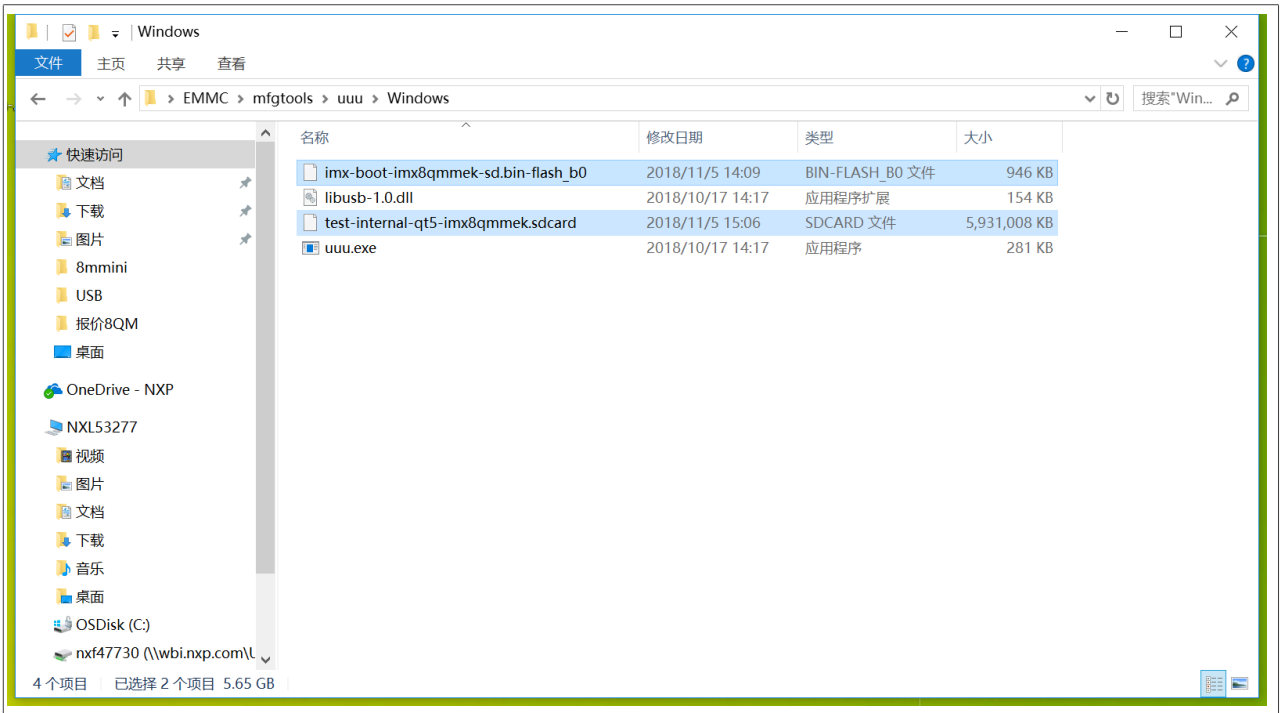

Figure 146. UUU Guide

3. 5. Open cmd, input

```
c:
cd C:\Users\nxf47730\Desktop\EMMC\mfgtools\uuu (The path is where the uuu
 tool at)
uuu      ////uuu user guide in command
uuu -b sd_all imx-boot-imx8qxpmek-sd.bin test-internal-qt5-imx8qxpmek.sdcard
```

4. Wait for the downloading over.

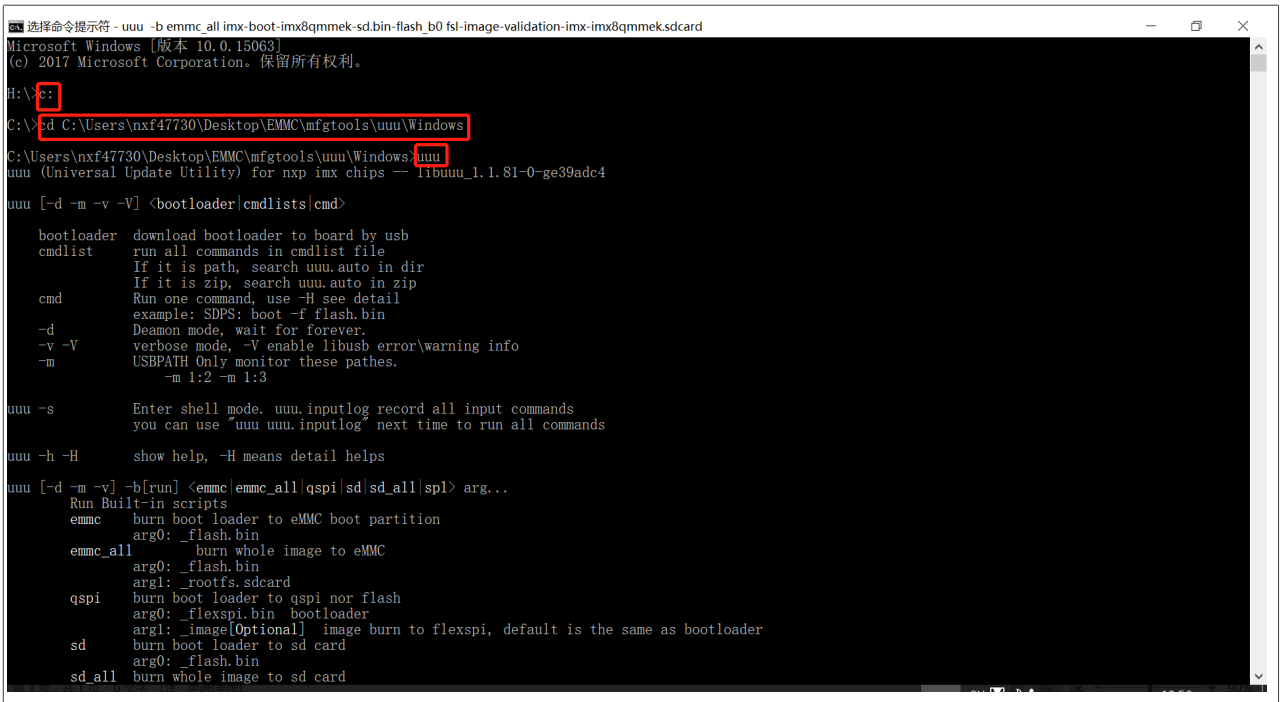

Figure 147. UUU Guide

8.4.3 Software configuration

1. After the board boots up, input the following commands:

```
nano configfs.sh
Example: .configfs.sh
if [ "$1" == "" ]; then
export FUNC="mass_storage"
else
export FUNC=$1
fi
#38100000.dwc3 for imx850D Synopsys USB3 IP
#gadget-cdns3 for imx8qm and imx8qxp Cadence USB3 IP
#ci_hdrc.0 for Legacy NXP USB2 IP
if [ "$2" == "" ]; then
export CONTROLLER="38100000.dwc3"
else
export CONTROLLER="ci_hdrc.0"
fi
if ! mount|grep -sq '/sys/kernel/config'; then
mount -t configfs none /sys/kernel/config
fi
cd /sys/kernel/config/usb_gadget
mkdir g1
cd g1
echo "0x1fc9" > idVendor
echo "0x0200" > idProduct
mkdir strings/0x409
echo "12345678ABCD" > strings/0x409/serialnumber
echo "NXP Semiconductors" > strings/0x409/manufacturer
echo "i.MX Reference Board" > strings/0x409/product
mkdir configs/c.1
```

```
mkdir functions/$FUNC".0"
ln -s functions/$FUNC".0" configs/c.1
if [ "$FUNC" == "mass_storage" ]; then
echo "/home/root/storage.img" > functions/mass_storage.0/lun.0/file
echo 1 > functions/mass_storage.0/lun.0/removable
echo 0xc0 > configs/c.1/bmAttributes
fi
if [ "$FUNC" == "ncm" ]; then
echo 10 > functions/ncm.0/qmult
fi
echo $CONTROLLER > /sys/kernel/config/usb_gadget/g1/UDC
```

2. Quit and save when I finish typing. Then to input:

```
chmod +x configfs.sh
dd if=/dev/zero of=/home/root/storage.img bs=1M count=256
mkfs.vfat /home/root/storage.img
reboot
```

8.4.4 8M register

Type-C port base address: 3810_0000h

Type-A port base address： 3820_0000h

Register address： base address+offset

8.4.4.1 Registers that entry into USB2.0 test eye diagram mode for Type A -- PORTPMSC_20

```
#offset:420h
# Test Packet/ Test_J/ Test_K/ Test SE0_NAK Mode
/unit_tests/memtool 0x38200424=0x40000000 // Force to output Test Packet for Eye
 Diagram Test
/unit_tests/memtool 0x38200424=0x10000000 //Force to output J_STATE
/unit_tests/memtool 0x38200424=0x20000000 //Force to output K_STATE
/unit_tests/memtool 0x38200424=0x30000000//Force to output SE0 (host) / NAK
 (device)
```

Table 57. PORTPMSC_20 field descriptions

Name	PORTPMSC_20															
Description	USB2 Port Power Management Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	u	u	u	u	0	0	0	0	0	0	0	0	0	0	0	u
Field definitions	PRTTSTCTRL				Reserved_27 _17											HLE
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u
Field definitions	L1DSLOT								HIRD				RWE	L1S		
Signal Names	**Description**															
PRTTST CTRL	Port Test Control, RW. Default = '0'. When this field is '0', the port is NOT operating in a test mode. Anon-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encodings of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled 1: Test J_STATE 2: Test K_STATE 3: Test SE0_NAK 4: Test Packet															

Table 57. PORTPMSC_20 field descriptions*...continued*

Name	PORTPMSC_20
	5: Test FORCE_ENABLE 6-14: Reserved. 15: Port Test Control Error.

8.4.4.2 Register to adjust the Type-A eye pattern-- PHY_CTL3_ADDR

```
Offset: 0x4Ch
Base Address for GLUE registers Type-A port base address -382F0000
/unit_tests/memtool 0x382F004C 1                // Read register data
/unit_tests/memtool 0x382F004C =94DCE6E4        // Write PHY_CTL3_ADDR register
 data
```

Table 58. PHY_CTL3_ADDR register

Name	PHY_CTL3_ADDR															
Description	USB3.0 PHY Status bits Register															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0
Field definitions	tx_vboost_lvl			ios_bias			TXREFTUNE0				TXRISETUNE0		TXRESTUNE0		TXP REEM PULSET UNE0	TXP REEM PMPT UNE0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0
Field definitions	TXP REEM PMP TUN E0E0	TXSHXSTUNE0		TXFSLSTUNE0			SQRXTUNE0				OTGTUNE0			COMPIDISTUNE		
Parameter Controls	**TXPREEMPULSETUNE0:** HS Transmitter Pre-Emphasis Duration Control Function: This signal controls the duration for which the HS pre-emphasis current is sourced onto DP<#> or DM<#>. The HS Transmitter pre-emphasis duration is defined in terms of unit amounts. One unit of pre-emphasis duration is approximately 580 ps and is defined as 1X pre-emphasis duration. This signal is valid only if either TXPREEMPAMPTUNE<#>[1] or TXPREEMPAMPTUNE<#>[0] is set to 1'b1. • 1: 1X, short pre-emphasis current duration • 0: 2X (design default), long pre-emphasis current duration If TXPREEMPPULSETUNE<#> is not used, set it to 1'b0. **TXRESTUNE0:** USB Source Impedance Adjustment Function: Some applications require additional devices to be added on the USB, such as a series switch, which can add significant series resistance. This bus adjusts the driver source impedance to compensate for added series resistance on the USB. • 11: Source impedance is decreased by approximately 4 Ω. • 10: Source impedance is decreased by approximately 2 Ω. • 01: Design default • 00: Source impedance is increased by approximately 1.5 Ω. Note: Any setting other than the default can result in source impedance variation across process, voltage, and temperature conditions that does not meet USB 2.0 specification limits. If this bus is not used, leave it at the default setting. **TXRISETUNE0**: HS Transmitter Rise/Fall Time Adjustment Function: Adjusts the rise/fall times of the high-speed waveform. To enable tuning at the board level, connect this bit to a register. Note: A positive binary bit setting change results in a –4 % incremental change in the HS rise/fall time. A negative binary bit setting change results in a +4 % incremental change in the HS rise/fall time.															

8.4.4.3 Registers that entry into USB2.0 test mode for Type C

```
# Test Packet/ Test_J/ Test_K/ Test SE0_NAK Mode
/unit_tests/memtool 0x38100424=0x40000000 // Force to output Test Packet for Eye
 Diagram Test
/unit_tests/memtool 0x38100424=0x10000000 //Force to output J_STATE
/unit_tests/memtool 0x38100424=0x20000000 //Force to output K_STATE
/unit_tests/memtool 0x38100424=0x30000000//Force to output SE0 (host) / NAK
 (device)
```

Table 59. PORTPMSC_20 field descriptions

Name	PORTPMSC_20															
Description	USB2 Port Power Management Status and Control															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Table 59. PORTPMSC_20 field descriptions*...continued*

Name	PORTPMSC_20															
Reset value	u	u	u	u	0	0	0	0	0	0	0	0	0	0	0	u
Field definitions	PRTTSTCTRL				Reserved_27 _17											HLE
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u
Field definitions	L1DSLOT								HIRD				RWE	L1S		
Signal Names	**Description**															
PRTTST CTRL	Port Test Control, RW. Default = '0'. When this field is '0', the port is NOT operating in a test mode. Anon-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 for the operational model for using these test modes. The encodings of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled 1: Test J_STATE 2: Test K_STATE 3: Test SE0_NAK 4: Test Packet 5: Test FORCE_ENABLE 6-14: Reserved. 15: Port Test Control Error.															

8.4.4.4 Register to adjust the Type C eye pattern-- PHY_CTL3_ADDR

```
#Offset: 0x4Ch
#Base Address for GLUE registers Type-C port base address:381F0000
/unit_tests/memtool 0x381F004C 1                // Read register data
/unit_tests/memtool 0x381F004C =94D4E464          //Write PHY_CTL3_ADDR register
 data
```

Table 60. PHY_CTL3_ADDR register

Name	PHY_CTL3_ADDR															
Description	USB3.0 PHY Status bits Register															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	1	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0
Field definitions	tx_vboost_lvl			ios_bias			TXREFTUNE0				TXRISETUNE0		TXRESTUNE0		TXP REEM PULSET UNE0	TXP REEM PMPT UNE0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0
Field definitions	TXP REEM PMPT UNE0E0	TXSHXSTUNE0		TXFSLSTUNE0				SQRXTUNE0			OTGTUNE0			COMPIDISTUNE		
Parameter Controls	**TXPREEMPULSETUNE0:** HS Transmitter Pre-Emphasis Duration Control Function: This signal controls the duration for which the HS pre-emphasis current is sourced onto DP<#> or DM<#>. The HS Transmitter pre-emphasis duration is defined in terms of unit amounts. One unit of pre-emphasis duration is approximately 580 ps and is defined as 1X pre-emphasis duration. This signal is valid only if either TXPREEMPAMPTUNE<#>[1] or TXPREEMPAMPTUNE<#>[0] is set to 1'b1. • 1: 1X, short pre-emphasis current duration • 0: 2X (design default), long pre-emphasis current duration If TXPREEMPPULSETUNE<#> is not used, set it to 1'b0. **TXRESTUNE0:** USB Source Impedance Adjustment Function: Some applications require additional devices to be added on the USB, such as a series switch, which can add significant series resistance. This bus adjusts the driver source impedance to compensate for added series resistance on the USB. • 11: Source impedance is decreased by approximately 4 Ω. • 10: Source impedance is decreased by approximately 2 Ω. • 01: Design default • 00: Source impedance is increased by approximately 1.5 Ω. Note: Any setting other than the default can result in source impedance variation across process, voltage, and temperature conditions that does not meet USB 2.0 specification limits. If this bus is not used, leave it at the default setting. **TXRISETUNE0**: HS Transmitter Rise/Fall Time Adjustment Function: Adjusts the rise/fall times of the high-speed waveform. To enable tuning at the board level, connect this bit to a register. Note: A positive binary bit setting change results in a –4 % incremental change in the HS rise/fall time. A negative binary bit setting change results in a +4 % incremental change in the HS rise/fall time.															

8.4.4.5 Adjust USB3.0 to compliance mode registers--PORTSC_30

```
#Offset: 430h
/unit_tests/memtool -32 0x38200430=0x0A010340
```

Table 61. PORTSC_30 field descriptions

Name	PORTSC_30															
Description	Port Status and Control Register Bit Definitions The PORTSC Register															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	u	u	0	0	u	u	u	0	u	u	u	u	u	u	u	u
Field definitions	WPR	DR	Reserved	Reserved	WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	u	u	u	u	u	u	1	0	1	0	1	0	0	1	u	0
Field definitions	PIC		PortSpeed				PP	PLS				PR	OCA	Reserved	PED	CCS
Signal Names	**Description**															
8-5 PLS	Port Link State (PLS), RWS. Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Values: 0: The link shall transition to a U0 state from any of the U states. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: If the port is in the Disabled state (PLS = Disabled, PP = '1'), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 1-2,4,6-15: Ignored. State Encoding: 0: Link is in the U0 State, 1: Link is in the U1 State, 2: Link is in the U2 State, 3: Link is in the U3 State (Device Suspended), 4: Link is in the Disabled State, 5: Link is in the RxDetect State, 6: Link is in the Inactive State, 7: Link is in the Polling State, 8: Link is in the Recovery State, 9: Link is in the Hot Reset State, 10: Link is in the Compliance Mode State, 11: Link is in the Test Mode State, 12-14: Reserved, 15: Link is in the Resume State. Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field. This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete. Refer to section 4.19 of xHCI specification for PLS transition conditions. Refer to sections 4.15.2 and 4.23.5 for more information on the use of this field															

8.5 i.MX 8MM USB PHY registers and software configurations

The test board has routed out two USB-Type C Ports, The register base address： Base 0x32e40000 + 230h offset, Base 0x32e50000 + 230h offset.

8.5.1 USB OTG PHY configuration register 1(USBNC_n_PHY_CFG1)

Most of these signals are used for parametric tuning of the USB transceiver functions.

Table 62. USBNC_n_PHY_CFG1 field descriptions

Name	USBNC_n_PHY_CFG1															
Description	The USB_OTGx_PHY_CFG1 register allows control of selected inputs to the USB OTG PHY.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	1	0	1	0	0	1	1	0	0	1	1
Field definitions	CHRG DET _ Megamix	TXPRE EMPPUL SET UNE0	TXPRE EMPAMPT UNE0		TXRESTUNE0		TXRISETUNE0		TXVREFTUNE0				TXFSLSTUNE0			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	1	1	1	0	0	0	1	1	1	0	0	1	0	1	1
Field definitions	--	TXHSXVTUNE0		OTGTUNE0			SQRXTUNE0			COMPDISTUNE0			FSEL			COMMON ONN
Signal Names	**Description**															
25–24 TXRI SET UNE0	HS Transmitter Rise/Fall Time Adjustment This bus adjusts the rise/fall times of the high-speed transmitter waveform. 00 -10 % 01 Design default															

Table 62. USBNC_n_PHY_CFG1 field descriptions*...continued*

Name	USBNC_n_PHY_CFG1
	10 +15 % 11 +20 %
23–20 TXV REFTUNE0	HS DC Voltage Level Adjustment This bus adjusts the high-speed transmitter DC level voltage. 0000 -6 % 0001 -4 % 0010 -2 % 0011 Design default 0100 +2 % 0101 +4 % 0110 +6 % 0111 +8 % 1000 +10 % 1001 +12 % 1010 +14 % 1011 +16 % 1100 +18 % 1101 +20 % 1110 +22 % 1111 +24 %

8.5.2 Registers that entry into USB2.0 eye diagram test mode for Type C -- USBx_nPORTSC1

```
#Offset: 184h
#Register address: 32E4_0000h base + 184h offset = 32E4_0184h（TypeC1）
                            32E5_0000h base + 184h offset = 32E5_0184h（TypeC2）
# Test Packet/ Test_J/ Test_K/ Test SE0_NAK Mode
/unit_tests/memtool 0x32E40184=0x10040000 // Force to output Test Packet for Eye
 Diagram Test
/unit_tests/memtool 0x32E40184=0x10010000 //Force to output J_STATE
/unit_tests/memtool 0x32E40184=0x10020000 //Force to output K_STATE
/unit_tests/memtool 0x32E40184=0x10030000//Force to output SE0 (host) / NAK
 (device)
```

Table 63. USBx_nPORTSC1 field descriptions

Name	USBx_nPORTSC1															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1		STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	PTC			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PIC		PO	PP	LS		HSP	PR	SUSP	FPR	OCC	0CA	PEC	PE	CSC	CCS

Signal Names	Description
PTC	Port Test Control - Read/Write. Default = 0000b. The FORCE_ENABLE_FS and FORCE ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values will force the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE will allow the port state machines to progress normally from that point. NOTE: Low speed operations are not supported as a peripheral device. Any other value than zero indicates that the port is operating in test mode. Value Specific Test 0000 TEST_MODE_DISABLE 0001 J_STATE 0010 K_STATE 0011 SE0 (host) / NAK (device) 0100 Packet 0101 FORCE_ENABLE_HS 0110 FORCE_ENABLE_FS 0111 FORCE_ENABLE_LS 1000-1111 Reserved

8.5.3 Other useful commands and scripts

1. Change u-boot bootargs for USB Certification (optional) We may need to load USB certification dtb

```
setenv fdt_file_usb_certi imx6ul-14x14-evk-usb-certi.dtb
setenv loadfdt_usb_certi 'fatload mmc ${mmcdev}:${mmcpart} ${fdt_addr}
${fdt_file_usb_certi}'
setenv usb_certi_boot 'run mmcargs;run loadimage; run loadfdt_usb_certi;bootz
 ${loadaddr} -
${fdt_addr};'
setenv bootcmd run usb_certi_boot
save
boot /* boot the board */
```

Note: *The above command changes dtb file name for USB certification. To use normal MMC board again, the user may need to run below command at u-boot:*

```
setenv mmcboot 'run mmcargs; run loadimage;run loadfdt;bootz ${loadaddr} -
 ${fdt_addr};'
save
run mmcboot
```

2. For peripheral only or otg peripheral certification test

```
dd if=/dev/zero of=/home/root/storage.img bs=1M count=256
mkfs.vfat /home/root/storage.img
/home/root/configfs.sh
```

The user can also add above operation to initialization script:

```
vi /etc/rc.local
add "/home/root/configfs.sh" before "exit 0"
```

3. Other Software Configurations (optional)
   Below configurations may be needed during certification test.
   a. Enable USB wake-up
      USB wake-up (as system wake-up source) is not enabled by default, so after plugging in the USB device, the user must enable USB wake-up using below script.

```
for i in $(find /sys -name wakeup | grep usb);do echo enabled > $i;echo
 "echo enabled >
$i";done;
echo enabled > /sys/bus/platform/devices/5b110000.cdns3/power/wakeup
```

   b. Let the system enter suspend (standby) mode
      For standard Linux BSP, the user can use below commands:

```
echo mem > /sys/power/state
```

   c. Operations for creating wake-up event
      Remote wake-up, disconnect and connect event will trigger wake-up event to let the system leave suspend (standby) mode.
      Note: *imx850D does not support USB wake-up from system suspend.*
   d. Disable runtime power management

```
for i in $(find /sys -name control | grep usb);do echo on > $i;echo "echo
 on > $i";done;
```

   e. Set another wake-up source for suspend mode
      Below is the example to wake up from console.

```
echo enabled > /sys/class/tty/ttymxc0/power/wakeup
```

```
Or
echo enabled > /sys/class/tty/ttyLP0/power/wakeup
```

8.6 i.MX 8DXL USB PHY registers and software configuration

The test board has routed out two USB ports: two Type C ports named USB-OTG1 and USB-OTG2.

8.6.1 Hardware configuration

As shown in the figure, the power supply of the board is connected, the debug port is connected to the computer with a serial cable, and the serial port is opened (set the serial port baud rate to 115200)

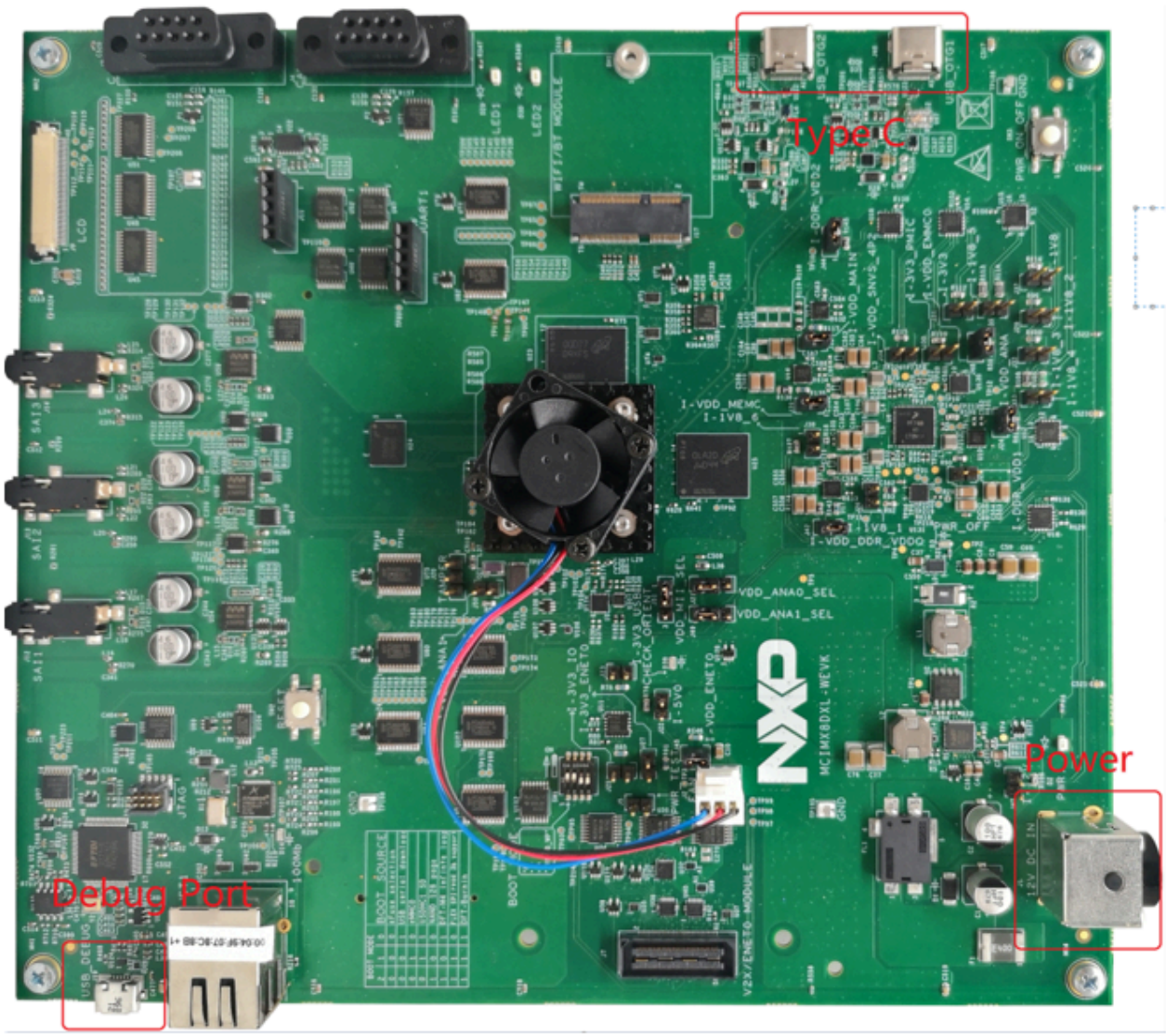

Figure 148. Hardware configuration

8.6.2 Software configuration

There are several steps to follow to adjust the software configuration:

1. Update the image
2. Download the uuu tool and software.
   a. Download the uuu tool from github.
   b. On the official NXP website, choose the selected product.
   c. Select “Software and tools” and find the Linux version for the board.
   d. Select” Embedded Linux for i.MX Applications Processors” and find the SW for your board.
3. Burn the release image into the SD card.
   a. Bootmode switch to Serial download mode.
   b. Plug in the Type C cable and the serial port cable.
   c. Open the serial port tool.
   d. Copy the two files: `.rootfs.wic` and `.bin-flash` to the same directory, as shown in the figure below.

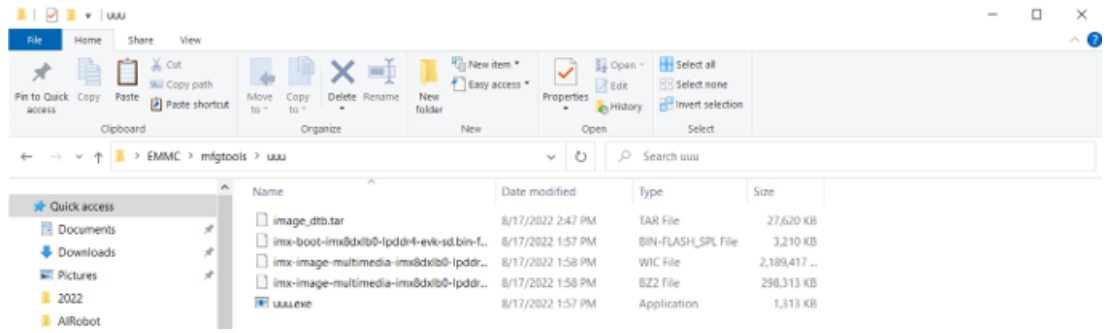

Figure 149. Copying files to the directory

   e. open cmd and input:

```
 cd C:\Users\nxfxxxxx\Desktop\EMMC\mfgtools\uuu
 uuu
 uuu -b sd_all imx-boot-imx8dxlb0-lpddr4-evk-sd.bin-flash_spl imx-image-
multimedia-imx8dxlb0-lpddr4-evk-20220428145028.rootfs.wic
```

   f. After the download is finished, power off the board and set the bootmode into SD card mode.
4. Adjusting the software configuration
   a. Power up the board and log in
      i. Enter the following command to create the `.sh` script file:

```
$ vi configfs.sh
```

      ii. Enter the interface as shown in the Figure 150:

Figure 150. The interface

b. Copy the following script into the `sh` script:

Note: *The lines preceded by the "#" character are comments and have no effect.*

```
#!/bin/sh
dd if=/dev/zero of=/home/root/storage.img bs=1M count=64
mkfs.vfat /home/root//storage.img
if [ "$1" == "" ]; then
export FUNC="mass_storage"
else
export FUNC=$1
fi
#38100000.dwc3 for imx850D Synopsys USB3 IP
#5b110000.usb3 for imx8qm and imx8qxp Cadence USB3 IP
#ci_hdrc.0 for Legacy NXP USB2 IP
if [ "$2" == "" ]; then
export CONTROLLER="ci_hdrc.0"
else
export CONTROLLER="ci_hdrc.1"
fi
if ! mount|grep -sq '/sys/kernel/config'; then
mount -t configfs none /sys/kernel/config
fi
cd /sys/kernel/config/usb_gadget
mkdir g1
cd g1
echo "0x1fc9" > idVendor
echo "0x0129" > idProduct
```

```
mkdir strings/0x409
echo "12345678ABCD" > strings/0x409/serialnumber
echo "NXP Semiconductors" > strings/0x409/manufacturer
echo "i.MX Reference Board" > strings/0x409/product
mkdir configs/c.1
mkdir functions/$FUNC".0"
ln -s functions/$FUNC".0" configs/c.1
if [ "$FUNC" == "mass_storage" ]; then
echo "/home/root/storage.img" > functions/mass_storage.0/lun.0/file
echo 1 > functions/mass_storage.0/lun.0/removable
echo 0xc0 > configs/c.1/bmAttributes
fi
if [ "$FUNC" == "ncm" ]; then
echo 10 > functions/ncm.0/qmult
fi
echo $CONTROLLER > /sys/kernel/config/usb_gadget/g1/UDC
```

c. To save the script, type `:wq` after pressing **esc.**

d. Enter the following commands in order:

```
$ chmod +x configfs.sh
$ dd if=/dev/zero of=/home/root/storage.img bs=1M count=64

$ mkfs.vfat /home/root//storage.img
```

e. To check that the process goes properly, enter the command `$:`

```
root@imx8dxlb0-lpddr4-evk:~# ls
configfs.sh g_mass_storage.ko g_zero.ko storage.img testusb1.sh
 testusb2.sh
```

When `configfs.sh` and `storage.img` appear, the configuration is successful.

8.6.3 Operation steps

8.6.3.1 USB OTG1 device mode

1. Power up the board.
2. Boot up or log in. After the board is booted, enter root, as shown in Figure 151:

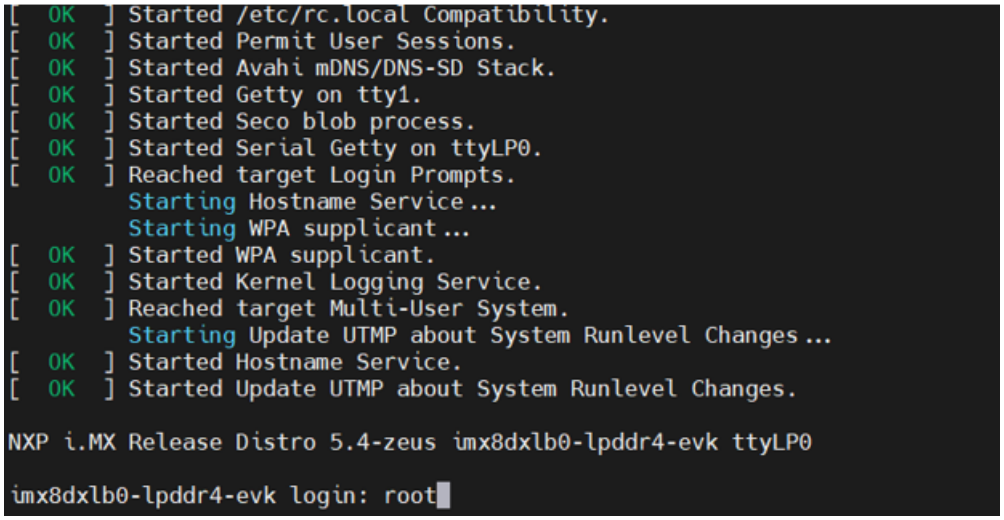

Figure 151. entering "root"

3. Enter the following command:

```
$./configfs.sh
```

8.6.3.2 USB OTG2 device mode

1. Power up the board.
2. Boot up or log in.
3. Enter the following command:

```
$./configfs.sh '' ci
```

8.6.3.3 USB OTG1 host mode

1. Power up the board.
2. Boot up or log in.

8.6.3.4 USB OTG2 host mode

1. Power up the board.
2. Boot up or log in.

8.6.4 8DXL register

```
USB2_PHY1 base address: 5B10_0000h
USB2_PHY2 base address: 5B11_0000h
USBO2(USB_OTG1)port base address: 5B0D_0000h
USBO2(USB_OTG2)port base address: 5B0E_0000h
Register address: base address+offset
```

8.6.4.1 Register to adjust USB 2.0 eye pattern --USBPHY_TX /USBPHY_RX

```
#Offset:10h
$/unit_tests/memtool 0x5b100010 1
#Write USBPHY_TX
$/unit_tests/memtool 0x5b100010=0x10080802
```

USB2_PHY1 base address: 5B10_0000h

USB2_PHY2 base address: 5B11_0000h

Register address: base address+offset.

Table 64. USBPHYx_TXn register settings

Name	USBPHYx_TXn															
Description	The USB PHY Transmitter Control Register handles the transmit controls.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Field definitions	Reserved			Reserved			Reserved	Reserved	Reserved		TXENCAL45DP	Reserved	TXCAL45DP			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
Field definitions	Reserved		TXENCAL45DM	Reserved	TXCAL45DM				Reserved				D_CAL			
Signal Names	Description															
TXCAL 45DP	Decode to trim the nominal 45 Ω series termination resistance to the USB_DP output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.															
TXCAL 45DM	Decode to trim the nominal 45 Ω series termination resistance to the USB_DM output pin. Maximum resistance = 0000. Resistance is centered by design at 1000. Trimming this resistance impacts both the overshoot/undershoot of the Full Speed TX output and the amplitude of the High-Speed TX output.															
D_CAL	Decode to trim the nominal 17.78 mA current source for the High-Speed TX drivers on USB_DP and USB_DM. This current is directly proportional to the amplitude of the High-Speed TX eye diagram. 0000 Maximum current, approximately 19 % above nominal. 0111 Nominal 1111 Minimum current, approximately 19 % below nominal.															

#Offset:20h

USB2_PHY1 base address: 5B10_0000h

USB2_PHY2 base address: 5B11_0000h

Register address: base address+offset

Table 65. USBPHYx_RXn register setting

Name	USBPHYx_RXn															
Description	The USB PHY Receiver Control Register handles the receive controls.															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved									RXDBYPASS	Reserved					
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	Reserved									DISCONADJ			Reserved	ENVADJ		
Signal Names	Description															
RX_ DIS CO NAD J	The DISCONADJ field adjusts the trip point for the disconnect detector. 000 Trip-Level Voltage is 0.56875 V															

Table 65. USBPHYx_RXn register setting*...continued*

Name	USBPHYx_RXn
	001 Trip-Level Voltage is 0.55000 V 010 Trip-Level Voltage is 0.58125 V 011 Trip-Level Voltage is 0.60000 V 1XX Reserved

8.6.4.2 Registers that entry into USB2.0 test mode-PORTSC1

```
#Offset:184h

USB OTG1 port base address: 5B0D_0000h

USB OTG2 port base address: 5B0E_0000h

Register address: base address+offset
```

```
$/unit_tests/memtool 0x5b0d0184 1
#Force to output Test Packet for Eye Diagram Test
$/unit_tests/memtool 0x5b0d0184=0x18041205
#Force to output J_STATE
$/unit_tests/memtool 0x5b0d0184=0x18011205
#Force to output K_STATE
$/unit_tests/memtool 0x5b0d0184=0x18021205
#Force to output SE0 (host) / NAK (device)
$/unit_tests/memtool 0x5b0d0184=0x18031205
```

Table 66. USB_PORTSC1 field descriptions

Name	PORTSC1															
Description	Device controller															
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PTS_1		STS	PTW	PSPD		PTS_2	PFSC	PHCD	WKOC	WKDC	WKCN	PTC			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field definitions	PIC		PO	PP	LS		HSP	PR	SUSP	FPR	OCC	OCA	PEC	PE	CSC	CCS
Signal Names	Description															
19–16 PTC	Port Test Control - read/write. Default = 0000b. Refer to Port Test Mode for the operational model for using these test modes and the USB Specification Revision 2.0, Chapter 7 for details on each test mode. The FORCE_ENABLE_FS and FORCE_ENABLE_LS are extensions to the test mode support specified in the EHCI specification. Writing the PTC field to any of the FORCE_ENABLE_{HS/FS/LS} values forces the port into the connected and enabled state at the selected speed. Writing the PTC field back to TEST_MODE_DISABLE allows the port state machines to progress normally from that point. ***Note:*** *Low-speed operations are not supported as a peripheral device.* Any other value than zero indicates that the port is operating in test mode. Value Specific Test 0000b TEST_MODE_DISABLE 0001b J_STATE 0010b K_STATE 0011b SE0 (host) / NAK (device) 0100b Packet 1000b-1111b Reserved																

8.7 Other i.MX 8 Serials USB PHY Registers and Software Configurations

TBD

9 Useful links

1. Freescale I.MX6 USB Certification Test Guide and Materials:
   https://community.freescale.com/docs/DOC-94923
2. USB Spec:
   https://www.usb.org/document-library/electrical-compliance-test-specification-superspeed-usb-10-gbps-rev-10
3. OTG and Embedded Host related documents:
   http://www.usb.org/developers/onthego/
4. OTG and Embedded Host Compliance Test Spec:
   http://www.usb.org/developers/onthego/otgeh_compliance_plan_1_2.pdf
5. Full and Low Speed Compliance Test Spec:
   https://www.usb.org/document-library/usb-20-electrical-test-specification
6. USB 2.0 Electrical Test Spec:
   https://www.usb.org/developers/compliance/USB-IF_USB_2_0_Electrical_Test_Spec081005.pdf
7. Gold Tree Test procedure:
   https://compliance.usb.org/resources/GoldSuite%20Test%20Procedure.pdf
8. Test software and tools:
   http://www.usb.org/developers/tools/
9. Checklist and TPL:
   http://www.usb.org/developers/compliance/check_list/
   http://www.usb.org/developers/compliance/check_list/TPL_form_otgeh2_0_v1.0_-_fill-in.pdfhttp://www.usb.org/developers/compliance/check_list/TPL_form_otgeh2_0_v1.0_-_fill-in.pdf
10. Electrical Test procedure for different Oscilloscopes:
    http://www.usb.org/developers/compliance/electrical_tests/
11. Detailed Electrical Test procedure for Keysight Oscilloscope with N5416A:
    http://www.keysight.com/upload/cmc_upload/All/N5416A_USB2_Compliance_App_Testing_Notes.pdf
12. USB-IF Compliance Updates:
    http://compliance.usb.org/index.asp?UpdateFile=Electrical&Format=Standardh
13. Search the TID for certified products:
    http://www.usb.org/kcompliance/view
14. Company VID List:
    http://www.usb.org/developers/tools/comp_dump
15. USB-PET User Manual:
    http://www.mqp.com/pdf/manuals/PET%20User%20Manual.pdf
16. USB-PET Software:
    http://www.mqp.com/dnld.htmh
17. Independent Test Labs
    http://www.usb.org/developers/compliance/labs/
18. i.MX 8 Series Applications Processors Materials:
    https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applications-processors/i.mx-8-processors:IMX8-SERIES
19. i.MX 7 Series Applications Processors Materials:
    https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applications-processors/i.mx-7-processors:IMX7-SERIES

20. USB 3.2 Specification
http://www.usb.org/developers/docs/

10 Abbreviations

Term	Definition
Client Computer	Controller computer networked to host PC for remote control desktop connection
DUT	Device Under Test
EHCI	Enhanced Host Controller Interface(USB2.0)
xHCI	Extensible Host Controller Interface(USB3.0)
OHCI	Open Host Controller Interface
UHCI	universal host controller interface(USB1.1)
Host Computer	Server platform operated by Client PC through remote desktop connection
HSETT	High Speed Electrical Test Tool
LAN	Local Area Network
Legacy-free	Any system that does not have PS/2 and other legacy ports
PCIe	Peripheral Component Interconnect Express Bus
PID	Product Identification Number
PS/2 port	A legacy mouse or keyboard port located on some motherboards
UAC	User Account Control
USB	Universal Serial Bus
VID	Vendor Identification Number
TID	Product Test ID assigned by USB-IF after passing the USB Certification Test

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12 Revision history

Table 67 provides a revision history for this application note. Note that this revision history table reflects the changes to this template, but it can also be used for your document's revision history.

Table 67. Revision history

Rev. Number	Date	Substantive Change
4	08 June 2023	Section 8.3.4.1 is updated
3	03/2023	Section 8.6 is added.
2	01/2019	Section 2.1 is modified to cover more i.MX series. Section 2.2 is modified to support the latest version of I.MX series. Section 2.3 and 2.4 add the corresponding equipment of USB 3.0 Super Speed compliance test. Section 2.8 update to the newest links. Section 3.2 is added to cover the software for i.MX 7/8. Section 3.4 is added to the USB 3.0 Super Speed Transmitter Compliance Test. Section 9 Useful links updated. The serial number of Figures are adjusted. Section 8 The USB PHY Registers and Software Configurations for some I.MX8 series are covered in this revision.
1	02/2017	Modified section 2.1 Modified section 2.2 Modified section 3.1 Section 7 Useful links updated
0	10/2015	Initial release

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