IMX8ULPCEC

i.MX 8ULP Applications Processor—Commercial Products

Rev. 1 — 09/2023

Data Sheet: Technical Data

The i.MX 8ULP family of processors features NXP's advanced implementation of the dual Arm® Cortex®-A35 cores alongside an Arm Cortex-M33. This combined architecture enables the device to run a rich operating system (such as Linux) on the Cortex-A35 core and an RTOS (such as FreeRTOS) on the Cortex-M33 core. It also includes a Fusion DSP for low-power audio and a HiFi4 DSP for advanced audio and machine learning applications. The i.MX 8ULP processor provides a 32-bit LPDDR3/LPDDR4/LPDDR4X memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays. Additionally, there are 2 co-processors connected to the Cortex-M33 core: PowerQuad and Casper, accelerating DSP and cryptography functions, respectively.

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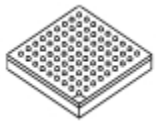
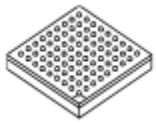


485 MAPBGA

15 x 15 mm, 0.5 mm pitch



512 FCBGA

9.4 x 9.4 mm, 0.4 mm pitch

Table 1. i.MX 8ULP features

Feature type	Application processor domain	Real-time processor domain
ARM Processor	Dual core Cortex®-A35	Cortex®-M33F
	Frequency: 800 MHz	Nominal (RUN) frequency: 216 MHz
	32 KB instruction and 32 KB data cache	32 KB instruction and 32 KB data cache
	Floating Point Unit (FPU)	Floating Point Unit (FPU)
	512 KB of L2 cache with Snoop Control Unit (SCU)	Memory Protection Unit (MPU)
	NEON™ SIMD engine	Co-processor interface for • PowerQuad hardware accelerator (Fixed and floating point +FFT) DSP functions • CASPER Crypto/FFT engine
	—	Tensilica DSP Fusion F1 DSP processor Nominal frequency: 200 MHz
	32 channel DMA	32 channel DMA
On-chip memory	64 KB of RAM	768 KB of Shared Memory, zero wait state
	192 KB of Boot ROM	96 KB of Boot ROM

Table continues on the next page...

Table 1. i.MX 8ULP features (continued)

Feature type	Application processor domain	Real-time processor domain
External memory interfaces	FlexSPI Serial flash interface to quad/octalSPI flash device	Dual FlexSPI Serial flash interface to quad/ octalSPI flash device
	3 eMMC/SD host interfaces supporting eMMC5.1 and SD3.0	—
	32-bit LPDDR3, LPDDR4, LPDDR4x	
Security	Cryptographic acceleration supporting • symmetric and asymmetric ciphering algorithms • SHA-256 hashing algorithm	EdgeLock secure enclave (ELke) as Root of Trust (RoT) • Core supporting up-to 216 MHz • Dedicated boot ROM with Advanced High Assurance boot (AHAB) • ECDSA P256 based signature verification • Support for symmetric Cryptographic acceleration (SGI) • Support for Asymmetric Cryptographic acceleration (PKC) • NIST compliant RNG with DRGB • One-Time Programmable electrical fuse used for security keys
	NIST-approved random number generator	On-The-Fly decryption of the encrypted code stored in external flash device
	32 KB secure RAM	—
Communication, Timer, and Analog peripherals	• Dual High speed USB OTG port with integrated PHY	—
	4x UART ports	4x UART ports
	2x SPI ports	4x SPI ports
	4x I2C ports	4x I2C ports
	I3C port	2x I3C ports
	2x I2S ports	4x I2S ports
	-	FlexCAN
	-	FlexIO
	1 x Ethernet 10/100-Mbit/s, compliant with the IEEE802.3-2002 standard.	-
	Secure and non-secure Watchdog timers	Secure and non-secure Watchdog timer for CM33. Watchdog timer for the Fusion DSP

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Table 1. i.MX 8ULP features (continued)

Feature type	Application processor domain	Real-time processor domain
	4x 32-bit timers	4x 32-bit timers
	1x MQS	1x MQS
	System timers	System timers
	-	2x 12-bit ADC
	-	2x DAC
		2x analog CMP
		8x DMIC (Dual/Stereo digital microphone interface)
Low power audio video video domain		
Processor	Tensilica HiFi4 DSP	
	Maximum Frequency up to 600 MHz	
	Quad MAC 32 with Dual Load/Store	
	Cached Based design with AXI access to LPDDR memory	
	Integrated Dual 2-way SMID VFPU	
	32-channel DMA	
On-chip memory	64 KB on-chip RAM	
	32 KB instruction cache	
	64 KB data cache	
	64 KB ITCM	
	64KB DTCM	
External memory interfaces	32-bit LPDDR3, LPDDR4, LPDDR4x	
Graphics, display and Camera interface	GPU3D • Support for Open GL ES 3.1, Vulkan 1.1, Open CL 2.x and Open VG1.1	
	GPU2D Composition Processing Core (CPC) GPU	
	4-lane MIPI DSI interface	
	Dual lane MIPI CSI interface	
	Image Sensing interface (ISI) with one pixel link interface	
	PXP E-Ink Display Engine	
	Display controller (DCNano) that supports EPDC panels through MIPI, Smart Displays and Video mode	
	Can be optionally powered off when not in use	
Audio peripherals	2 I2S ports	
Timers	1x 32-bit Timer	

Table continues on the next page...

Table 1. i.MX 8ULP features (continued)

Feature type	Application processor domain	Real-time processor domain
	1x Watchdog (WDOG) timer	
Low Power Implementation		
Power Management	uPower Sub-system for advanced Power measurement[1] and control functionality • RISC-V ISA compliant CPU core • Dedicated code and data RAM • Critical path and process monitors to provide device parameters • Supports DVFS (Dynamic Voltage and Frequency Scaling)	
	Multiple power domains and ultra-low power modes allow flexible power saving	
	HiFi4 DSP can be power gated while keeping DSP domain operational for Voice trigger	

1. Power measurement accuracy is expected to be +/- 10% after trim, for currents of 20% to 100% of switches' specified current value. This IP has not been characterized. Measure capability not implemented on all switches

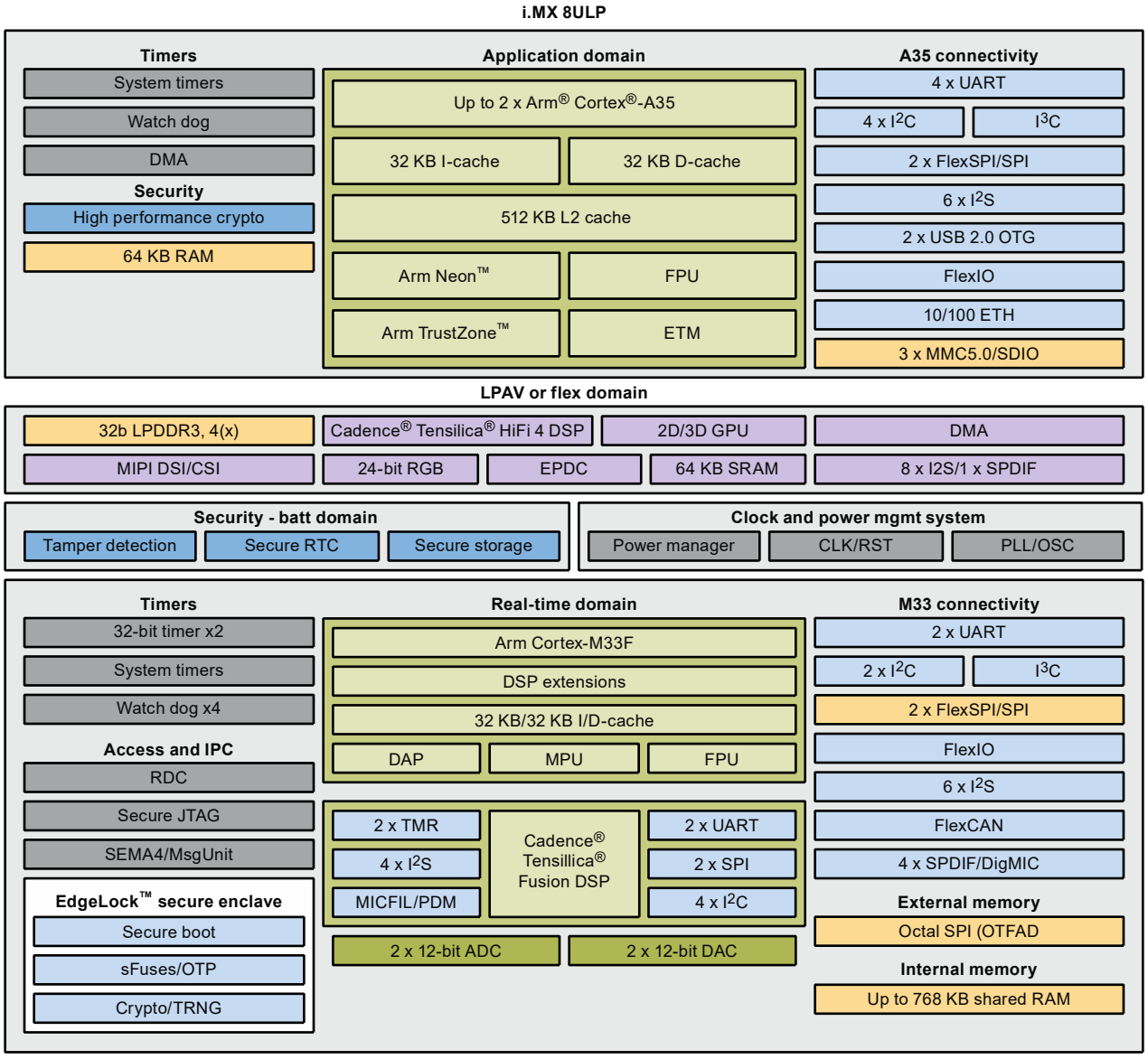

Figure 1. i.MX 8ULP Block Diagram

The following table provides examples of orderable sample part numbers covered by this data sheet.

Table 2. Ordering information

MC Part Numbers	Cortex-A35 Speed Grade	Cortex-M33 Speed Grade (MHz)	Package	Temperature Range
MIMX8UD5DVP08SC	800 MHz	216	MAPBGA 15 mm x 15 mm, 0.5 mm pitch	T_a0 to T_j+95 °C
MIMX8US3DVP08SC	800 MHz	216	MAPBGA 15 mm x 15 mm, 0.5 mm pitch	T_a0 to T_j+95 °C

Table continues on the next page...

Table 2. Ordering information (continued)

MC Part Numbers	Cortex-A35 Speed Grade	Cortex-M33 Speed Grade (MHz)	Package	Temperature Range
MIMX8UD3DVK08SC	800 MHz	216	FCBGA 9.4 mm x 9.4 mm, 0.4 mm pitch	T_a0 to T_j+95 °C
MIMX8UD5DVK08SC	800 MHz	216	FCBGA 9.4 mm x 9.4 mm, 0.4 mm pitch	T_a0 to T_j+95 °C
MIMX8UD7DVP08SC	800 MHz	216	MAPBGA 15 mm x 15 mm, 0.5 mm pitch	T_a0 to T_j+95 °C
MIMX8UD3DVP08SC	800 MHz	216	MAPBGA 15 mm x 15 mm, 0.5 mm pitch	T_a0 to T_j+95 °C
MIMX8US5DVP08SC	800 MHz	216	MAPBGA 15 mm x 15 mm, 0.5 mm pitch	T_a0 to T_j+95 °C
MIMX8US3DVK08SC	800 MHz	216	FCBGA 9.4 mm x 9.4 mm, 0.4 mm pitch	T_a0 to T_j+95 °C
MIMX8UD5CVP08SC	800 MHz	216	MAPBGA 15 mm x 15 mm, 0.5 mm pitch	T_a-40 to T_j+105 °C

The following figure describes the part number nomenclature so users can identify the characteristics of the specific part number.

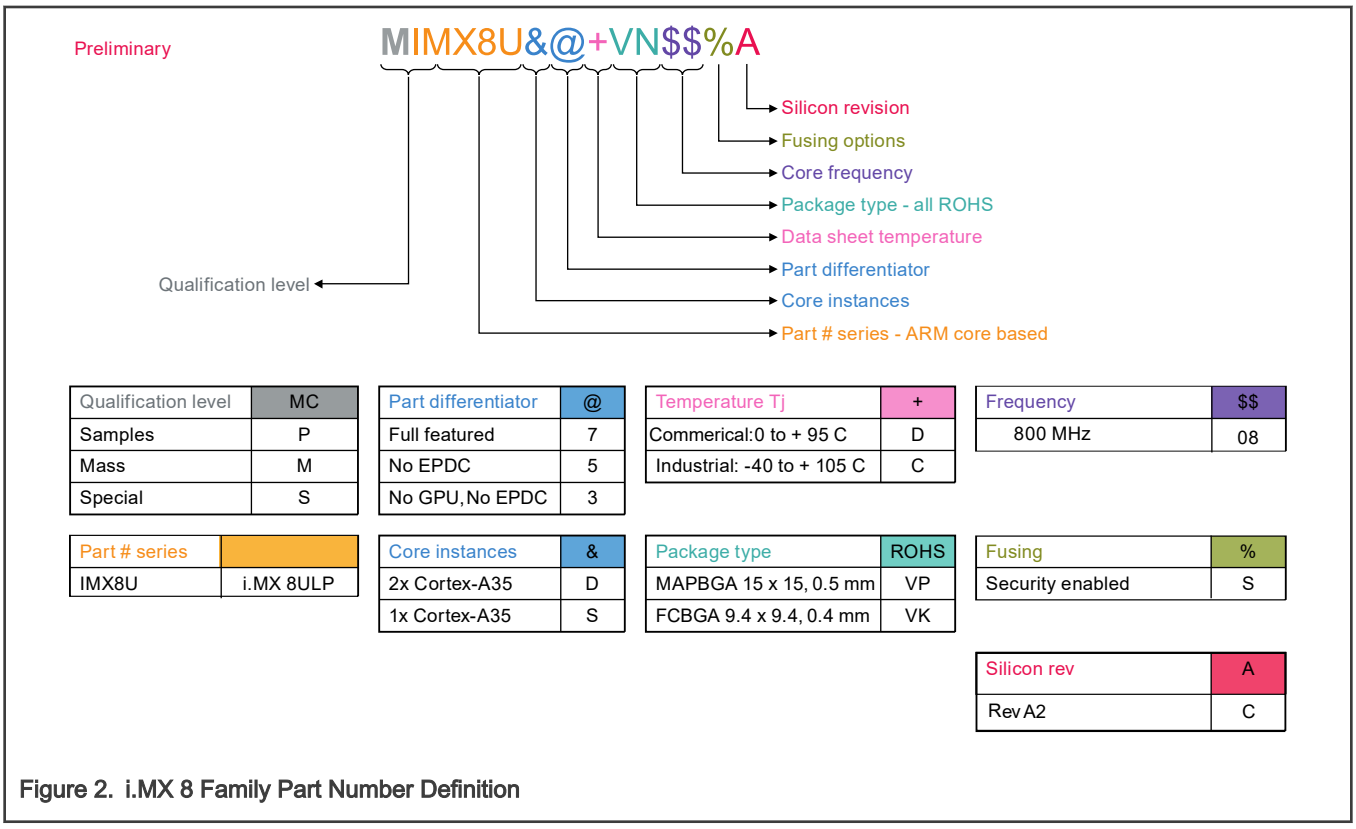

Figure 2. i.MX 8 Family Part Number Definition

Table 3. Related Resources

Type	Description
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Reference Manual	The *i.MX 8ULP Applications Processor Reference Manual* contains a comprehensive description of the structure and function (operation) of the SoC.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in the data sheet.

Contents

1 i.MX 8ULP modules list

The i.MX 8ULP applications processor contains a variety of digital and analog modules.

In the Domain column in this table:

- APD = Application Power or A35 Domain (primarily controlled by the Cortex-A35 core)
- RTD = Real-Time or M33 Domain (primarily controlled by the Cortex-M33 core)
- LPAVD/Flex = Low Power Audio Video domain
- DSPD: DSP Processor Domain

Module	Domain	Description
Memories and memory controllers		
SRAM1	LPAVD	An AXI RAM Controller (RAMC), which acts as an interface between the AXI bus and RAM, is used on each SRAM connected to the NIC crossbar.
SSRAM	RTD	768KB of System Memory shared between M33, Fusion and other Masters. SSRAM is divided into multiple partitions. System software will determine how each partition is utilized and CPU/Master controlling that partition. Fusion and M33 accesses these partition via dedicated tightly couple memory buses (TCM), with zero wait-state. There is also backdoor port that allows M33 DMA and other bus masters in the SoC to access this memory.
XCACHE	RTD	The AHB Cache Controller (CAC) is a processor-local Level 1 (L1) bus cache controller for use with cores using AMBA-AHB input/output buses. It is optimized for minimum RunIDD (dynamic power).
LPDDR4C	APD, LPAVD	The LPDDR Controller is a configurable DDR controller that provides interface to 32-bit LPDDR3, LPDDR4 and LPDDR4x memories. It supports up to 2 GB DDR memory space. The LDDR4C includes a DFI interface to work with PHY. The controller is responsible for communication with the system through AXI interface, DDR commands generation, DDR command optimizations, and read/ write data path. The PHY performs timing adjustment using special calibration mechanisms to ensure data capture margin at the supported clock rate.
FlexSPI0-2	APD, RTD	The Flexible Serial Peripheral Interface (FlexSPI) module provides an interface to various types of serial flash memory. The QSPI interface allows up to two serial flash connections. It supports 1-bit, 4-bit and 8-bit SPI bus width.
uSDHC0-2	APD	The ultra Secure Digital Host Controller (uSDHC) provides the interface between the host system and SD, SDIO or eMMC cards. The uSDHC acts as a bridge, passing host bus transactions to the cards by sending commands and performing data accesses to/from the cards or devices. It handles SD, SDIO and eMMC protocol at transmission level.
DMA, Bus Fabric and Gaskets		

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Module	Domain	Description
Memories and memory controllers		
DMA0-2	APD, RTD	Direct Memory Access (DMA) is capable of performing complex data transfers with minimal intervention from a host processor. Each DMA module supports 32 DMA channels. The transfer control descriptors for each of the 32 channels located in system memory.
DMAMUX0-2		The Direct Memory Access Multiplexer (DMAMUX) module routes DMA sources, called slots, to any of the supported DMA channels. On this device, DMAMUX is an integrated component within the DMA module.
NIC-301	APD	The AMBA Network Interconnect Crossbar (NIC) is a high performance AMBA-compliant network infrastructure which arbitrates between multiple AXI or AHB masters to grant access to internal or external memories or other slave devices. It supports connectivity between several slave and master ports for parallel processing. It uses a hybrid round-robin arbitration scheme and contains frequency converters, data width converters, bus protocol converter, and AXI channel buffers.
AXBS-Lite (XBAR_7x2 and XBAR_DSP) and AXBS-Full (AXBS0, AXBS1)	APD, RTD	AHB-Lite Cross Bar Switch (AXBS-Lite) is a crossbar switch module that arbitrates between multiple AHB masters to grant access to downstream AHB slave devices. The crossbar enables multiple masters to connect to slaves and parallel processing.
AHB-PBridge (PBRIDGE0-5)	RTD, APD, LPAVD	The AHB-Peripheral Bridge (AHB-PBridge) module interfaces an AHB bus to the peripheral bus. There are 2 AHB-PBridge instances in this device. Each AHBPBridge module supports 128 IP slots. Each slot occupies 64 KB of address space.
PortSplitter		The PortSplitter gasket splits an AHB master port to multiple AHB slave ports based on address decoding.
BME	RTD	The Bit Manipulation Engine (BME) provides hardware support for atomic read-modify-write memory operations to the peripheral address space. This architectural capability is also known as "decorated storage" as it defines a mechanism to provide additional semantics for load and store operations to memory-mapped peripherals beyond just the reading and writing of data values to the addressed memory locations.
Multicore peripherals		
MU0-3	RTD, LPAVD, and DSPD	Messaging Unit (MU) is a shared peripheral with a 32-bit IP bus interface and interrupt request signals to each host processor. The MU exposes a set of registers to each processor which facilitate inter-processor communication via 32-bit words, interrupts and flags. Interrupts may be independently masked by each processor to allow polled- mode operation. The uPower subsystem also contains 2 instances of MU module.
SEMA42_0-2	APD, RTD, and LPAVD	The Hardware Semaphore (SEMA42) module provides the hardware support needed in multicore systems for implementing semaphores

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Module	Domain	Description
Memories and memory controllers		
		and provide a simple mechanism to achieve "lock/unlock" operations via a single write access.
XRDC	RTD	The Extended Resource Domain Controller (XRDC) provides an integrated, scalable architectural framework for access control, system memory protection and peripheral isolation. It allows software to assign chip resources (like processor cores, non-core bus masters, memory regions and slave peripherals) to processing domains, to support enforcement of robust operational environments. The XRDC implementation is distributed across multiple submodules instantiated throughout the device.
MGR	RTD	The XRDC Manager (MGR) submodule coordinates all programming model reads and writes.
MDAC	APD, RTD	The XRDC Master Domain Assignment Controller (MDAC) submodule handles resource assignments and generation of the domain identifiers.
MRC	APD, RTD	The XRDC Memory Region Controller (MRC) submodule implements the access controls for slave memories based on the pre-programmed region descriptor registers
PAC	APD, RTD	The XRDC Peripheral Access Controller (PAC) implements the access controls for slave peripherals based on the pre-programmed domain access control registers.
TRDC	RTD	The Trusted Resource Domain Controller (TRDC) provides an integrated, scalable architectural framework for access control, system memory protection and peripheral isolation. It allows software to assign chip resources including processor cores, non-core bus masters, memory regions and slave peripherals to processing domains to support enforcement of robust operational environments.
Connectivity and communications		
SAI0-7	APD, RTD	The Synchronous Audio Interface (SAI) module implements full-duplex serial interfaces with frame synchronization such as I2S, AC97, and CODEC/DSP interfaces.
LPI2C0-7	APD, RTD	The Low Power Inter-Integrated Circuit (LPI2C) module implements an efficient interface to an I2C bus as a master. The LPI2C can continue operating while the processor is in stop mode provided an appropriate peripheral clock is available.This module is designed for low CPU overhead with DMA offloading of FIFO register accesses.
I3C0-2	APD, RTD	I3C Master/Slave interface. Supports DDR.
ENET	APD	10M/100M Ethernet Controller (ENET).
FlexCAN	RTD	The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications

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Module	Domain	Description
Memories and memory controllers		
LPUART0-7	APD, RTD	The Low Power Universal Asynchronous Receiver/Transmitter (LPUART) module provides asynchronous, serial communication capability with external devices. LPUART supports non-return-to-zero (NRZ) encoding format and IrDA-compatible infrared (low-speed) SIR format. The LPUART can continue operating while the processor is in stop mode if an appropriate peripheral clock is available. This module is designed for low CPU overhead with DMA offloading of FIFO register accesses.
LPSPI0-5	APD, RTD	The Low Power Serial Peripheral Interface (LPSPI) module implements an efficient interface to a SPI bus as a master and/or a slave. The LPSPI can continue operating while the processor is in stop mode if an appropriate peripheral clock is available. This module is designed for low CPU overhead with DMA off-loading of FIFO register accesses.
USB-OTG0-1, USB-XBAR	APD, RTD	The Universal System Bus On-The-Go (USB-OTG) module is a USB 2.0-compliant implementation. The registers and data structures of this USB controller are based on the Enhanced Host Controller Interface Specification for Universal Serial Bus(EHCI). This module can act as a host, a device or an On-The-Go negotiable host/device on the USB bus.
USBDCD	APD	The USBDCD module works with the USB transceiver to detect whether the USB device is attached to a Charging Port, either a Dedicated Charging Port (DCP) or a Charging Downstream Port (CDP).
USB-PHY	APD	The Universal System Bus Physical Layer (USB-PHY) macrocell implements USB physical layer connecting to USB host/device systems at low-speed, full-speed, and high-speed. USB-PHY provides a standard UTMI interface for connection to the USB-OTG controller.
FlexIO0-1	APD, RTD	The Flexible Input/Output (FlexIO) module is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, etc.
Timers		
LPTMR0-1	APD, RTD	The Low Power Timer (LPTMR) module is a 16-bit timer which operates as real-time interrupt or pulse accumulator. This LPTMR module can remain functional when the chip is in low power modes, provided the reference clock to this timer is active.
LPTPM0-8	APD, RTD	The Timer/Pulse Width Modulation Module (LPTPM or TPM) is a multi-channel timer module that supports input capture, output compare, and the generation of PWM signals.The counter, compare and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

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Module	Domain	Description
Memories and memory controllers		
LPIT0-1	APD, RTD	Low Power Periodic Interrupt Timer (LPIT) is a multi- channel timer module that can generate independent pre- trigger and trigger outputs. These timer channels can operate individually or can be chained together. The pre- trigger and trigger outputscan be used to trigger other modules on the device. The LPIT can also operate in low power modes.
MRT	RTD	The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval.
TSTMR0-1	APD, RTD	The TSTMR module is a free running incrementing counter that starts running after system reset de-assertion and can be read at any time by the software for determining the software ticks. The TSTMR is a 64-bit clock cycle counter. It runs off the 1 MHz clock and resets on every system reset. The counter only stops when the clock to the TSTMR is disabled.
WDOG0-8	APD, DSPD, RTD and LPAVD	The Watchdog Timer (WDOG) module keeps a watch on the system functioning and resets it in case of its failure. Reasons for failure include run-away software code and the stoppage of the system clock that in a safety critical system can lead to serious consequences. In such cases, the WDOG brings the system into a safe state of operation.The WDOG monitors the operation of the system by expecting periodic communication from the software, generally known as servicing orrefreshing the WDOG. If this periodic refreshing does not occur, the WDOG resets the system. There are two instances of WDOG in the uPower subsystem and two instances within the EdgeLock secure enclave subsystem.
EWM	RTD	The External Watchdog Monitor (EWM) module is designed to monitor external circuits, as well as the software flow. This provides a back-up mechanism to the internal WDOG that can reset the system. The EWM differs from the internal WDOG in that it does not reset the system. The EWM, if allowed to time-out, provides an independent trigger pin that when asserted resets or places an external circuit into a safe mode.
Graphic Processor Human Machine Interfaces		
GPU-3D	LPAVD	Verisilicon GCNanoUltra3.1 supports Open GL ES 3.1, Vulkan 1.3, Open CL 3.0 and Open VG1.1
GPU-2D	LPAVD	GPU-2D supports user interface rendering and performs functions like blending, filtering, rotation, overlay, resizing, transparency, and other dynamic effects.
MIPI DSI Controller	LPAVD	The MIPI Display Serial Interface Controller (DSI Controller) is responsible for serializing display data from the GPU. Data can come from either the GPU or the processor/DMA controller.

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Module	Domain	Description
Memories and memory controllers		
MIPI-CSI-2 Controller	LPAVD	MIPI Camera Serial Interface (MIPI-CSI-2) is a dual lane interface that supports up to 1500 Mbps.
MIPI D-PHY	LPAVD	Both MPI-DSI (4-lane) and MIPI-CSI-2 (2-lane) use MIPI Display Physical Layer (D-PHY).
LCDIF/DCNano	LPAVD	The DCNano (from Verisilicon) is a general purpose display controller used to drive a wide range of display devices varying in size and capabilities.
SPDIF	LPAVD	The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF transceiver allows the handling of both SPDIF channel status (CS) and User(U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.
PDM/MICFIL	LPAVD, DSPD	PDM Microphone Interface (DMIC) allows connection of MEMS digital microphones with PDM output to the MCU. The interface can support from 1 to 16 microphones, using up to 8 input data lines and one clock line.
PXP	LPAVD	Pixel Pipeline interface to process graphics buffers composite video and graphics data before sending to an display.
EPDC	LPAVD	The Electrophoretic Display Controller(EPDC) is a feature-rich, low power and high performance direct drive active matrix EPD controller. It is specifically designed to drive E•INK™ EPD panels supporting a wide variety of TFT backplanes.
ISI	LPAVD	The Image Sensing Interface (ISI) module interfaces 1 pixel link source to obtain the image data for processing in its pipeline channels.
Analog		
ADC0-1	RTD	Analog to Digital Converter (ADC) is a 12-bit resolution, successive approximation analog to digital converter. The ADC module supports up to 16 single-ended external analog inputs. It outputs 12-bit, 10-bit, or 8-bit digital signal in right-justified unsigned format.
DAC0-1	RTD	Digital to Analog Converter (DAC) is the 12-bit resolution digital-to-analog converters with programmable reference generator output. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator or ADC.
CMP0-1	RTD	The Comparator (CMP) module provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail to rail operation).
Security		
CAAM	APD	Cryptographic Acceleration and Assurance Module (CAAM) is an multi-function accelerator that supports the cryptographic functions common

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Module	Domain	Description
Memories and memory controllers		
		in many security protocols. This includes AES128, AES256, DES, 3DES, SHA1, SHA224, SHA256, and a random number generator with a true entropic seed. CAAM includes a DMA engine that is descriptor based to reduce processor-accelerator interaction. Security feature clear keys and memories when on-chip security monitor detects tampering. The Secure RAM is implemented and provides secure storage of sensitive information both in on-chip RAM and in off-chip, nonvolatile memory.
EdgeLock secure enclave (ELke)	RTD	RISC-V based Root of Trust. Part of M33 domain.It includes dedicated ROM that authenticates any FW images via Advanced HAB(AHAB). ELke also moderates any Read/writes to the fuses apart from crypto accelerators.
CRC[1]	RTD	The Cyclic Redundancy Check (CRC) module is a hardware CRC generator circuit using 16/32-bit shift register. The CRC module supports error detection for all single, double, odd, and most multi-bits errors, programmable initial seed value, and optional feature to transpose input data and CRC result via transpose register.
OTFAD[2]	RTD	The On-The-Fly AES Decryption (OTFAD) module provides an advanced hardware implementation that minimizes any incremental cycles of latency introduced by the decryption in the overall external memory access time. The OTFAD engine also includes complete hardware support for a standard AES key unwrap mechanism to decrypt a key BLOB data instruction containing the parameters needed for up to 4 unique AES contexts.
Debug and Test		
DAP	RTD	Debug Port Access (DAP) provides debugger access to on- chip system resources via the SWJ-DP port. The DAP provides internal system access to A35 Debug Port, M33 Debug Port, System Bus, JTAG controller, and SoC Control and Status. TheDAP also enables system access to CoreSight debug subsystem through the APBIC port.
CTM	RTD	Cross Trigger Matrix (CTM) is a component of the Embedded Cross Trigger (ECT), which is key in the multi- core debug strategy. The CTM receives signals from various sources (i.e. cores and peripherals) and propagates or routes them to thedifferent debug resources of the SoC. Those debug resources can include time stamping capability, real-time trace, triggers and debug interrupts.
ETF	RTD	The Embedded Trace FIFO (ETF) consists of a formatter, control, and the trace RAM. It is a configuration of the Trace Memory Controller (TMC). The ETF will have a memory size of 16Kbytes. The ETF and associated memory should be connectedin the system such that it will retain the information though a warm or cold reset of the system. This is to allow for debug information to be retained for debugging problems that may arise and cause a reset of the system.

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Module	Domain	Description
Memories and memory controllers		
ETR	RTD	The ETR is a trace sink that redirects the trace stream onto the AXI bus to external storage. It can utilize a single contiguous region or a scattered allocation of blocks for a circular buffer. Reading of the AXI based trace buffer can either be done directly over AXI from a normal bus master. The ETR is a configuration option of the TMC as is the ETF.
FUNL	RTD	The Trace Funnel (FUNL) is used when there is more than one trace source. The Trace Funnel combines multiple trace stream onto a single ATB bus. The Trace Funnel includes an arbiter that determines the priority of the ATB inputs.
Replicator	RTD	The Trace Replicator (Replicator) enables two trace sinks (TPIU and TMC) to be wired together and receive ATB trace data from the same trace source. It takes incoming data from a single source and replicates it to two master ports.
TPIU	RTD	Trace Port Interface Unit (TPIU) acts as a bridge between on-chip trace data, ID distinguishable, and a TPA. It receives ATB trace data and sends it off chip via Arm’s standard trace interface. The TPIU includes ATB interface, APB interface,Formatter, Asychronous FIFO, Register bank, Trace out serializer, and a Pattern generator.
SWO	RTD	Single Wire Output (SWO) is a trace data drain that acts as bridge between the on-chip trace data to a data stream that is captured by the Trace Port Analyzer. It is a TPIU-like device that supports a limited subset of the full TPIU functionality for asimple debug solution.
TimeStamp Components		The timestamp components generate and distribute a consistent timestamp value for multiple processors and other blocks in a SoC. [revisit]
JTAGC	RTD	Joint Test Action Group Controller (JTAGC) provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard
Clock Sources and Control		
CGC0-2	RTD, APD, LPAVD	The System Clock Generation (SCG) module is responsible for clock generation and distribution across this device. Functions performed by the SCG include: clock reference selection, generation of clock used to derive processor, system, peripheral bus and external memory interface clocks; source selection for peripheral clocks; and, control of power saving clock gating mode.
PCC0-5	RTD, APD	The Peripheral Clock Control (PCC) module is responsible for clock selection, optional division and clock gating mode for peripherals in their respected power domain.

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Module	Domain	Description
Memories and memory controllers		
RTC OSC		The Real Time Clock Oscillator (RTC OSC) module provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock for the RTC.
SYS OSC		The System Oscillator (SYS OSC) module is a crystal oscillator. The SYS OSC, in conjunction with an external crystal or resonator, generates a reference clock for this device. It also supports optionally external input bypass clock from EXTAL signal directly.
USB PLL		USB Phase Locked Loop (USB PLL) is embedded in the USB transceiver block. This PLL allows an exact 480 MHz to be generated from a supported reference clock of 24 MHz. The output of this PLL is primarily used for PLL operation. The USB PLL clock is also made available as a clock source for other peripherals in the SoC.
Fixed-Freq PLL (PLL0)		The Fixed-freq PLL is the same as the USB PLL . In addition to the main clock output, this PLL also includes 4 Phase Fractional Dividers (PFDs) that can generate other clock frequencies. There is one instance of the Fixed-freq PLL (PLL0) provides clocks for M4 core and buses and peripherals in the Realtime domains.
Frac-N PLL (PLL1-3)		The Fractional-N (Frac-N) PLL can generate an output clock of 528 MHz from a supported reference clock. In addition to the main clock output, this PLL also includes up to 4 Phase Fractional Dividers (PFDs) that can generate other clock frequencies. This PLL also supports tunnable clock for audio applications.
AV Frac-N-PLL		1.2 GHz Fractional PLL
192 MHz FRO		Low Power IRC with tuning logic to generate 192 MHz. System defaults to FRO for as initial boot clock.
LPO (1 MHz)		The Internal Reference Clock (1 MHz) module is an internal oscillator that can generate a reference clock of 1 MHz. The LPO clock is enabled in all modes of operation, including all low power modes.
Power Management		
Micro-Power (uPower)	RTD, APD	Dedicated RISC-V based Power management and control block. Allows DVFS via dedicated processor monitors and control logic.
Digital PMC		The Digital PMC module allows user software to control power modes of the chip and to optimize power consumption for the level of functionality needed. There are two instances of Digital PMC on this device, one for each main power domain. It is a part of micro-Power subsystem.
Analog PMC		The Analog PMC consists of voltage/current references, core logic supply regulators, memory supply regulators, Back and Forward Biasing regulators, monitors and power switches, etc. There are three

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Module	Domain	Description
Memories and memory controllers		
		Analog PMC subsystems in 8ULP, one associated with the M33 power domain, one with LPAV and the other with the A35 power domain.
System Control		
RMC0-1		Reset Mode Controller (RMC) implements reset modes and reset functions of the chip.
CMC0-2	APD, RTD, LPAVD	The Real Time Domain Core Mode Controller (CMC0) is responsible for sequencing the M33 CPU and associated logic through the different operating modes. The Application Domain Core Mode Controller (CMC1) is responsible for sequencing the A35 CPU cluster and associated logic through the different operating modes. CMC2 is the CMC instance in the low-power audio video domain (LPAV), which is a slave domain without internal ARM Core. Its Low Power Modes, Clock Gate Modes and reset follows the Master Domain, either Real-time or Application domain.
WUU0-1	APD, RTD	The Low-Leakage Wake-Up Unit (LLWU) module allows user to select up to 32 external pin sources and up to 8 internal modules as a wakeup source from low-leakage power modes. Also known as LLWU.
WIC		The Wakeup Interrupt Controller (WIC) module is capable of interrupt detection and wake up a processor when it is in low power mode.
WKPU0-1	RTD, APD	Wakeup Unit (WKPU) module is capable of interrupt detection and wake a Cortex-A processor when it is in low power mode. There is one WKPU instance for each A35 Core on i.MX 8ULP.
IOMUXC0-2	APD, RTD	The Input/Output Multiplexing Controller (IOMUXC) enables the chip to share one pad for multiple signals from different peripheral interfaces. This pad sharing mechanism is done by multiplexing the pad's input and output signals. TheIOMUXC also controls the pads setting parameters and digital filter functions of the pad. In addition, the IOMUXC controls input multiplexing logic for input signals multiplexed at multiple locations
SIM0-2	APD, RTD, LPAVD	The System Integration Module (SIM) provides system control and chip configuration registers. The SIM may include the TSTMR module.
TRGMUX0-1	APD, RTD	Peripheral Trigger Multiplexing (TRGMUX)
RGPIO2P0-1	RTD, APD	The Rapid General-Purpose Input and Output with 2 Ports (RGPIO2P) is similar to the RGPIO module, except it has an AHB-lite port, in addition to the IPS port, for faster access.
OCOTP_CTRL		The On-Chip One-Time-Programmable Controller (OCOTP_CTRL) module provides an interface for reading, programming and/or overriding identification andcontrol information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses. The OCOTP_CTRL also provides a set of volatile software-accessible

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Module	Domain	Description
Memories and memory controllers		
		signals which can be used for software control of hardware elements, not requiring non-volatility.
Co-Processors		
PowerQuad	RTD	PowerQuad is a Digital Signal Co-Processing companion to a Cortex-M v8M CPU core. It can be accessed via Co-processor interface provided by the Cortex CPU, and via AHB address space.
CASPER	RTD	The Cryptographic Accelerator and Signaling Processing Engine with RAM-sharing (CASPER) peripheral provides acceleration of asymmetric cryptographic algorithms as well as optionally of certain signal processing algorithms.

1. Only available in EdgeLock secure enclave document
2. Only available in security RM

2 Specifications

NOTE

- All the specifications/values contained in the subsequent sections of this document are preliminary and subject to change.
- Any reference to VDD or VDD throughout the document corresponds to VDD_DIG0, VDD_DIG1 or VDD_DIG2, depending on where the module resides physically.

2.1 Application domain (implementing Arm Cortex-A35)

Application domain is built around a dual core Cortex-A35 cluster optimized for 800 MHz operation for Linux based applications. The Application domain has several different power islands where each island is optimized for idle, low power idle and suspend modes. The i.MX 8ULP processor provides a 32-bit LPDDR3, LPDDR4, and LPDDR4X memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays.

2.1.1 Memory system—application domain

2.1.1.1 Internal memory (application domain)

- SRAM0 (64KB)
- SRAM2 (256 KB shared with L2 Cache)

2.1.1.2 eMMC

eMMC is a managed NAND device.

2.1.2 Peripherals—application domain

2.1.2.1 Security—application domain

The following section provides detail about the security modules.

2.1.2.1.1 True Random Number Generator (TRNG)

The TRNG module is used to generate high quality, cryptographically secure, random data. The TRNG module is capable of generating its own entropy using an integrated ring oscillator. In addition, the module's Pseudo-Random Number Generator (PRNG) provides accelerated processing of pseudo-random data.

2.1.2.1.2 Real-Time Clock (RTC)

The RTC module provides 64-bit monotonic counter with roll-over protection, 32-bit seconds counter with roll-over protection and 32-bit alarm. This timer module is extremely low power that allows it to operate on a backup power supply when the main power supply is cut off. The RTC remains functional in all low power modes and can generate an interrupt to exit any low power mode.

2.1.2.1.3 Battery-Backed secure module (BBSM)

The Battery-Backed Security Module (BBSM) serves as nonvolatile security logic and storage for Edgelock secure enclave. See S400 Reference Manual for BBSM chapter.

The following table shows the osc32 specs of this module.

Symbol	Parameter	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal	-	32.768	-	kHz
$V_{ec\_extal32}$	Externally provided input clock amplitude	0.7	-	VDD_VBAT18_CAP	V

2.1.2.2 Timers—application domain

The i.MX 8ULP Application Domain implements the following timers:

- Low Power Periodic Interrupt Timer (LPIT)
- Timer/PWM Module (LPTPM)
- External Watchdog Monitor(EWM)
- Time stamp timer module (TSTMR)
- Watchdog Timer (WDOG)
- Multirate Timer (MRT)

See i.MX 8ULP modules list.

2.1.2.3 Connectivity and communications—applications domain

The i.MX 8ULP Application Domain implements the following connectivity and communications peripherals:

- Secure Digital (SD) Interface via the uSDHC
- Low Power Universal Asynchronous Receiver/Transmitter (LPUART)
- Low Power Inter-Integrated Circuit (LPI2C)
- Low Power Serial Peripheral Interface (LPSPI)
- Universal System Bus On-The-Go (USB-OTG)
- Improved Inter-Integrated Circuit Interface (I3C)
- Flexible Serial Peripheral Interface (FlexSPI)
- 10/100 Mpbs Ethernet Controller (ENET)

- Flexible Input/Output (FlexIO)

See the i.MX 8ULP modules list for more details.

2.2 Peripherals—low power audio video (LPAV) domain

2.2.1 Graphics processor and human machine interfaces

The i.MX 8ULP Application Domain implements the following graphics processor human machine interfaces:

- 3D graphics processing unit (GPU-3D)
- 2D graphics processing unit (GPU-2D)
- MIPI Display Serial Interface Controller (MIPI DSI)
- DCNano Display Controller
- Pixel Pipeline interface (PXP)
- MIPI Camera Serial Interface (MIPI-CSI)
- The Electrophoretic Display Controller (EPDC)
- HiFi4 DSP

See the i.MX 8ULP modules list for more details.

2.3 Real-time domain (implementing Arm Cortex-M33)

The real-time domain is built around an Arm Cortex-M33 processor that contains a floating-point unit and is optimized for lowest possible leakage.

2.3.1 Fusion DSP domain

Fusion DSP is part of real-time domain (RTD) and runs at the same core voltage as CM33. Similar to LPAV domain, this is also considered a slave domain and does not have its own power modes but follows M33. This domain comes up as "disabled" until it is explicitly enabled by M33 during boot.

2.3.2 Memory system—real-time domain

2.3.2.1 Internal memory—real-time domain

The real-time domain contains 768 KB of SRAM. Each sub-block can be power-gated under software control to optimize power consumption.

2.3.3 Peripherals—real-time domain

2.3.3.1 Analog—real-time domain

The i.MX 8ULP Real-Time Domain implements the following analog peripherals:

- 12-bit Analog to Digital Converter
- 12-bit Digital to Analog Converter
- Comparators

See i.MX 8ULP modules list for more details.

2.3.3.2 Connectivity and communications—real-time domain

The i.MX 8ULP Real-Time Domain implements the following connectivity and communications peripherals:

- Low Power Universal Asynchronous Receiver/Transmitter (LPUART)
- Low Power Inter-Integrated Circuit (LPI2C)
- Low Power Serial Peripheral Interface (LPSPI)
- Rapid General-Purpose Input and Output with 2 Ports (RGPIO2P)
- Flexible Input/Output (FlexIO)
- Flexible Controlled Area Network (FlexCAN)

See the i.MX 8ULP modules list for more details.

3 System control modules

3.1 JTAG—system control

Joint Test Action Group Controller (JTAGC) provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard.

3.2 JTAG device identification register

The device identification register (Device_ID) is 32-bit length register which provides component identification information. For more details, see the device identification register section of i.MX 8ULP Applications Processor Reference Manual for details. This table shows the Device_ID fields for each i.MX 8ULP silicon revision.

Table 4. JTAG device identification register information

Silicon Revision	Version (4 MSBs)	Part Number	Manufacturer Identity	IEEE 1149.1 Requirement (LSB)
A2	0001	1000100011101000	00000001110	1

The contents of the Device_ID register are also mirrored in a SIM register called MIRROR_OF_JTAG_ID_REG (address:2802_A010). See the i.MX8ULPRM for details.

3.3 Oscillators and PLLs

3.3.1 System oscillator (SYS OSC)

The system oscillator (SYS OSC) is a crystal oscillator. The SYS OSC, in conjunction with an external crystal or resonator, generates a reference clock for this chip. It also provides the option for external input bypass clock from the EXTAL signal directly.

3.3.2 Real-Time Clock Oscillator (RTC OSC)

The RTC OSC module provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock for the RTC.

3.3.3 192 MHz Free-Running Oscillator (FRO)

Low Power internal reference clock (IRC) with tuning logic to generate 192 MHz. System defaults to FRO for as initial boot clock.

3.3.4 1 MHz Low-Power Oscillator (LPO)

The Internal Reference Clock (1 MHz) module is an internal oscillator that can generate a reference clock of 1 MHz. The LPO clock is enabled in all modes of operation, including all low power modes.

3.3.5 USB PLL

The USB PLL is embedded in the USB transceiver block. This PLL allows an exact 480 MHz to be generated from a supported reference clock of 24 MHz. The output of this PLL is primarily used for USB operations on USB-OTG0. The USB PLL clock is also made available as a clock source for other peripherals on the device.

3.3.6 Fixed Frequency PLL (Fixed-freq PLL)

In addition to the main clock output, this PLL also includes 4 Phase Fractional Dividers (PFDs) that can generate other clock frequencies. There is one instance of the Fixed-freq PLL (PLL0), which provides clocks for the M33 core, buses, and peripherals in the real-time domain.

3.3.7 Fractional-N PLL (FracN PLL)

The Fractional-N (Frac-N) PLL can generate an output clock 528 MHz from a supported reference clock. In addition to the main clock output, this PLL also includes up to four Phase Fractional Dividers (PFDs) that can generate other clock frequencies. This PLL also supports a tunable clock for audio applications.

3.4 Power Management

The i.MX 8ULP implements multiple options minimizing application power consumption:

- On chip power management including regulators, drivers and switches for flexible power supplies, efficient power consumption and short wake up time
- Multiple power domains and ultra-low power modes allow flexible power saving
- Voltage and frequency scaling in dynamic operating modes
- Software-controlled clock gating for cores and peripherals

3.4.1 Digital PMC

The digital PMC module allows user software to control power modes and of the chip and to optimize power consumption for the level of functionality needed. There are two instances of digital PMC on this chip, one for each main power domain.

3.4.2 Analog power management controller (Analog PMC)

The Analog PMC consists of voltage/current references, core logic supply regulators, memory supply regulators, back and forward biasing regulators, monitors and power switches, etc. There are two Analog PMC subsystems, one associated with the M33 power domain and the other with the A35 power domain.

Table 5. Analog PMC rise and fall trip point specifications

		Rise			Fall		
	Fuse setting	Min	Typ	Max	Min	Typ	Max
LVD1	0x3	0.805	0.825	0.845	0.78	0.8	0.82
LVD2	0x7	0.908	0.928	0.948	0.88	0.9	0.92
LVD3	0x7	0.98	0.928	0.948	0.88	0.9	0.92

Table continues on the next page...

Table 5. Analog PMC rise and fall trip point specifications (continued)

		Rise			Fall		
	Fuse setting	Min	Typ	Max	Min	Typ	Max
HVD1		1.232	1.252	1.272	1.209	1.229	1.249
HVD2		1.232	1.252	1.272	1.209	1.229	1.249
HVD3		1.232	1.252	1.272	1.209	1.229	1.249

4 System specifications

4.1 Ratings

4.1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	-55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-1000	+1000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-250	+250	V	2

1. Determined according to JEDEC Standard JS-001, *JOINT JEDEC/ESDA STANDARD FOR ELECTROSTATIC DISCHARGE SENSITIVITY TEST - HUMAN BODY MODEL (HBM) - COMPONENT LEVEL*.
2. Determined according to JEDEC Standard JS-002, *ESDA/JEDEC JOINT STANDARD FOR ELECTROSTATIC DISCHARGE SENSITIVITY TESTING – CHARGED DEVICE MODEL (CDM) – DEVICE LEVEL*.

4.1.4 Absolute maximum ratings

CAUTION

Stresses beyond those listed under this table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE

Any reference to VDD or V_{DD} throughout the document corresponds to VDD_DIG0, VDD_DIG1 or VDD_DIG2, depending on where the module resides physically.

Table 6. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Unit
BBSM domain LDO supply input	VDD_VBAT42	-0.3	4.5	V
M33/A35 PMC and PMC IO supply input	VDD_PMC18	-0.3	1.98	V
1.8V IO supply reference and A35 supply reference input	VDD18_IOREF_1/2	-0.3	1.98	V
Real-time domain LDO and internal memory LDO supply input	VDD_PMC18_DIG0	1.14	1.89	V
Real-time domain core (CM33) and logic supply input	VDD_DIG0	-0.3	1.155	V
Application domain core (CA35) and logic supply inputs	VDD_DIG1	-0.3	1.155	V
GPIO Port A supply input	VDD_PTA	-0.3	3.96	V
GPIO Port B supply input	VDD_PTB	-0.3	1.98	V
GPIO Port C supply input	VDD_PTC	-0.3	3.96	V
GPIO Port D supply input	VDD_PTD	-0.3	3.96	V
GPIO Port E supply input	VDD_PTE	-0.3	3.96	V
GPIO Port F supply input	VDD_PTF	-0.3	3.96	V
DDR I/O supply input (output driver)	VDDQ_DDR	-0.3	1.2	V
DDR pre-driver supply input	VDDQX_DDR	-0.3	1.2	V
I/O supply for CKE and RESET_N pads.	VDDQX_AO_DDR	-0.3	1.2	V
PLL 1.0 V supply	VDD_DDR_PLL	-0.3	1.1	V
MIPI DSI 1.1V supply input	VDD_DSI11	-0.3	1.155	V
MIPI DSI 1.8V supply input	VDD_DSI18	-0.3	1.98	V
USB PHY 3.3V supply input	VDD_USB33	-0.3	3.6	V
USB PHY 1.8V supply input	VDD_USB18	-0.3	1.98	V
USB0 VBUS detection	USB0_VBUS_DETECT	-0.3	5.6	V
USB1 VBUS detection	USB1_VBUS_DETECT	-0.3	5.6	V
PLL analog supply input	VDD_PLL18	-0.3	1.98	V
ADC high reference supply input	VREFH_ANA18	-0.3	1.98	V

Table continues on the next page...

Table 6. Absolute maximum ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ADC analog and IO 1.8V supply input	VDD_ANA18	-0.3	1.98	V
ADC analog and IO 3.3V or 1.8V supply input	VDD_ANA33	-0.3	3.96	V

4.1.5 Recommended operating conditions—system

Table 7. Recommended operating conditions[1]

Symbol	Description	Conditions	Min	Typ	Max	Units
BBSM (Always On) Domain Supply Voltage Requirements						
VDD_VBAT42	BBSM domain LDO supply input	—	2.4	3.0	4.5	V
VDD_VBAT18_CAP	BBSM domain LDO output	—	—	1.8	—	V
Real Time Domain (M33 domain) Supply Voltage Requirements						
VDD_PMC18	M33/A35 PMC and PMC IO supply input	—	1.71	1.8	1.89	V
VDD_FUSE18	eFuse supply input	—	1.71	1.8	1.9	V
VDD18_IOREF_1	1.8V IO supply reference and A35 supply reference input	—	1.71	1.8	1.89	V
VDD18_IOREF_2	1.8V IO supply reference and A35 supply reference input	—	1.71	1.8	1.89	V
VDD_PMC18_DIG0[2]	M33 domain LDO supply input	—	1.14	1.2	1.89	V
VDD_PMC11_DIG0_CAP[3]	M33 domain LDO supply output	—	0.65	—	1.1	V
Real Time Domain (M33 domain) PMC 0 Register Configuration Requirements						
<PMC register for Active Mode>	PMC0 Active mode LDO configuration requirement	Active mode AFBB[4]=VDD	1.0	—	1.15	V
<PMC register for Active Mode>	PMC0 Active mode LDO Bypass	Active mode AFBB=VDD	1.0	—	1.15	V
<PMC register for Active Mode>	PMC0 Active mode LDO configuration requirement	Active mode ARBB[5]=1.3 V	0.9	—	1.15	V
<PMC register for Active Mode>	PMC0 Active mode LDO Bypass	Active mode ARBB=1.3 V	0.9	—	1.15	V
<PMC register for Sleep Mode>	PMC0 Sleep Mode	Sleep mode AFBB=VDD	1.0	—	1.15	V
<PMC register for Deep Sleep Mode>	PMC0 Deep Sleep Mode	Deep Sleep mode RBB[6]=Optional	0.65	—	—	V
<PMC register for Power Down Mode>	PMC0 Power Down Mode	Power Down mode	0.65	—	—	V

Table continues on the next page...

Table 7. Recommended operating conditions[1] (continued)

Symbol	Description	Conditions	Min	Typ	Max	Units
		RBB=Enabled				
RDIG0	External board routing impedance from VDD_PMC11_DIG0_CAP to VDD_DIG0	—	—	—	50	mΩ
Application Domain (A35 domain) Supply Voltage Requirements						
VDD_DIG1 [7] VDD_DSI11[8]	Application domain core (CA35) and logic supply inputs MIPI DSI 1.1V supply input	Active mode AFBB=VDD	1.0	—	1.15	V
		Sleep mode AFBB=VDD	1.0	—	1.15	V
		Deep Sleep mode RBB=Optional	0.65	—	—	V
		Power Down mode RBB=Enabled	0.65	—	—	V
GPIO Supplies						
VDD_PTA[9,10]	FSGPIO Port A supply input (low voltage range)	—	1.71	1.8	1.98	V
	FSGPIO Port A supply input (high voltage range)	—	3.0	3.3	3.6	V
	FSGPIO Port A supply input (continuous voltage range, derated2)	—	1.71		1.98	V
	FSGPIO Port A supply input (continuous voltage range, derated)	—	1.98		2.7	V
	FSGPIO Port A supply input (continuous voltage range, normal)	—	2.7		3.6	V
VDD_PTB	FSGPIO Port B supply input (low voltage range)	—	1.71	1.8	1.98	V
	FSGPIO Port B supply input (continuous voltage range, derated2)	—	1.71		1.98	V
VDD_PTC	STGPIO Port C supply input (low-voltage range)	—	1.65	1.8	1.95	V
	STGPIO Port C supply input (high voltage range)	—	2.7	3.3	3.6	V

Table continues on the next page...

Table 7. Recommended operating conditions[1] (continued)

Symbol	Description	Conditions	Min	Typ	Max	Units
VDD_PTD	STGPIO Port D supply input (low-voltage range)	—	1.65	1.8	1.95	V
	STGPIO Port D supply input (high voltage range)	—	2.7	3.3	3.6	V
VDD_PTE	FSGPIO Port E supply input (low voltage range)	—	1.71	1.8	1.98	V
	FSGPIO Port E supply input (high voltage range)	—	3.0	3.3	3.6	V
	FSGPIO Port E supply input (continuous voltage range)	—	1.71	—	1.98	V
	FSGPIO Port E supply input (continuous voltage range, derated2)	—	1.98	—	2.7	V
	FSGPIO Port E supply input (continuous voltage range, derated)	—	2.7	—	3.6	V
VDD_PTF [11]	FSGPIO Port F supply input (low voltage range, normal)	—	1.71	1.8	1.98	V
	FSGPIO Port F supply input (high voltage range)	—	3.0	3.3	3.6	V
	FSGPIO Port F supply input (continuous voltage range, derated2)	—	1.71	—	1.98	V
	FSGPIO Port F supply input (continuous voltage range, derated)	—	1.98	—	2.7	V
	FSGPIO Port F supply input (continuous voltage range, normal)	—	2.7	—	3.6	V
Peripheral/Interface Supplies						
VDDQ_DDR	DDR I/O supply input (output driver): LPDDR3	—	1.14	1.2	1.3	V
	DDR I/O supply input (output driver): LPDDR4	—	1.06	1.1	1.17	V
	DDR I/O supply input (output driver): LPDDR4x	—	0.57	0.6	0.65	V
VDDQX_DDR	DDR I/O supply input (pre-driver): LPDDR3	—	1.14	1.2	1.3	V
	DDR I/O supply input (pre-driver): LPDDR4	—	1.06	1.1	1.17	V
	DDR I/O supply input (pre-driver): LPDDR4x	—	1.06	1.1	1.17	V
VDDQX_AO_DDR	DDR I/O supply for CKE and RESET_N pads: LPDDR3	—	1.14	1.2	1.3	V

Table continues on the next page...

Table 7. Recommended operating conditions[1] (continued)

Symbol	Description	Conditions	Min	Typ	Max	Units
	DDR I/O supply for CKE and RESET_N pads: LPDDR4	—	1.06	1.1	1.17	V
	DDR I/O supply for CKE and RESET_N pads: LPDDR4x	—	1.06	1.1	1.17	V
VDD_DDR_PLL	DDR PLL 1.0 V supply	—	0.65	1.0	1.15	V
VDD_DSI11	MIPI DSI 1.1V supply input	—	0.8	1.1	1.155	V
VDD_DSI18	MIPI DSI 1.8V supply input	—	1.71	1.8	1.89	V
VDD_CSI11[12]	MIPI CSI 1.1 V supply input	—	0.8	1.1	1.155	V
VDD_CSI18	MIPI CSI 1.8V supply input	—	1.71	1.8	1.89	V
VDD_USB33	USB PHY 3.3V supply input	—	3.0	3.3	3.6	V
VDD_USB18	USB PHY 1.8V supply input	—	1.71	1.8	1.89	V
USB0_VBUS_DETECT	USB0 VBUS detection	—	4.0[13] or 3.0[14]	5.0	5.5	V
USB1_VBUS_DETECT	USB1 VBUS detection	—		5.0	5.5	V
Analog Supplies						
VDD_PLL18	PLL analog supply input	—	1.71	1.8	1.89	V
VREFH_ANA18	ADC high reference supply input	—	1.71	1.8	1.89	V
VREFL_ANA	ADC low reference supply input	—	0	0	0	V
VDD_ANA18	ADC analog and IO 1.8V supply input	—	1.71	1.8	1.89	V
VDD_ANA33	ADC analog and IO 3.3V or 1.8V supply input	—	1.71	1.8 or 3.3	3.6	V

1. All supply inputs shown represent the voltage at the package ball.
2. If VDD_PMC18_DIG0 is operated at 1.8 V, it should be tied to VDD_PMC18 at the board level.
3. In M33 LDO bypass mode, LDO_EN should be tied to GND. It would be better to add 10k pull down on VDD_PMC18_DIG0 and VDD_PMC11_DIG0_CAP. Also, in LDO bypass mode, VDD_DIG0 should be driven by PMIC or external power supply. In M33 LDO enable mode, LDO_EN should be pulled up to VDD_PMV18. VDD_PMC11_DIG0_CAP should be connected to VDD_DIG0 at the board-level. The voltage observed at VDD_PMC11_DIG0_CAP differs from the from the programmed voltage on the internal LDO because the sense point for the LDO is on-chip.
4. Asymmetric Forward Body Bias; see the Power Management chapter in i.MX 8ULP Reference Manual for details.
5. Asymmetric Reverse Body Bias; see the Power Management chapter in i.MX 8ULP Reference Manual for details.
6. Reverse Body Bias; see the Power Management chapter in i.MX 8ULP Reference Manual for details.
7. VDD_DIG1 and VDD_DIG2 should be shorted together at the board-level.
8. VDD_DSI11 and VDD_DSI18 should be powered even if MIPI DSI is not used..
9. VDD_PTA must be powered during a power-on reset (POR) for the CMC0 Mode register (MR) BOOTCFG and BOOTMODE field to properly latch the boot configuration and boot mode from the PTA and BOOT_MODE signals.
10. VDD_ANA33 must be shorted to VDD_PTA at the board level.
11. VDD_PTF must be powered during a power-on reset (POR) for the SMC1 Mode register (MR) BOOTCFG field to properly latch the boot configuration from the PTF signals (GPIO Boot mode).
12. If the MIPI CSI is used, VDD_CSI11 must be connected to VDD_DIG1 at board level. If MIPI CSI is not used, VDD_CSI11 can be connected to ground through a 10KΩ resistor.
13. The i.MX 8ULP USB PHY provides two options for reporting VBUS valid back to the USB controller:
    - A programmable internal VBUS_VALID comparator (the default option), or

- An alternate VBUS_VALID_3V detector that will report VBUS valid for voltages above 3 V

14. The i.MX 8ULP USB PHY provides two options for reporting VBUS valid back to the USB controller:
    - A programmable internal VBUS_VALID comparator (the default option), or
    - An alternate VBUS_VALID_3V detector that will report VBUS valid for voltages above 3 V.

4.1.6 Thermal specifications

4.1.6.1 Thermal operating requirements

Table 8. Thermal operating requirements

Symbol	Parameter	Min.	Max.	Unit
T_j	Die junction temperature—Commercial	-	95	°C
T_a	Die ambient temperature—Commercial	0	-	°C

4.1.6.2 Thermal attributes

Table 9. Thermal resistance data

Rating	Board type[1]	Symbol	15x15 mm Package Value	9.4 x 9.4 mm Package Value	Unit
Junction to Ambient Thermal Resistance[2]	Four-layer board, 2s2p	$R_{\theta JA}$	21.4	20	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	Four-layer board, 2s2p	Ψ_{JT}	0.4	0.1	°C/W
Junction to Case Thermal Resistance[3]	Single-layer board (1S)	$R_{\theta JC}$	7.1	4.2	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9). PCB has 89 thermal vias under the die shadow area.
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
3. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature is the surface temperature of package top side.

NOTE

Non-uniform power was applied on to the die.

4.2 System clocks

4.2.1 Clock modules

4.2.1.1 Oscillator electrical specifications

4.2.1.1.1 Oscillator DC electrical specifications

Table 10. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{EXTAL}	EXTAL input voltage — external clock mode	0	—	V_{DD}	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
I_{DD}	Current consumption (high-gain mode)	—	2	—	mA	
	Current consumption (low-power mode)	—	1	—	mA	
C_x	EXTAL load capacitance	—	—	—		1
C_y	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor — low-power mode (HGO=0)	—	—	—	MΩ	1 2
	Feedback resistor — high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-power mode (HGO=0)	—	0	—	Ω	
	Series resistor — high-gain mode (HGO=1)					
V_{pp} [3]	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.8	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	0.75 x VDD_PMC18	0.8 x VDD_PMC18	—	V	

1. See crystal or resonator manufacturer's recommendation
2. When low power mode is selected, R_F is integrated and must not be attached externally.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

4.2.1.1.2 System oscillator frequency specifications

Table 11. System oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode	4	24	32	MHz
t_{dc_extal}	Input clock duty cycle (external clock mode)	49		51	%
t_{start}	Start-up time (if 24MHz used only, high gainand low power mode	—	0.2	—	ms

4.2.1.2 32 kHz oscillator electrical specifications

4.2.1.2.1 32 kHz oscillator DC electrical specifications

Table 12. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	1.5	2.0	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

4.2.1.2.2 32 kHz oscillator frequency specifications

Table 13. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	500	—	ms	[1]
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	[2], [3]

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

4.2.1.3 Free-running oscillator FRO-192M specifications

Table 14. FRO-192M specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$f_{fro192m}$	FRO-192M frequency (nominal)		192		MHz
$\Delta f_{fro192m}$	Frequency deviation • 1T trim (Open loop)	—	—	±1.5	% %
$t_{startup}$	Start-up time	—	70	—	µs
jit_{cyc}	Cycle to cycle jitter	—	105	—	ps
$I_{fro192m}$	Current consumption	—	40	50	µA

NOTE

Any divided versions of the FRO that are not being used anywhere should be turned off to save power.

4.2.1.4 LPO 1 MHz oscillator specifications

Parameter	Min.	Typ.	Max.	Unit
Frequency	—	1 (+10,-20%%)	—	MHz
Duty cycle	—	50% (±5%)	—	
Start-up time	—	85 (±20%)	—	µs
Current	—	1.25	—	µA

4.2.2 Core, platform, and system bus clock frequency

4.2.2.1 Maximum operating frequencies

Table 15. Maximum operating frequencies[1], [2]

Power Domain	Min. Voltage (V)[3]	Maximum[4] Frequency	Biasing setting
Cortex A35	1.05	800 MHz	AFBB enabled
	1.0	650 MHz	
Cortex M33/Fusion	1.05	216/200 MHz	AFBB enabled
	1.0	127/127 MHz	
	0.9	38.4/38.4 MHz	ARBB enabled
VBAT	—	32 kHz	AFBB enabled

1. All Peripherals to support a core voltage of 0.8V-1.15V.
2. Retention mode (shared memory retained) can still be supported at a lower voltage (0.65 V)
3. Voltage at the pin
4. All values are subject to change

Table 16. Clock frequencies

Clock name	Voltage range at the pin		
	1.05 V	1.0 V	0.9 V w/ARBB
CM33_BUSCLK	108	65	20
CM33_SLOWCLK	24	20	12.5
DSP CORECLK	200	150	50
DSP_BUSCLK	100	75	25
DSP_SLOWCLK	33	33	24
FlexSPI0	177	99	48
FlexSPI1	177	99	48
LPUART0	60	60	48
LPI2C0	60	60	48
LPSPI0	60	60	48

Table continues on the next page...

Table 16. Clock frequencies (continued)

Clock name	Voltage range at the pin		
	1.05 V	1.0 V	0.9 V w/ARBB
I3C0	25	25	24
FlexCAN0	40	40	32
FLEXIO	80	50	32
SAI	50	50	24
LPIT0	60	60	32
WDOG0	24	24	24
ADC0	60	60	32
LPTPM0	60	60	32
TPIU	100	50	24
SWO	100	50	24
NIC_AP_CLK	452	328	—
NIC_PER_CLK	226	164	—
XBAR_AP_CLK	226	164	—
XBAR_BUS_CLK	113	82	—
AD_SLOW_CLK	37.7	27.3	—
uSDHC0	198	99	—
uSDHC1-PTD	164	82	—
uSDHC1-PTE/F	99	48	—
uSDHC2-PTD	82	41	—
uSDHC2-PTF	99	48	—
USB	480	480	—
ENET	198	198	—
FlexSPI2-PTD	164	82	—
FlexSPI2-PTE	99	48	—
LPUART4	60	60	—
LPI2C4	60	60	—
LPSPI4	125	96	—
I3C2	25	25	—
FLEXIO1	80	50	—
LPTPM4	60	60	—
LPIT1	60	60	—

Table continues on the next page...

Table 16. Clock frequencies (continued)

Clock name	Voltage range at the pin		
	1.05 V	1.0 V	0.9 V w/ARBB
WDOG	25	25	—
SAI1	50	50	—
HIFI4_CLK	475	264	—
NIC_HIFI4_CLK	238	132	—
NIC_LPAV_AXI_CLK	316.8	198	—
NIC_LPAV_AHB_CLK	158.4	96	—
LPAV_BUS_CLK	79.2	48	—
DDR_CLK	266[1], [2]	200	—
DDR PHY	528[1]	400	—
GPU3D	288	198	—
GPU2D	288	198	—
DCNano	105	75	—
MIPI CSI	140	140	—
MIPI CSI UI	93	93	—
ISI	93	93	—
MIPI CSI ESC	80	50	—
EPDC	297	198	—
WDOG5	20	20	—
LPTPM8	60	60	—

1. Supported only for LPDDR4/4x
2. The PLL4 PFD0 PLL output clock maximum frequency when VDD_DIG2 = 1.0 V nominal is 528 MHz. The PLL2_VCO output clock maximum frequency when VDD_DIG1 = 1.0 V nominal is 725 MHz. When VDD_DIG0, VDD_DIG1 or VDD_DIG2 is at 0.9 V nominal, the fastest selectable clock source available is the FRO192 for the corresponding domain

4.3 Power sequencing—system

4.3.1 Power-on sequencing

The power-on sequencing requirements for the device are described in this section.

VBAT Domain Power Supply

VDD_VBAT42 must be powered and stable before all other supplies begin to ramp up.

Real-Time Domain Power Supplies

The Real-Time Domain supplies must be powered and stable before RESET0_B is deasserted. The real-time domain supplies listed below may be powered on in any order except for those indicating specific sequencing requirements.

- When RTD is being powered by internal M33 LDO(LDO_ENABLE pin is pulled up to VDD_PMC18), VDD_PMC18_DIG0 and VDD_PMC18 must be powered on together, or VDD_PMC18 must be powered on first followed by VDD_PMC18_DIG0. VDD18_IOREF_1/2 must be powered up together with VDD_PMC18.
- VDD_PTA and VDD_PTB must be powered no later than VDD_PMC18_DIG0 ramp up.
- VDD_ANA18 must be powered on before or at same time of VDD_PMC18.
- VDD_FUSE18
- VDD_PLL18
- VREFH_ANA18
- VREFL_ANA
- VDD_ANA33

When RTD is being powered by an external PMIC power supply rail(LDO_ENABLE pin is tied to 0):

The VDD_PMC18_DIG0 and VDD_PMC11_DIG0_CAP should be shorted to GND with 10KOhm.

- VDD_PMC18 and VDD18_IOREF_1/2 must be powered up together.
- VDD_ANA18 must be powered on before or at same time of VDD_PMC18
- VDD_FUSE18
- VDD_PLL_18
- VREFH_ANA18
- VREFL_ANA
- VDD_ANA33
- VDD_DIG0
- VDD_PTA and VDD_PTB must be powered before VDD_ DIG0 ramp up

Application and Low Power Audio Video Domain Power Supplies

For Single and Dual Boot options, the Application and Low Power Audio Video Domain power supplies must be powered on and stable before the CA35 core exits reset.

For LP boot, this is handled by uPower FW that communicates with PMIC to enable all power supplies on demand

The application domain supplies listed below may be powered on in any order except for those indicating specific sequencing requirements.

- VDD_DIG1
- VDD_PTE and VDD_PTF must be powered before VDD_ DIG1 ramp up.
- VDD_DIG2 must be powered together with VDD_DDR_PLL
- VDDQX_AO and VDDQX must be powered together or after VDD_DIG2 and VDD_DDR_PLL.
- VDD_DIG2 and VDD_DDR_PLL need to kept at same voltage levels during system operation.
- The VDDQ must be powered together with VDDQX_AO and VDDQX or after them.
- VDD_PTD: VDD18_IOREF_1/2 must be powered on before VDD_PTD
- VDDQX must always be greater than or equal to VDDQ.
- MIPI_DSI18
- MIPI_CSI18
- MIPI_DSI11 (MIPI_DSI_11 should be shorted to VDD_DIG2 when used)
- MIPI_CSI11

- VDD_USB0_18
- VDD_USB0_33
- VDD_USB1_18
- VDD_USB1_33

The following figure shows the power-on sequence.

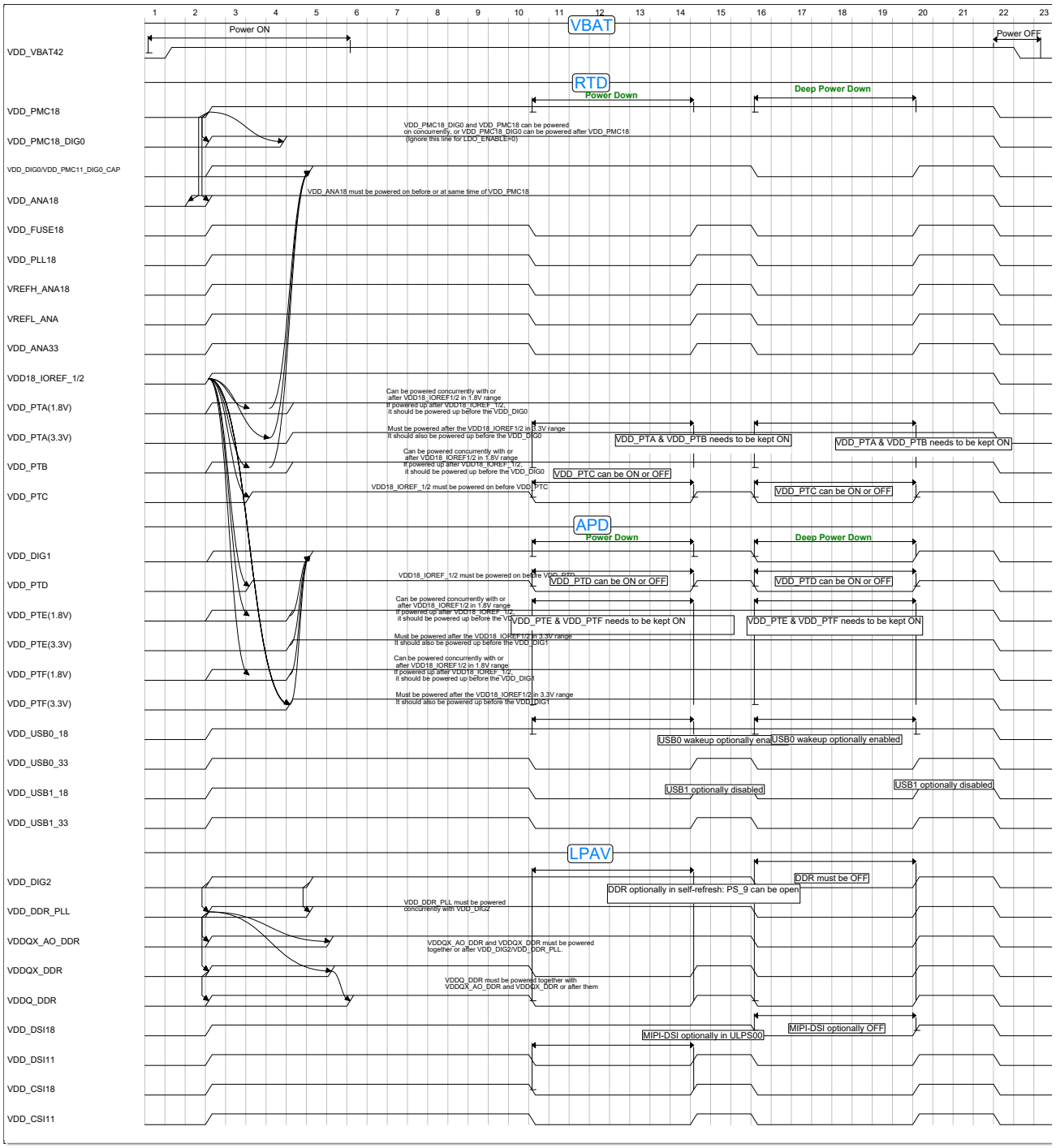


Figure 3. Power-on sequence

4.3.2 Power down sequencing

As a rule, reverse the order detailed above. Pay attention for the VDD_PTC and VDD_PTD being powered OFF before the VDD18_IOREF_1/2 being powered OFF.

4.4 Requirements for unused interfaces

This table shows the required connections for unused interfaces. See i.MX 8ULP Hardware Developers Guide, for details.

Table 17. Required connections for unused interfaces

Module	Supply Name	Description	Recommendations if module is unused
ADC	VREFH_ANA18	High Reference supply for ADC	10 kΩ resistor to ground
	VREFL_ANA	Low Reference supply for ADC	Must be powered
	VDD_ANA18	1.8 V supply for ADC Analog and IO segment	Must be powered
	VDD_ANA33	ADC analog and IO 3.3 V or 1.8 V supply input	10 kΩ resistor to ground
DAC	DAC0_OUT	DAC0 output	Leave unconnected
	DAC1_OUT	DAC1 output	Leave unconnected
MIPI DSI	VDD_DSI11	MIPI 1.1 V supply	Must be powered
	VDD_DSI18	MIPI 1.8 V supply	Must be powered
	DSI_CLK_N	MIPI Negative Clock Signal	Leave unconnected
	DSI_CLK_P	MIPI Positive Clock Signal	Leave unconnected
	DSI_DATA0_N	MIPI Negative Data0 Signal	Leave unconnected
	DSI_DATA0_P	MIPI Positive Data0 Signal	Leave unconnected
	DSI_DATA1_N	MIPI Negative Data1 Signal	Leave unconnected
	DSI_DATA1_P	MIPI Positive Data1 Signal	Leave unconnected
	DSI_DATA2_N	MIPI Negative Data2 Signal	Leave unconnected
	DSI_DATA2_P	MIPI Positive Data2 Signal	Leave unconnected
	DSI_DATA3_N	MIPI Negative Data3 Signal	Leave unconnected
	DSI_DATA3_P	MIPI Positive Data3 Signal	Leave unconnected
MIPI CSI	VDD_CSI11	MIPI 1.1 V supply	10 kΩ resistor to ground
	VDD_CSI18	MIPI 1.8 V supply	10 kΩ resistor to ground
	CSI_CLK_N	MIPI Negative Clock Signal	Leave unconnected
	CSI_CLK_P	MIPI Positive Clock Signal	Leave unconnected
	CSI_DATA0_N	MIPI Negative Data0 Signal	Leave unconnected
	CSI_DATA0_P	MIPI Positive Data0 Signal	Leave unconnected
	CSI_DATA1_N	MIPI Negative Data1 Signal	Leave unconnected
	CSI_DATA1_P	MIPI Positive Data1 Signal	Leave unconnected

Table continues on the next page...

Table 17. Required connections for unused interfaces (continued)

Module	Supply Name	Description	Recommendations if module is unused
	CSI_DATA2_N	MIPI Negative Data2 Signal	Leave unconnected
	CSI_DATA2_P	MIPI Positive Data2 Signal	Leave unconnected
	CSI_DATA3_N	MIPI Negative Data3 Signal	Leave unconnected
	CSI_DATA3_P	MIPI Positive Data3 Signal	Leave unconnected
Port A Signals	VDD_PTA	Port A supply	Must be powered
Port B Signals	VDD_PTB	Port B 1.8 V supply	Must be powered
Port C Signals	VDD_PTC	Port C supply	10 kΩ resistor to ground
Port D Signals	VDD_PTD	Port D supply	10 kΩ resistor to ground
Port E Signals	VDD_PTE	Port E supply	Must be powered
Port F Signals	VDD_PTF	Port F supply	Must be powered
USB0	VDD_USB33	USB0 PHY 3.3 V supply	Must be powered
	VDD_USB18	USB0 PHY 1.8 V supply	Must be powered
	USB0_DM	USB D- Analog Data Signal on the USB Bus	Leave unconnected
	USB0_DP	USB D+ Analog Data Signal on the USB Bus	Leave unconnected
	USB0_VBUS_DETECT	USB0 VBUS Detect	10 kΩ resistor to ground
USB1	VDD_USB33	USB1 PHY 3.3 V supply	Must be powered
	VDD_USB18	USB1 PHY 1.8 V supply	Must be powered
	USB1_DM	USB D- Analog Data Signal on the USB Bus	Leave unconnected
	USB1_DP	USB D+ Analog Data Signal on the USB Bus	Leave unconnected
	USB1_VBUS_DETECT	USB1 VBUS Detect	10 kΩ resistor to ground

4.5 Electrical Characteristics and Thermal Specifications

4.5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

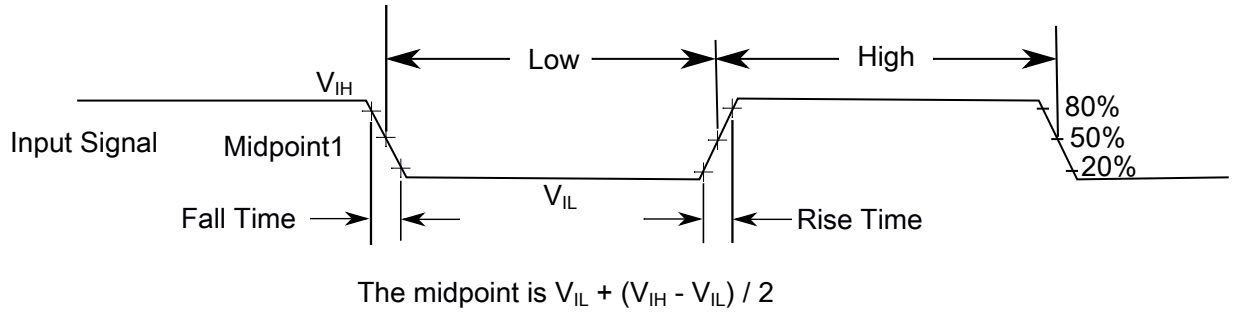


Figure 4. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
   - have C_L=15 pF loads,
   - are slew rate disabled, and
   - are normal drive strength

4.5.2 Nonswitching electrical characteristics

4.5.2.1 GPIO DC Electrical Requirements

Table 18. STGPIO DC electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{oh}	High-level output voltage	Ioh= -0.1mA DSE=1	0.8*VDD_PTx	—	—	V
		Ioh= -2mA DSE=0	0.8*VDD_PTx	—	—	V
V_{ol}	Low-level output voltage	Iol= 0.1mA DSE=1	—	—	0.125*VDD_PTx	V
		Iol= 2mA DSE=0	—	—	—	V
V_{ih}	High-level input voltage	—	0.7*VDD_PTx	—	VDD_PTx	V
V_{il}	Low-level input voltage	—	0	—	0.3*VDD_PTx	V
I_{in}	Input current (no PU/PD)	VI = 0, VI = VDD_PTx PUN = "H", PDN = "H"	-1	—	1	uA

Table 19. FailSafe GPIO (FSGPIO) DC Electrical Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{oh}	High-level output voltage	Ioh= -10mA (Normal Voltage Range) Ioh=-6mA (Derated Voltage Range) Ioh=-5mA (Derated2 Voltage Range) Ioh=-10mA (Low Voltage Range) Ioh=-10mA (High Voltage Range) DSE=1	VDD_PTx-0.5	—	—	V
		Ioh= -5mA (Normal Voltage Range) Ioh=-3mA (Derated Voltage Range) Ioh=-2.5mA (Derated2 Voltage Range) Ioh=-5mA (Low Voltage Range) Ioh=-5mA (High Voltage Range) DSE=0	VDD_PTx-0.5	—	—	V
V_{ol}	Low-level output voltage	Iol= 10mA (Normal Voltage Range) Iol=6mA (Derated Voltage Range) Iol=5mA (Derated2 Voltage Range) Iol=10mA (Low Voltage Range) Iol=10mA (High Voltage Range) DSE=1	—	—	0.5	V
		Iol= 5mA (Normal Voltage Range) Iol=3mA (Derated Voltage Range) Iol=2.5mA	—	—	0.5	V

Table continues on the next page...

Table 19. FailSafe GPIO (FSGPIO) DC Electrical Requirements (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(Derated2 Voltage Range) Iol=5mA (Low Voltage Range) Iol=5mA (High Voltage Range) DSE=0				
V_{ih}	High-level input voltage	All Voltage Range	0.75*VDD18_IOREF_x	__	VDD_PTx	V
V_{il}	Low-level input voltage	All Voltage Range	0	__	0.3*VDD18_IOREF_x	V
I_{in}	Input current (no PU/PD)	VI = 0, VI = VDD_PTx PUN = "H", PDN = "H"	-1	__	1	uA

4.5.2.1.1 GPIO Pull-up and Pull-Down Resistance

Table 20. Failsafe GPIO (FSGPIO) pull-up and pull-down resistance (PTA, PTB, PTE and PTF)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
R Pull up	Pull-up resistance	25	--	50	kΩ	1
R Pull down	Pulldown resistance	25	--	50	kΩ	1

1. Failsafe GPIOs (FSGPIO) are used on ports A, B, E, and F.

Table 21. Standard GPIO (STGPIO) pull-up and pull-down resistance (PTC, PTD)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
R Pull up	Pull-up resistance high voltage range (2.7 V – 3.6 V)	10	--	100	kΩ	1
	Pull-up resistance low voltage range (1.71 V – 1.89 V)	20	--	50	kΩ	
R Pull down	Pulldown resistance high voltage range (2.7 V – 3.6 V)	10	--	100	kΩ	1
	Pulldown resistance high	20	--	50	kΩ	

Table continues on the next page...

Table 21. Standard GPIO (STGPIO) pull-up and pull-down resistance (PTC, PTD) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	voltage range (1.71 V – 1.89 V)					

1. Standard GPIOs (STGPIO) are used on Port C and Port D.

4.5.3 Capacitance attributes

See the device IBIS model for pin capacitance values for the package being used.

4.6 Switching electrical characteristics

4.6.1 General switching timing specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timer functions.

Table 22. General switching timing specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
tw_GPIO_sync	GPIO pin interrupt pulse width (Digital Filter disabled) — Synchronous path	1.5	—	—	Bus clock cycles [1]	[2]
tw_RESET_async	External RESET and NMI pin interrupt pulse width — Asynchronous path	30	—	—	ns	[3]
tw_GPIO_async	GPIO pin interrupt pulse width — Asynchronous path	30	—	—	ns	[3]

1. See the Clocking chapter in i.MX 8ULP Reference Manual for details.
2. The greater synchronous and asynchronous timing must be met.
3. This is the shortest pulse that is guaranteed to be recognized.

4.6.2 GPIO rise and fall times

Table 23. FSGPIO rise and fall times

Symbol	Parameter	Condition			Min	Typ	Max	Unit
t_{rf}	transition time	Continuous Voltage Range Normal VDD_PTx = 2.7 - 3.6 V	CL=15pF	Slow Slew Rate, High Drive Strength	--	2.2176	5.3834	ns
				Standard Slew Rate, High Drive Strength	--	0.509	1.0907	ns
				Slow Slew Rate, Standard Drive Strength	--	2.9165	6.3051	ns
				Standard Slew Rate, Standard Drive Strength	--	0.6188	1.3144	ns

Table continues on the next page...

Table 23. FSGPIO rise and fall times (continued)

Symbol	Parameter	Condition			Min	Typ	Max	Unit
t_{rf}	transition time	Continuous Voltage Range Derated VDD_PTx = 1.98 - 2.7 V	CL=15pF	Slow Slew Rate, High Drive Strength	--	1.8083	4.2001	ns
				Standard Slew Rate, High Drive Strength	--	0.347	1.1157	ns
				Slow Slew Rate, Standard Drive Strength	--	2.4988	4.7943	ns
				Standard Slew Rate, Standard Drive Strength	--	0.4346	0.7815	ns
t_{rf}	transition time	Continuous Voltage Range Derated2 VDD_PTx = 1.71 - 1.98 V	CL=15pF	Slow Slew Rate, High Drive Strength	--	1.5285	3.0727	ns
				Standard Slew Rate, High Drive Strength	--	0.2984	0.4355	ns
				Slow Slew Rate, Standard Drive Strength	--	2.1201	3.5707	ns
				Standard Slew Rate, Standard Drive Strength	--	0.3569	0.6338	ns
t_{rf}	transition time	High Voltage Range VDD_PTx = 3.0 - 3.6 V	CL=15pF	Slow Slew Rate, High Drive Strength	--	2.3523	5.5195	ns
				Standard Slew Rate, High Drive Strength	--	0.6938	1.5374	ns
				Slow Slew Rate, Standard Drive Strength	--	3.02	6.6893	ns
				Standard Slew Rate, Standard Drive Strength	--	0.8121	1.6844	ns
t_{rf}	transition time	Low Voltage Range VDD_PTx = 1.71 - 1.98 V	CL=15pF	Slow Slew Rate, High Drive Strength	--	1.4732	3.1865	ns
				Standard Slew Rate, High Drive Strength	--	0.2944	0.4472	ns

Table continues on the next page...

Table 23. FSGPIO rise and fall times (continued)

Symbol	Parameter	Condition			Min	Typ	Max	Unit
				Slow Slew Rate, Standard Drive Strength	--	2.0494	3.6952	ns
				Standard Slew Rate, Standard Drive Strength	--	0.3523	0.636	ns

Table 24. STGPIO rise and fall times

Symbol	Parameter	Condition			Min	Typ	Max	Unit
t_{rf}	transition time	High Voltage Range VDD_PTx = 2.7 - 3.6 V	CL=15pF	Standard Slew Rate, High Drive Strength	--	0.2807	0.3698	ns
				Standard Slew Rate, Standard Drive Strength	--	0.3334	0.437	ns
t_{rf}	transition time	Med Voltage Range VDD_PTx = 1.71 - 1.95 V	CL=15pF	Standard Slew Rate, High Drive Strength	--	0.2346	0.3007	ns
				Standard Slew Rate, Standard Drive Strength	--	0.2538	0.3135	ns
t_{rf}	transition time	Low Voltage Range VDD_PTx = 1.14 - 1.32 V	CL=15pF	Standard Slew Rate, High Drive Strength	--	0.3522	0.6169	ns
				Standard Slew Rate, Standard Drive Strength	--	0.6808	1.7133	ns

4.6.3 GPIO output buffer maximum frequency

Table 25. GPIO output buffer maximum frequency

Symbol	Parameter	Condition	Min	Max	Unit
F_{max} (low drive low slew)	Maximum Frequency	VDD_PTx = 1.71 - 1.95 V, CL = 5pf	—	120	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 10pf	—	100	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 40pf	—	50	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 5pf	—	115	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 10pf	—	95	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 40pf	—	40	MHz

Table continues on the next page...

Table 25. GPIO output buffer maximum frequency (continued)

Symbol	Parameter	Condition	Min	Max	Unit
F_{max} (low drive high slew)	Maximum Frequency	VDD_PTx = 1.71 - 1.95 V, CL = 5pf	—	185	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 10pf	—	145	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 40pf	—	50	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 5pf	—	170	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 10pf	—	130	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 40pf	—	40	MHz
F_{max} (high drive low slew)	Maximum Frequency	VDD_PTx = 1.71 - 1.95 V, CL = 5pf	—	140	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 10pf	—	125	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 40pf	—	85	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 5pf	—	130	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 10pf	—	115	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 40pf	—	70	MHz
F_{max} (high drive high slew)	Maximum Frequency	VDD_PTx = 1.71 - 1.95 V, CL = 5pf	—	235	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 10pf	—	200	MHz
		VDD_PTx = 1.71 - 1.95 V, CL = 40pf	—	100	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 5pf	—	215	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 10pf	—	185	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 40pf	—	80	MHz

4.6.4 GPIO input buffer maximum frequency

Table 26. GPIO input buffer maximum frequency

Symbol	Parameter	Condition	Min	Max	Unit
Input buffer Fmax	Maximum frequency of input buffer	VDD_PTx = 1.71 - 1.95 V, CL = 50 fF	550	—	MHz
		VDD_PTx = 2.7 - 3.6 V, CL = 50 fF	430	—	MHz

4.7 Debug and trace modules

4.7.1 JTAG timing specifications

Table 27. JTAG timing specifications

Symbol	Parameter	Min	Max	Unit
J1	TCLK frequency of operation			
	• Boundary Scan	1	10	MHz
	• JTAG	0	25	MHz
J2	TCLK cycle period	1000/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG	20	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	5	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	10.5	—	ns
J10	TMS, TDI input data hold time after TCLK rise	2.5	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	2	—	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

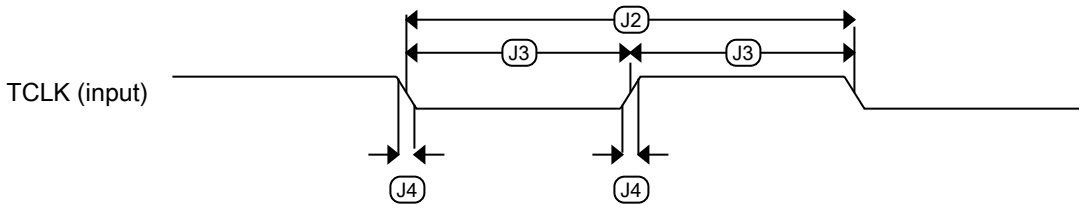


Figure 5. Test clock input timing

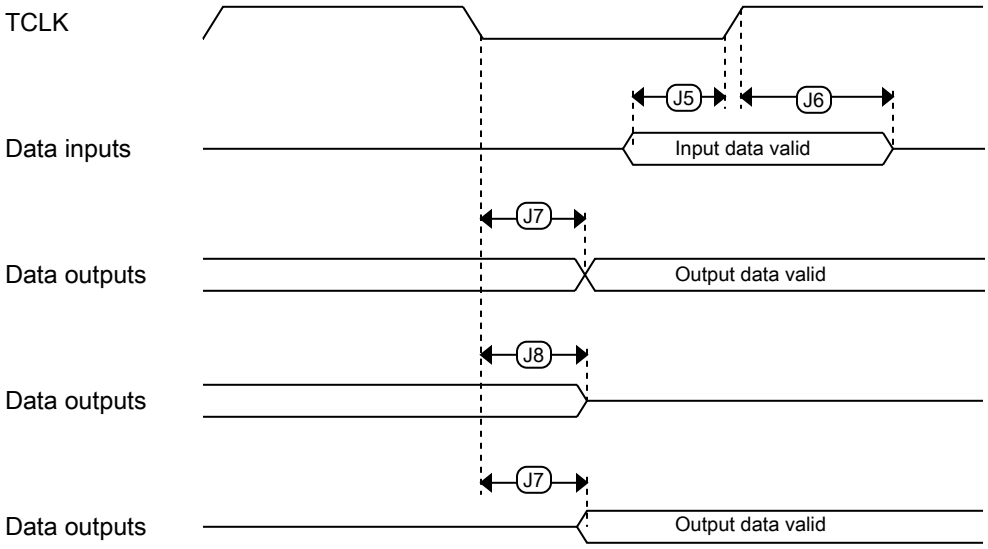


Figure 6. Boundary scan (JTAG) timing

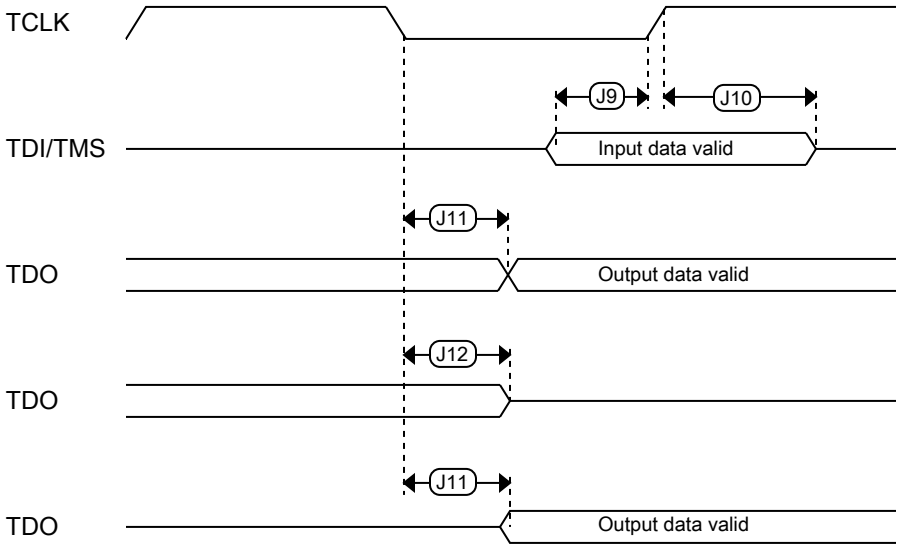


Figure 7. Test Access Port timing

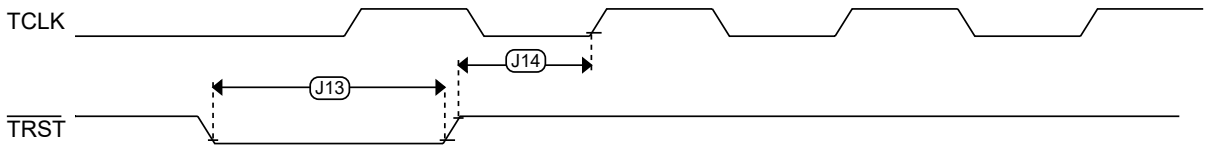


Figure 8. TRST timing

4.7.2 SWD Electricals

Table 28. SWD timing specificaions

Symbol	Description	Min	Max	Unit
J1	SWD_CLK frequency of operation	—	25	MHz
J2	SWD_CLK cycle period	1000/J1	—	ns
J3	SWD_CLK clock pulse width	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	37	ns
J12	SWD_CLK high to SWD_DIO high-Z	2	—	ns

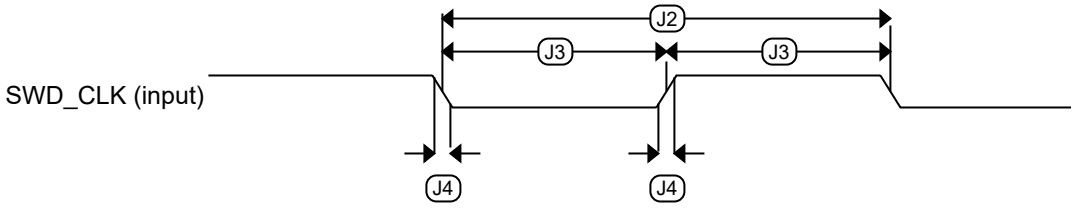


Figure 9. Serial wire clock input timing

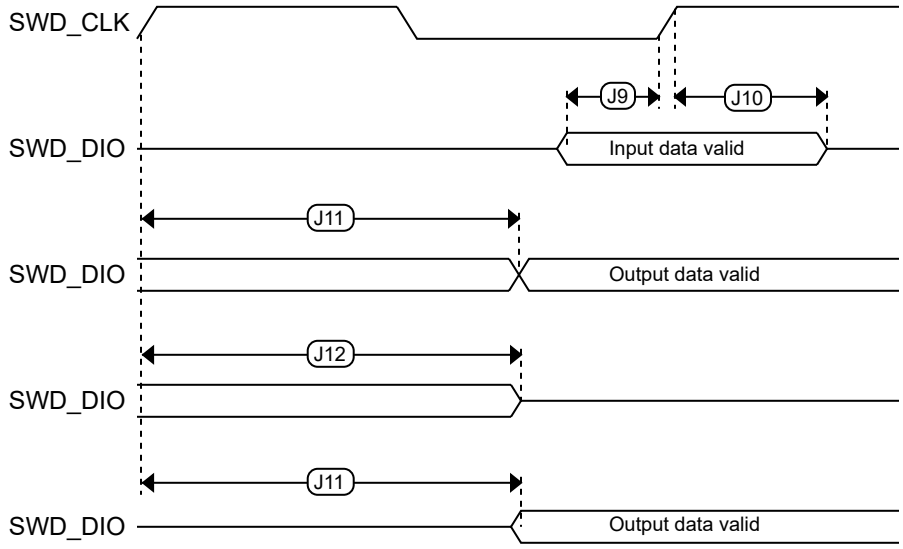


Figure 10. Serial wire data timing

5 Specifications—application domain

5.1 Application domain (APD) power modes

Table 29. APD power modes

Power Mode		Min. Voltage at the pin (V) VDD_DIG1	Max Frequency (MHz) CA35	Biasing Setting	Description
Active	Over Drive	1.05	800	AFBB enabled	All logic is functional in this mode.
	Normal Drive	1	650 MHz	AFBB enabled	Allows Dynamic Voltage Scaling
Sleep		0.9	-	RBB enabled (optional)	Core in Wait-for-Interrupt (WFI) Core, bus, peripheral clock gating configurable by software
Deep Sleep		0.65	-	RBB enabled	Core is in wait-for-interrupt(WFI) state Core/System clock gated

Table continues on the next page...

Table 29. APD power modes (continued)

Power Mode	Min. Voltage at the pin (V) VDD_DIG1	Max Frequency (MHz) CA35	Biasing Setting	Description
				Some peripheral optional functional SRAM contents retained DRAM optionally self-refresh
Power Down	0.65	-	RBB enabled	Core/System/ peripherals power gated SRAM with configurable retention DRAM optionally self-refresh
Deep Power Down	-	-	-	APD domain completely power agted

5.2 Recommended operating conditions—application domain

See Table 7

5.3 Power sequencing—application domain

See Power sequencing—system.

5.4 Peripheral operating requirements and behaviors

5.4.1 DDR timing—application domain

See LPDDR Controller (LPDDRC).

5.4.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing—application domain

The uSDHC interfaces confirms the following eMMC, SD, and SDIO specifications.

- eMMC Electrical Standard revision 5.1 (JESD84-B51A)
- SD Physical Specification revision 3.0
- SDIO Physical Specification revision 3.0

The following table shows eMMC/SD/SDIO mode supports on each port.

Table 30. eMMC/SD/SDIO mode support

uSDCH Instance		uSDHC0	uSDHC1		uSDHC2		
Port Mux (Usage)		D (eMMC/SD)	D (eMMC/SD)	E (SD/SDIO)	D (SD/SDIO)	E (SD/SDIO)	F (SD/SDIO)
Modes	I/O Voltage						
MMC Legacy	3.3 V, 1.8 V	Yes	Yes	No	No	No	No
eMMC High-Speed SDR	3.3 V, 1.8 V	Yes	Yes	No	No	No	No
eMMC High-Speed DDR	3.3 V, 1.8 V	Yes	Yes	No	No	No	No
eMMC HS200	1.8 V	Yes	Yes	No	No	No	No
eMMC HS400	1.8 V	Yes	Yes	No	No	No	No
SD Default	3.3 V	Yes	Yes	Yes	Yes	Yes	Yes
SD High-Speed	3.3 V	Yes	Yes	Yes	Yes	Yes	Yes
SD SDR12	1.8 V	Yes	Yes	Yes	Yes	Yes	Yes
SD SDR25	1.8 V	Yes	Yes	Yes	Yes	Yes	Yes
SD SDR50	1.8 V	Yes	Yes	Yes	Yes	Yes	Yes
SD SDR104	1.8 V	Yes	Yes	Yes	Yes	Yes	Yes
SD DDR50	1.8 V	Yes	Yes	Yes	Yes	Yes	Yes

Table 31. eMMC SD Modes

Modes	Bus Width	I/O Voltage	Max Clock Frequency	Transfer rate	Max Throughput	Introduced in Spec Version
MMC Legacy	1, 4, 8	3.3 V, 1.8 V, 1.2 V	26 MHz	Single	26 MB/sec	
eMMC High-Speed SDR	1, 4, 8	3.3V , 1.8 V, 1.2 V	52MHz	Single	52 MB/sec	
eMMC High-Speed DDR	4, 8	3.3 V, 1.8 V, 1.2 V	52MHz	Dual	104 MB/sec	
eMMC HS200	4, 8	1.8 V, 1.2 V	200MHz	Single	200 MB/sec	
eMMC HS400	8	1.8 V, 1.2 V	200MHz	Dual	400 MB/sec	
SD Default	4	3.3 V	25 MHz	Single	12.5 MB/sec	
SD High-Speed	4	3.3 V	50 MHz	Single	25 MB/sec	
SD SDR12	4	1.8 V	25 MHz	Single	12.5 MB/sec	
SD SDR25	4	1.8 V	50 MHz	Single	25 MB/sec	

Table continues on the next page...

Table 31. eMMC SD Modes (continued)

Modes	Bus Width	I/O Voltage	Max Clock Frequency	Transfer rate	Max Throughput	Introduced in Spec Version
SD SDR50	4	1.8 V	100 MHz	Single	50 MB/sec	
SD SDR104	4	1.8 V	208 MHz	Single	104 MB/sec	
SD DDR50	4	1.8 V	50 MHz	Dual	50 MB/sec	

The following table shows the frequencies at different functional modes and voltages.

Table 32. uSDHC frequencies at different modes

Interface	Protocol	Mode	Freq at 1.1v OD (MHz)		Freq at 1.0v NM (MHz)	
			1.8v	3.3v	1.8v	3.3v
uSDHC0	PTD	HS400	200	N/A	148	N/A
		SDR104	200		148	
		SDR	100		100	
		DDR	50	50	50	50
uSDHC1	PTD	HS400	166	N/A	148	N/A
		SDR104	166		148	
		SDR	100		83	
		DDR	50	50	50	50
uSDHC1	PTF	SDR	100	50	83	50
		DDR	50	N/A	50	N/A
uSDHC2	PTD	SDR104	166	N/A	148	N/A
		SDR	100	50	83	50
		DDR	50	N/A	`50	N/A
uSDHC2	PTF	SDR	100	50	83	50
		DDR	50	N/A	50	N/A
uSDHC2	PTE	SDR	100	50	83	50
		DDR	50	N/A	50	N/A

5.4.2.1 AC timing specification of eMMC and SD operation modes up to 52MHz in SDR mode

The following table shows the AC timing specifications of:

- eMMC Legacy
- eMMC High-Speed SDR
- SD Default
- SD High-speed
- SD SDR12
- SD SDR25

Table 33. eMMC/SD timing specification for operation modes up to 52 MHz

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.1	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.1	—	ns

1. In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
2. In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In High-speed mode, clock frequency can be any value between 0–50 MHz.
3. In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In High-speed mode, clock frequency can be any value between 0–52 MHz.
4. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

The following figure lists the timing characteristics.

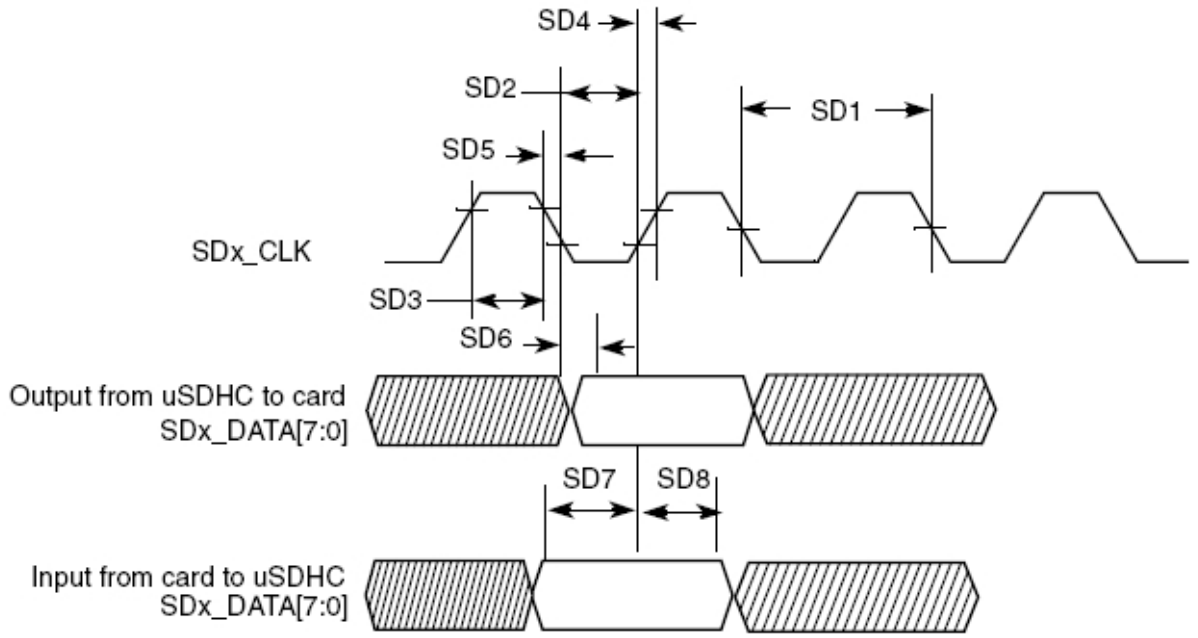


Figure 11. SD3.0 High-Speed mode Timing

5.4.2.2 AC timing specification of eMMC DDR52 and SD DDR50 modes

The following table lists the timing characteristics of eMMC DDR52 mode and SD DDR50 mode, and the following figure depicts the input and output timing diagram at uSDHC IO pins. Note that SDx_DATA signals are triggered and sampled on both edges of the clock, and the SDx_CMD signal is triggered and sampled only on rising edge.

Table 34. AC timing specifications of eMMC DDR52 and SD DDR50 modes

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	3.0	6.4	ns
uSDHC Input / Card Outputs SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.2	—	ns

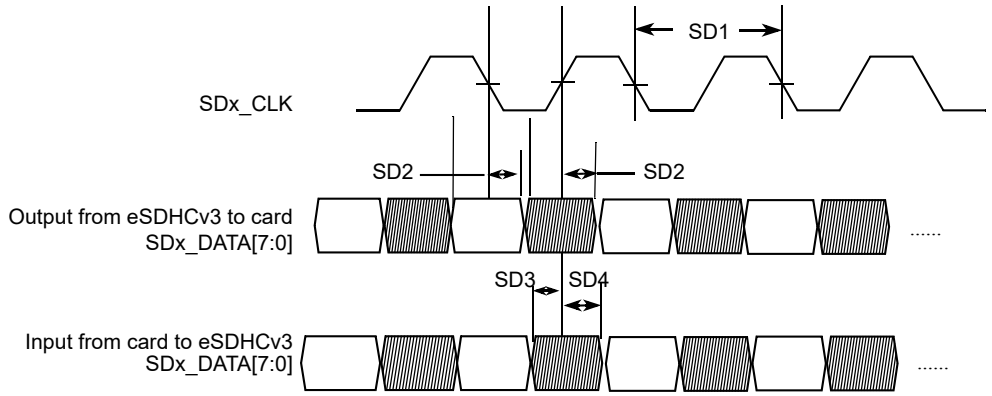


Figure 12. eMMC DDR52 mode and SD DDR50 mode timing

5.4.2.3 SDR50/SDR104 AC timing

The following table shows the timing of SDR50/SDR104, and the figure depicts the SDR50/SDR104 timing characteristics.

Table 35. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	4.6 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	4.6 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3.8	1.6	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.5	0.9	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.1	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.1	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

1. Data window in SDR104 mode is variable.

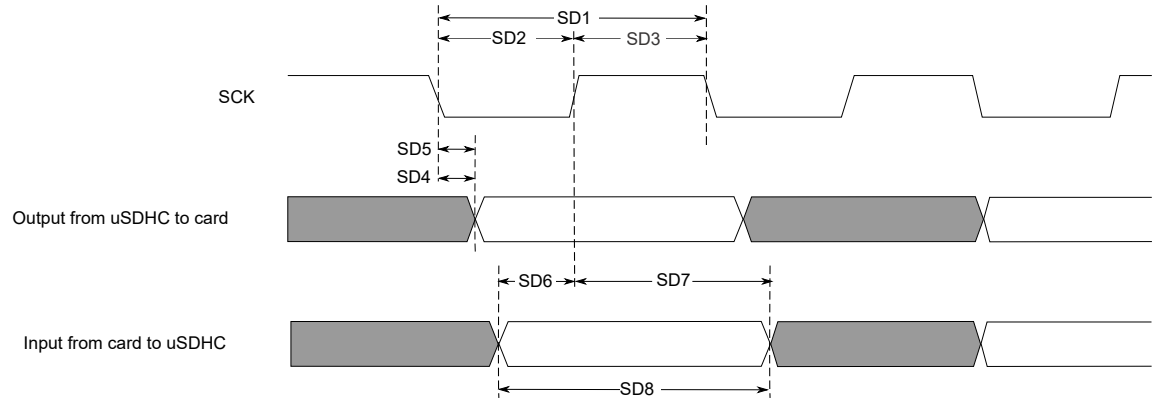


Figure 13. SDR50/SDR104 timing

5.4.2.4 HS200_AC_timing

The following table lists the HS200 timing characteristics and the subsequent figure depicts the timing of HS200 mode.

Table 36. HS200 interface timing specifications

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.5	0.9	ns
uSDHC Input/SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD8	Input Valid Window	t_{ODW}	0.5 x t_{CLK}	—	ns

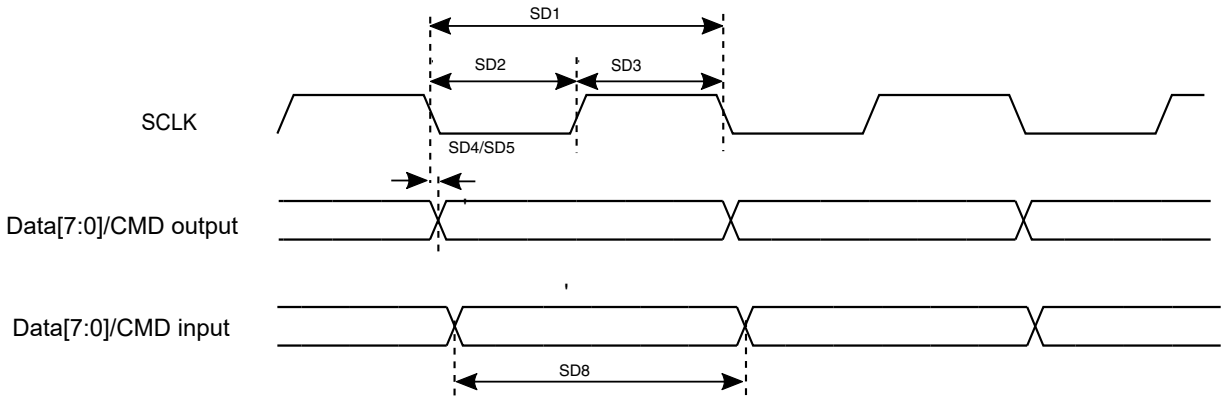


Figure 14. HS200 timing

5.4.2.5 HS400 AC timing

The following table lists the HS400 timing characteristics, and the subsequent figure depicts the timing of HS400. Be aware that only data is sampled on both edges of the clock. The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check parameters SD5, SD6, and SD7 in Table 35 for CMD input/output timing for HS400 mode.

Table 37. HS400 interface timing specifications

ID	Parameter	Symbol	Min.	Max.	Unit
Card Input clock					
SD1	Clock Frequency	f_{pp}	0	200	MHz
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card inputs DAT (Reference to SCK)					
SD4	Output Skew from Data of Edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output Skew from Edge of SCK to Data	t_{OSkew2}	0.45	—	ns
uSDHC input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

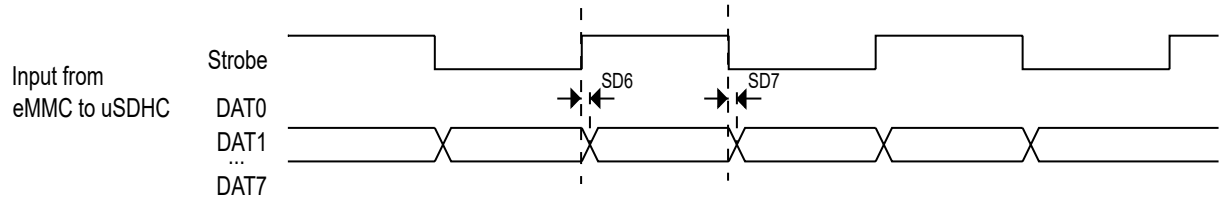


Figure 15. HS400 timing Input

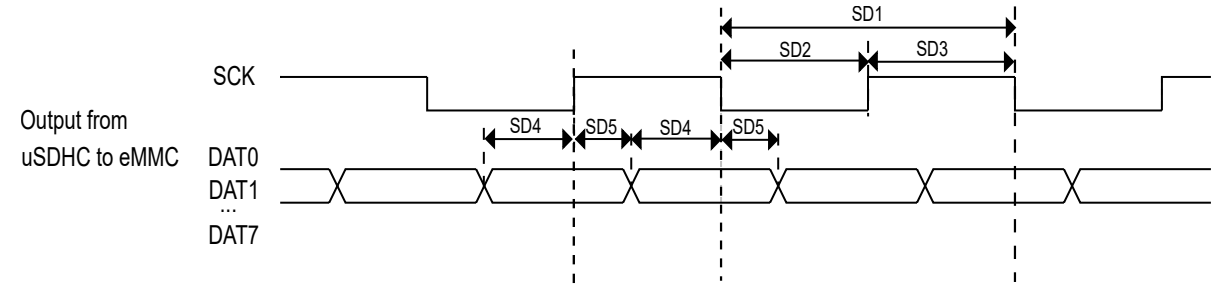


Figure 16. HS400 timing Output

5.4.3 Timer specifications—application domain

See General switching timing specifications for EWM, LPTMR, and TPM.

5.4.4 Connectivity and communications specifications—application domain

5.4.4.1 Ethernet Controller (ENET) AC electrical specifications

The following timing specifications are defined at the chip I/O pin and must be translated appropriately to arrive at timing specifications/constraints for the physical interface.

5.4.4.1.1 ENET MII mode timing

5.4.4.1.1.1 MII receive signal timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

The following table describes MII receive signal timings and the figure below depicts the timing parameters (M1–M4).

Table 38. MII receive signal timing

ID	Characteristic	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	-	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	-	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

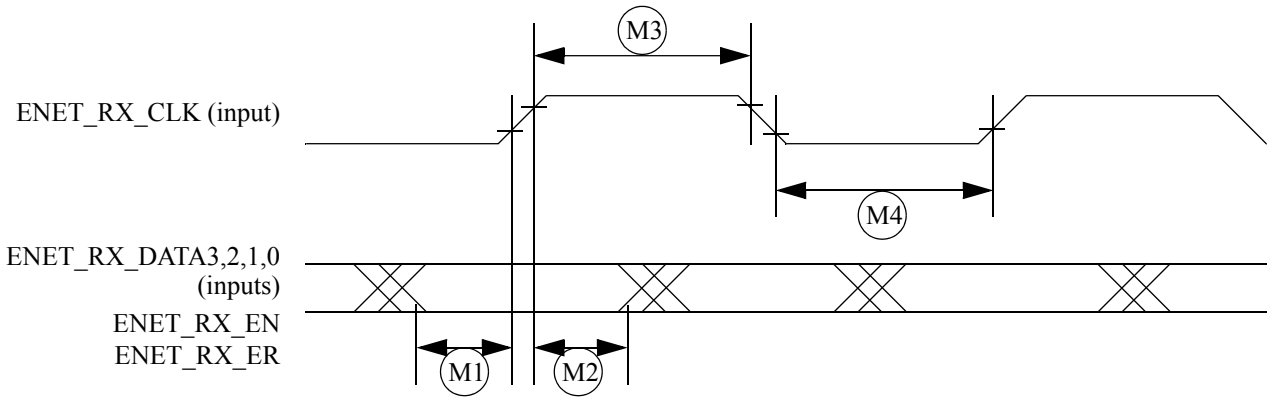


Figure 17. MII receive signal timing diagram

5.4.4.1.2 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

The table below describes the timing parameters (M5–M8).

Table 39. MII transmit signal timing

ID	Characteristic	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

The following figure MII transmit signal timings, as described in the table.

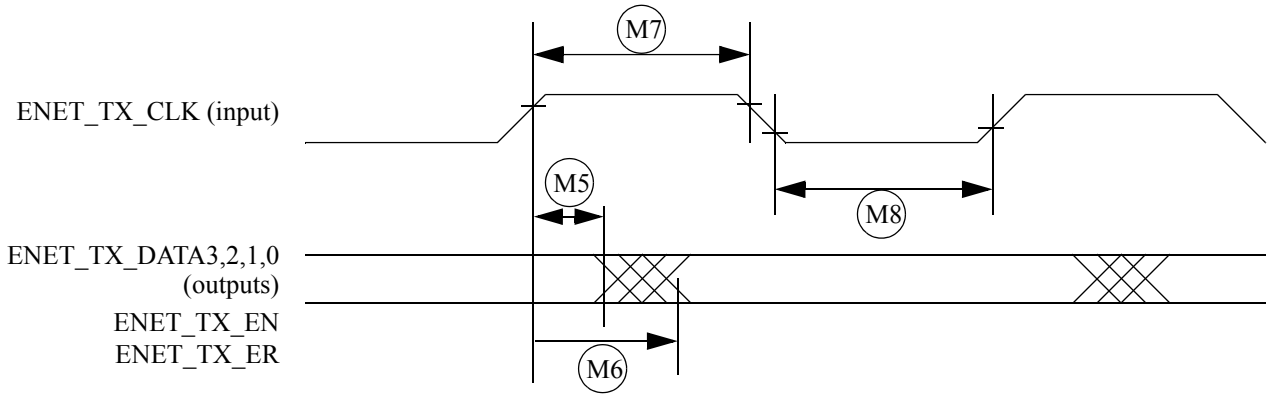


Figure 18. MII transmit signal timing diagram

5.4.4.1.1.3 MII asynchronous inputs signal timing (ENET_CRS and ENET_COL)

The table below describes the timing parameter (M9) .

Table 40. MII asynchronous inputs signal timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

1. ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

The following figure shows MII asynchronous input timings.

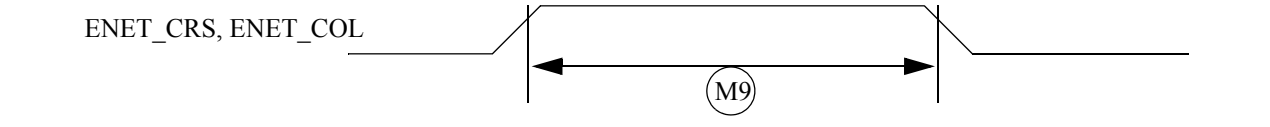


Figure 19. MII async inputs timing diagram

5.4.4.1.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

The table below describes the timing parameters (M10–M15).

Table 41. MII serial management channel timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ENET_TX_CLK period
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

The following figure shows MII asynchronous input timings.

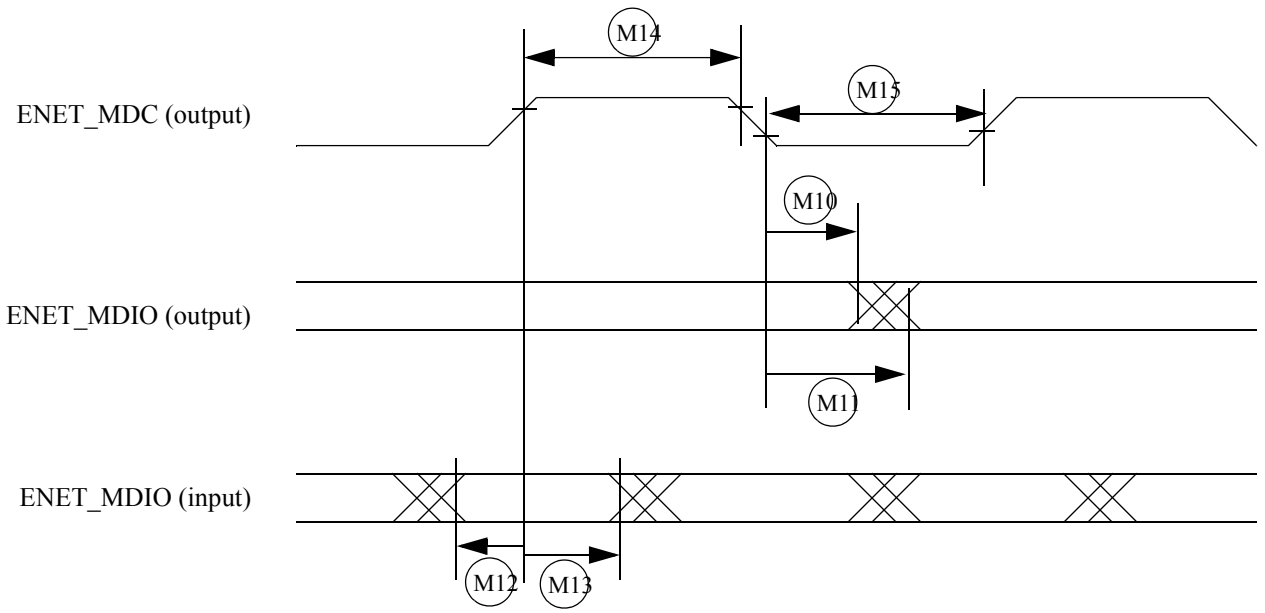


Figure 20. MII serial management channel timing diagram

5.4.4.1.2 RMII mode timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

The table below describes the timing parameters (M16–M21).

Table 42. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	-	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	-	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	3.5	-	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	-	ns

The following figure shows RMII mode timings.

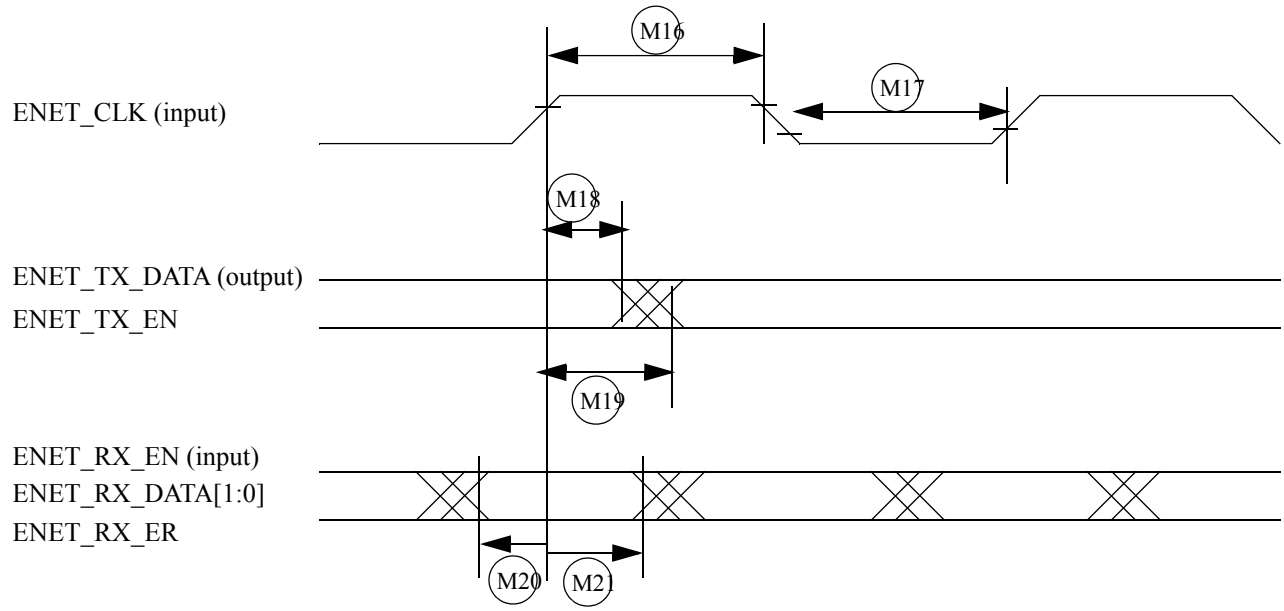


Figure 21. RMII signal timing diagram

5.4.4.2 LPUART

See General switching timing specifications.

5.4.4.3 Inter-Integrated Circuit Interface (I^2C) timing

Table 43. I^2C timing (Standard, Fast modes)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2,5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

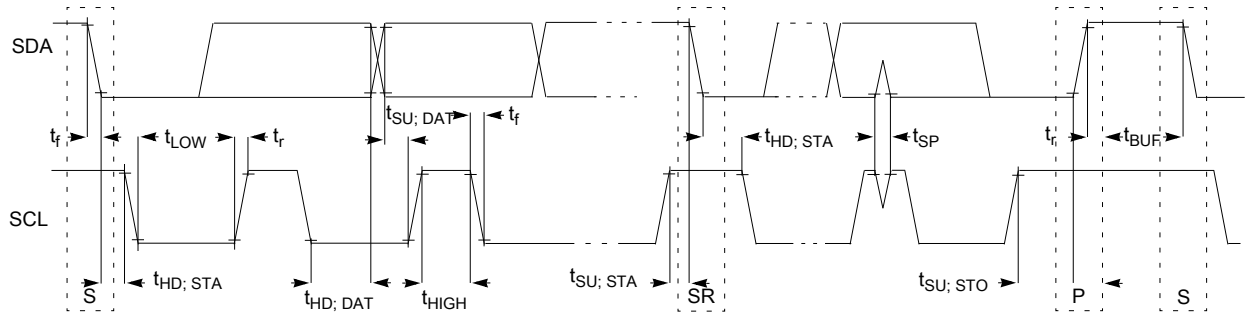


Figure 22. Timing definition for standard, and fast devices on the I^2C bus

Table 44. I ^{2}C 1 Mbps timing

Parameter	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f_{SCLH}	0	1	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	ns
LOW period of the SCL clock	t_{LOW}	0.5	—	ns
HIGH period of the SCL clock	t_{HIGH}	0.26	—	ns
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	ns
Data hold time for I_2C bus devices	t_{HD}; DAT	0	—	ns
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_{rCL}	20 +0.1C_b	120	ns
Fall time of SDA and SCL signals	t_{rCL1}	20 +0.1C_b	120	ns
Set-up time for STOP condition	t_{fCL}	0.26	—	ns
Bus free time between STOP and START condition	t_{rDA}	0.5	—	ns
Pulse width of spikes that must be suppressed by the input filter	t_{fDA}	0	50	ns

5.4.4.4 Improved Inter-Integrated Circuit Interface (I3C) specifications

Unless otherwise specified, I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

Table 45. MIPI-I3C specifications when communicating with legacy I^{2}C devices

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	0.4	0	1.0	MHz
t_{SU_STA}	Set-up time for a repeated START condition	600	—	260	—	ns
Hold time (repeated) START condition	t_{HD}; STA	600	—	260	—	ns
t_{LOW}	LOW period of the SCL clock	1300	—	500	—	ns
t_{HIGH}	HIGH period of the SCL clock	600	—	260	—	ns
t_{SU_DAT}	Data set-up time	100	—	50	—	ns
t_{HD_DAT}	Data hold time for I_2C bus devices	0	—	0	—	ns
t_f	Fall time of SDA and SCL signals	20 + 0.1C_b[1]	300	20 + 0.1C_b[1]	120	ns
t_r	Rise time of SDA and SCL signals	20 + 0.1C_b[1]	300	20 + 0.1C_b[1]	120	ns
t_{SU_STO}	Set-up time for STOP condition	600	—	260	—	ns

Table continues on the next page...

Table 45. MIPI-I3C specifications when communicating with legacy I^2C devices (continued)

Symbol	Characteristic	400 kHz/Fast mode		1 MHz/ Fast+ mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time between STOP and START condition	1.3	—	0.5	—	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns

1. C_b = total capacitance of the one bus line in pF.

Table 46. MIPI-I3C open drain mode specifications

Symbol	Characteristic	Min.	Max.	Unit	Notes
t_{LOW_OD}	LOW period of the SCL clock	200	—	ns	
$t_{DIG\_OD\_L}$		t_{LOW_OD} + t_{fDA_OD} (min)	—	ns	
t_{HIGH}	HIGH period of the SCL clock	t_{CF}	12	ns	
t_{fDA_OD}	Fall time of SDA signal	20 +0.1C_b	120	ns	1
t_{SU_OD}	Data set-up time during open drain mode	3	—	ns	
t_{CAS}	Clock after START (S) Condition • ENTAS0 • ENTAS1 • ENTAS2 • ENTAS3	 38.4 n 38.4 n 38.4 n 38.4 n	 1 µ 100 µ 2 m 50 m	 s s s s	
t_{CBP}	Clock before STOP (P) condition	t_{CAS}(min)/2	—	ns	
$t_{MMOverlap}$	Current master to secondary master overlap time during handoff	$t_{DIG\_OD\_L}$	—	ns	
t_{AVAL}	Bus available condition	1	—	µs	
t_{IDLE}	Bus idle condition	1	—	ms	
t_{MMLock}	Time internal where new master not driving SDA low	t_{AVAL}	—	µs	

1. C_b = total capacitance of the one bus line in pF.

Table 47. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
f_{SCL}	SCL Clock Frequency	0.01	12	12.9	MHz	
t_{LOW}	LOW period of the SCL clock	24	—	—	ns	
t_{DIG_L}		32	—	—	ns	
t_{HIGH_MIXED}	HIGH period of the SCL clock for a mixed bus	24	—	—	ns	

Table continues on the next page...

Table 47. MIPI-I3C push-pull specifications for SDR and HDR-DDR modes (continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$t_{DIG\_H\_MIXED}$		32	—	45	ns	1
t_{HIGH}	HIGH period of the SCL clock	24	—	—	ns	
t_{DIG_H}		32	—	—	ns	
t_{SCO}	Clock in to data out for a slave	—	—	12	ns	
t_{CR}	SCL clock rise time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	
t_{CF}	SCL clock fall time	—	—	150 x 1/ f_{SCL} (capped at 60)	ns	
t_{HD_PP}	SDA signal data hold • Master mode • Slave mode	t_{CR} + 3 and t_{CF} + 3 0	— —	— —	ns	
t_{SU_PP}	SDA signal setup	3	—	—	ns	
t_{CASr}	Clock after repeated START (Sr)	t_{CAS} (min)	—	—	ns	
t_{CBSr}	Clock before repeated START (Sr)	t_{CAS} (min)/2	—	—	ns	
C_b	Capacitive load per bus line	—	—	50	pF	

1. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C devices do not interpret I3C signaling as valid I^2C signaling.

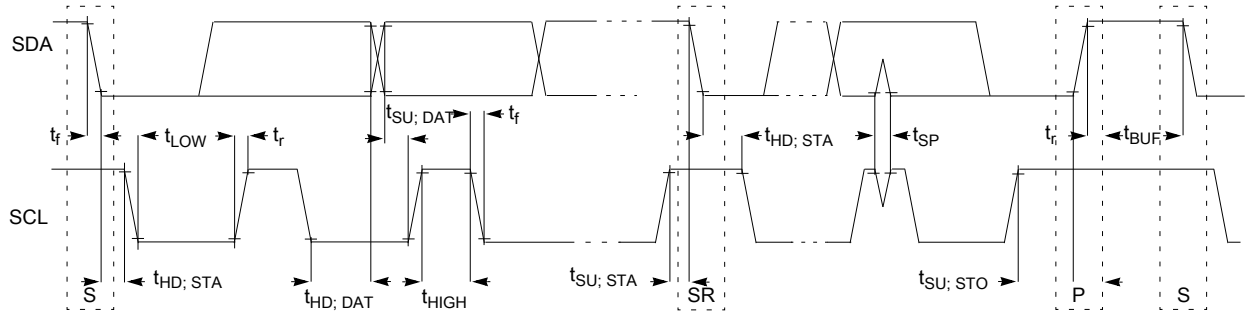


Figure 23. Timing definition for devices on the I^2C bus

5.4.4.5 Low-power serial peripheral interface (LPSPI) switching specifications—application domain

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes. See the LPSPI chapter of the chip reference manual for information about the modified transfer formats used for communicating with slower peripheral devices.

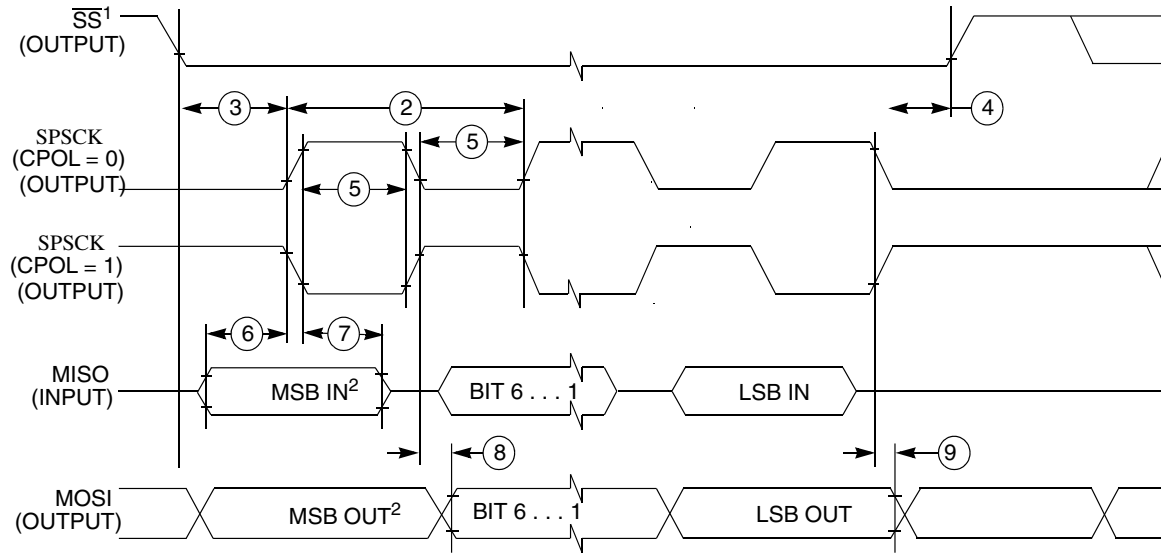
All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 48. LPSPI master mode timing

Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation • LPSPI0-LPSPI3 • LPSPI4-LPSPI5	 $f_{periph}/2048$ $f_{periph}/2048$	 30 60	 MHz MHz	1
LP2	SPSCK period (t_{SPSK}) • LPSPI0-3 • LPSPI4-5	 33.33 16.67	 2048 x t_{periph} 2048 x t_{periph}	 ns	
LP3	Enable lead time	1/2	—	t_{SPSK}	2
LP4	Enable lag time	1/2	—	t_{SPSK}	2
LP5	Clock (SPSCK) high or low time	$t_{SPSCK}/2$ - 2	$t_{SPSCK}/2$ + 2	ns	—
LP6	Data setup time (inputs) • LPSPI0-3 • LPSPI4-5	 12.0 6.0	 — —	 ns	—
LP7	Data hold time (inputs)	0	—	ns	—
LP8	Data valid (after SPSCK edge) • LPSPI0-3 • LPSPI4-5	 — —	 9.0 6.0	 ns	—
LP9	Data hold time (outputs)	-1	—	ns	—

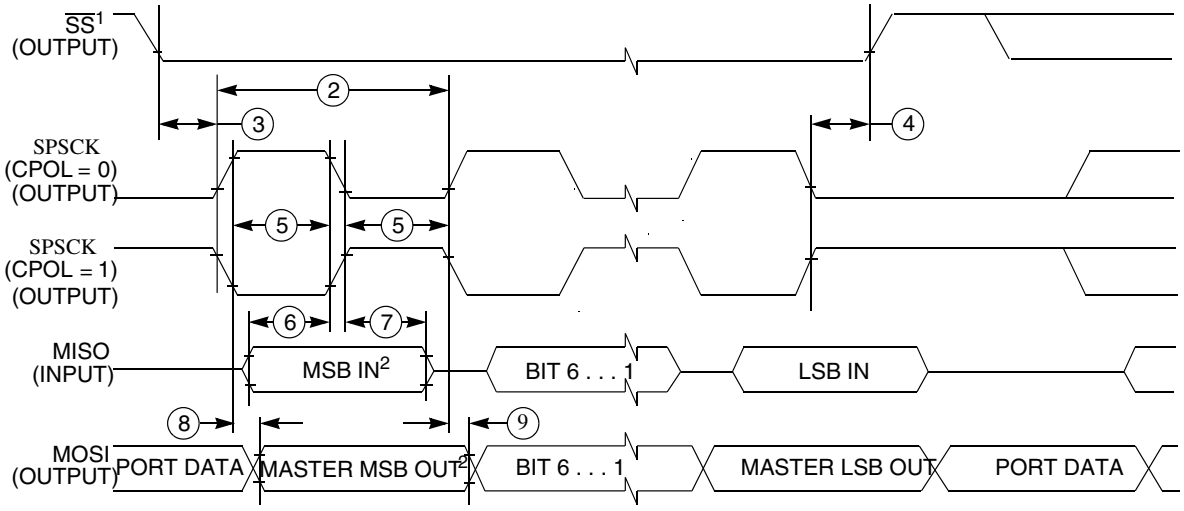
1. The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/2$, where f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$

The following figures show the master mode timing characteristics for LPSPI.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ... bit 6, MSB.

Figure 24. LPSPI master mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 25. LPSPI master mode timing (CPHA = 1)

Table 49. LPSPI slave mode timing

Symbol	Description	Min.	Max.	Unit	Notes
LP1	Frequency of operation • LPSPI0-LPSPI3 • LPSPI4-LPSPI5	 — —	 15 30	 MHz MHz	1
LP2	SPSCK period (t_{SPSK})	66.67	2048 x t_{periph}	ns	

Table continues on the next page...

Table 49. LPSPI slave mode timing (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• LPSPI0-3 • LPSPI4-5	33.33	2048 x t_{periph}		
LP3	Enable lead time	1	—	t_{periph}	2
LP4	Enable lag time	1	—	t_{periph}	2
LP5	Clock (SPSCK) high or low time	$t_{SPSCK}/2 - 2$	$t_{SPSCK}/2 + 2$	ns	—
LP6	Data setup time (inputs) • LPSPI0-3 • LPSPI4-5	 7.0 4.0	 — —	ns	—
LP7	Data hold time (inputs) • LPSPI0-3 • LPSPI4-5	 5.0 3.0	 — —	ns	—
LP8	SPI_SPSCK to SPI_MISO data valid (output data valid): ($t_{SPSCK2DV}$) • LPSPI0-3 • LPSPI4-5	 — —	 15 13	ns	
LP9	SPI_SPSCK to SPI_MISO data invalid (output data hold): ($t_{SPSCK2DH}$) • LPSPI0-3 • LPSPI4-5	 2.0 2.0	 — —	ns	
LP10	SPI_SS active to SPI_MISO driven (t_{SS2DRV})	12	—	ns	—
LP11	SPI_SS inactive to SPI_MISO not driven (t_{SS2HIZ})	12	—	ns	—

1. The frequency of operation is also limited to a minimum of $f_{periph}/2048$ and a max of $f_{periph}/4$, where f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$

The following figures show the slave mode timing characteristics for LPSPI.

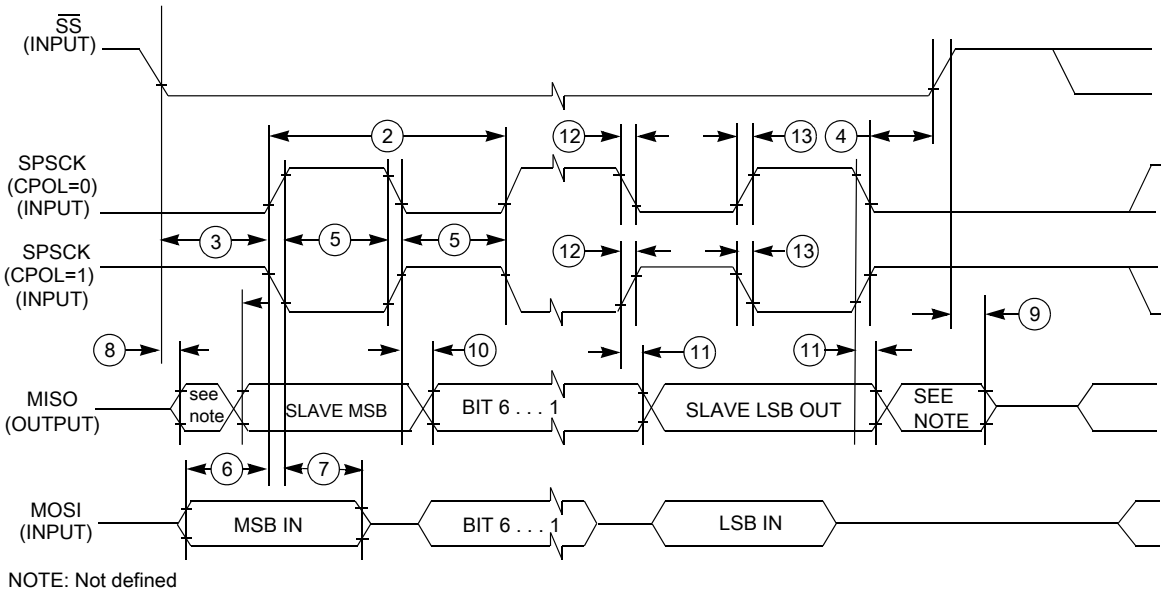


Figure 26. SPI slave mode timing (CPHA = 0)

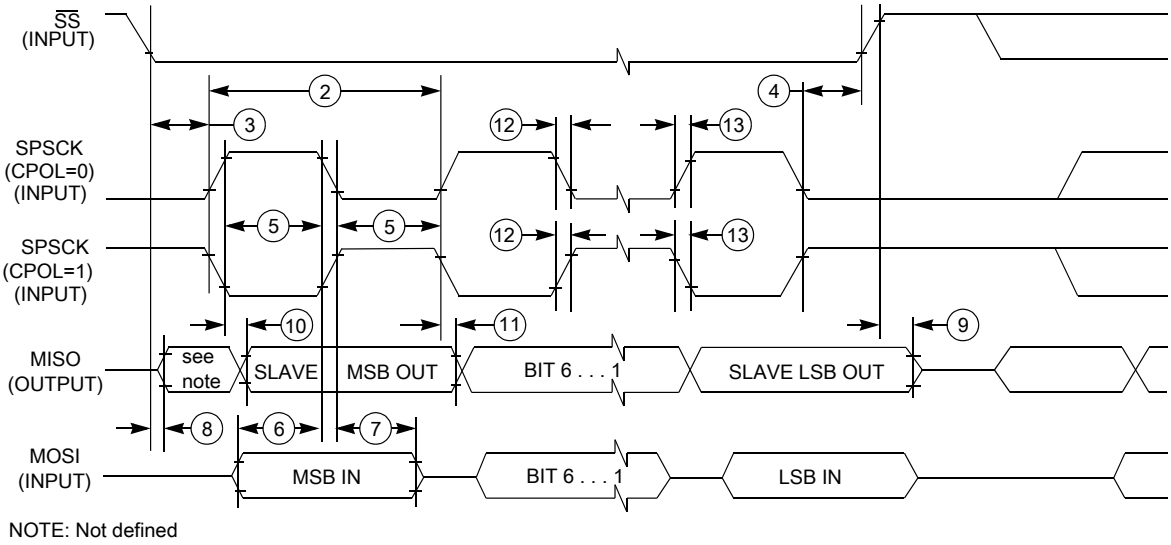


Figure 27. SPI slave mode timing (CPHA = 1)

5.4.4.6 USB Full Speed Transceiver and High Speed PHY specifications

This section describes the High Speed USB PHY parameters. The high speed PHY is capable of full and low speed signaling as well.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000

- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

USB0_VBUS pin is a detector function which is 5v tolerant and complies with the above specifications without needing any external voltage division components.

6 Specifications—LPAV domain

6.1 LPDDR Controller (LPDDRC)

The LPDDR Controller is a configurable DDR controller that provides interface to LPDDR3, LPDDR4 and LPDDR4X memories. The LPDDR4/4X includes a DFI interface to work with PHY. The controller is responsible for communication with the system through AXI interface, DDR commands generation, DDR command optimizations, and read/ write data path. The PHY performs timing adjustment using special calibration mechanisms to ensure data capture margin at the supported clock rate.

6.1.1 LPDDR3/4/4X parameters

The LPDDR Memory Controller (LPDDRC) is designed to be compatible with JEDEC-compliant SDRAMs.

- JESD209-4B compliant LPDDR4/LPDDR4X memories
- JESD209-3C compliant LPDDR3 memory

LPDDRC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 8ULP application processor. Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here. Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation; PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on device page i.MX8 Processors

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

The following table shows the configuration for LPDDR3/4/4X used in i.MX 8ULP.

Table 50. LPDDR3/4/4x configurations

Parameter	LPDDR3	LPDDR4	LPDDR4X
Data rates	800 MT/s[1]	1056 MT/s	1056 MT/s
Bus width	32-bit	32-bit	32-bit
Channels	1	2	2
Chip Selects	2	2	2

1. With ODT enabled

6.2 Display, Video, and Audio Interfaces

6.2.1 MIPI DSI timing—LPAV domain

The i.MX 8ULP conforms to the MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant for MIPI display port x4 lanes. It also supports MIPI Specification for D-PHY Version 2.1 and is backward compatible with MIPI Specification for D-PHY v1.2 and D-PHY v1.1

6.2.2 MIPI CSI timing—LPAV domain

The i.MX 8ULP conforms to the MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.1 compliant for MIPI display port x2 lanes. It also supports MIPI DPHY^{SM} V1.1 specification.

6.2.3 PDM Microphone Interface (MICFIL) timing parameters

NOTE

These timing requirements apply only if the clock divider is enabled (PDM_CTRL2[CLKDIV]=0), otherwise there are no special timing requirements.

The PDM microphones must meet the setup and hold timing requirements shown in the following table. The "k" factor value in Table 51 depends on the selected quality mode as shown in Table 52.

Table 51. Timing parameters

Parameter	Value
trs, tfs	$<= \frac{\text{floor(K x } CLKDIV) - 1}{\text{@(moduleNickname)\_CLK\_ROOT rate}}$ [1]
trh. tfh	>=0

1. @moduleNickname= PDM. Depending on K value, the user must make sure floor(K x CLKDIV) > 1 to avoid timing problems.

Table 52. K factor value

Quality factor	K factor
High Qaulity	1/2
Medium Quality, Very Low Quality 0	1
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4

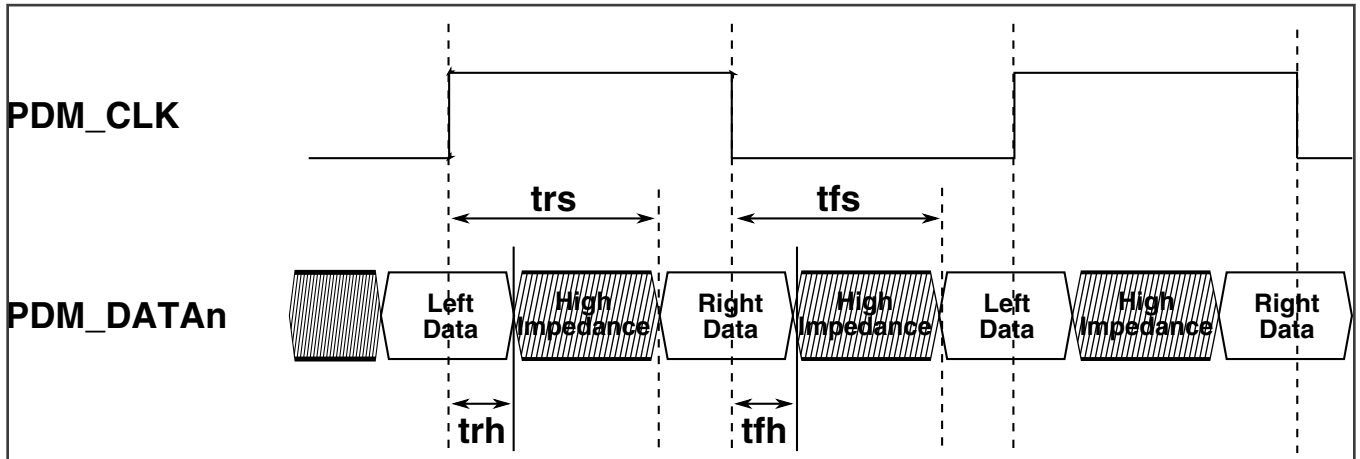


Figure 28. Input/Output TIming Requirements

6.2.4 EPDC timing specifications

The following table containg the EPDC timing specifications,

AXI bus clock domain: 316.8 MHz

PIX clock domain: 300 MHz

Table 53. EPDC timing specifications

Parameter	EPDC IO ports	Note
EPDC output skew	GDCLK	Minimize the output skew to be <1/4 EPDC internal pixel clock cycle.
	GDSP	
	GDRL	
	SDCLK	
	SDCLKN	
	SDLE	
	SDOEZ	
	SDOED	
	SDOE	
	SDDO[*]	
	SDCE[*]	
	SDSHR	
EPDC input skew	PWRSTAT	Minimize the input skew to be <1/4 EPDC AXI bus clock cycle.
	PWRIRQ	
EPDC output skew	BDR[*]	Minimize the output skew to be <1/4 EPDC AXI bus clock cycle.
	PWRCTRL[*]	
	PWRWAKE	
	PWRCOM	

7 Specifications—real-time domain

7.1 Real time domain (RTD) power modes

Table 54. RTD power modes

Power Mode		Min. Voltage at the pin (V) VDD_DIG0	Max Frequency (MHz) CM33/ Fusion DSP	Biasing Setting	Description
Active	Over Drive	1.05	216/200	AFBB enabled	All logic is functional in this mode. Allows Dynamic Voltage Scaling(DVS)
	Normal Drive	1	127/127	AFBB enabled	
	Under Drive	0.9	38.4/38.4	ARBB enabled	
Sleep		0.9	-	RBB enabled (optional)	Core in Wait-for-Interrupt (WFI) Core, bus, peripheral clock gating configurable by software
Deep Sleep		0.65	-	RBB enabled	Core is in wait-for-interrupt(WFI) state Core/System clock gated Some peripheral optional functional SRAM contents retained
POWER DOWN		0.65	-	RBB enabled	Core/System/ peripherals power gated SRAM with configurable retention Comparator, LP timers optionally functional
DEEP POWER DOWN		-	-	-	RTD domain completely power gated

Table continues on the next page...

Table 54. RTD power modes (continued)

Power Mode	Min. Voltage at the pin (V) VDD_DIG0	Max Frequency (MHz) CM33/ Fusion DSP	Biasing Setting	Description
				DGO (aka Always ON) domain ON Comparator, LP timers optionally functional

7.2 Power sequencing—real-time domain

See Power sequencing—system.

7.3 Peripheral operating requirements and behaviors—real-time domain

7.3.1 FlexSPI parameters

The FlexSPI bus interface can operate in Single Data Rate (SDR) or Double Data Rate (DDR) signaling modes. Different AC timings are specified for SDR and DDR signaling modes.

The FlexSPI interface uses the Read Strobe signal (DQS) as the reference clock to sample input data. There are two types of flash memory devices: one with a Read Strobe pin and one without. The FlexSPI interface supports both types of memory device. When the external flash device does not have a DQS pin, the FlexSPI controller internally generates a dummy Read Strobe and loopback.

FlexSPI supports the following clocking scheme for a read data path:

- Dummy read strobe generated by the FlexSPI controller and looped back internally (FlexSPIn_MCR0[RXCLKSRC] = 0x0, or Mode 0)
- Read strobe provided by memory device and input from DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x3 or Mode 3)

The maximum FlexSPI frequency depends on the following factors:

- Bus signaling mode: SDR or DDR
- Clocking scheme for read data path
- IO voltage level
- Core voltage level
- Type of IO pad, where the FlexSPI interface is multiplexed

See the tables below to know the FlexSPI maximum supported frequencies in various modes at different locations.

Table 55. FlexSPI frequency for various modes on RTD

Interface	Modes	Frequency at 1.05v OD (MHz)		Frequency at 1.0v ND (MHz)[1]		Frequency at 0.9v ARBB (MHz)	
		1.8v[2]	3.3v[3]	1.8v	3.3v	1.8v	3.3v
FlexSPI0_A	Mode 0 SDR	90	86	90	86	45	45
	Mode 0 DDR	45	43	45	43	22	22
FlexSPI0_B	Mode 0 SDR	60	60	60	60	45	45

Table continues on the next page...

Table 55. FlexSPI frequency for various modes on RTD (continued)

Interface	Modes	Frequency at 1.05v OD (MHz)		Frequency at 1.0v ND (MHz)[1]		Frequency at 0.9v ARBB (MHz)	
	Mode 0 DDR	30	30	30	30	22	22
FlexSPI0_A/B	Mode 3 DDR	180	100	100	100	45	45
FlexSPI1_A/B	Mode 0 SDR	60	60	60	60	60	45
	Mode 0 DDR	30	30	30	30	30	22
	Mode 3 DDR	180	100	100	100	42	42

1. Voltage at the pin.
2. 1.8 v corresponds to PAD voltage
3. 3.3v corresponds to PAD voltage

Table 56. FlexSPI frequency for various modes on APD

Interface	Modes	Frequency at 1.05v OD (MHz)		Frequency at 1.0v ND (MHz)[1]	
		1.8v[2]	3.3v[3]	1.8v	3.3v
FlexSPI2_A (PTD pins)	Mode 0 SDR	90	90	90	88
	Mode 0 DDR	45	45	45	44
FlexSPI2_B (PTD pins)	Mode 0 SDR	60	60	60	60
	Mode 0 DDR	30	30	30	30
FlexSPI2_A/B (PTD pins)	Mode 3 DDR	166	100	83	100
FlexSPI2_A/B (PTE pins)	Mode 0 SDR	60	60	60	50
	Mode 0 DDR	30	30	30	25
	Mode 3 DDR	100	83	50	50

1. Voltage at the pin.
2. 1.8 v corresponds to PAD voltage
3. 3.3v corresponds to PAD voltage

7.3.1.1 FlexSPI timings for SDR with internal loopback input sample (Mode 0 - FlexSPIn_MCR0[RXCLKSRC] = 0x0)

Table 57. FlexSPI timings for SDR in Mode 0

ID	Parameter	Min.	Max.	Unit
-	FlexSPIx[A/B]_SCLK cycle frequency	—	See Mode 0 in Table 58	MHz
t_1	FlexSPIx[A/B]_SCLK High or Low Time	7.5	—	ns
t_2	FlexSPIx[A/B]_SSy_B pulse width	1.0	—	SCLK

Table continues on the next page...

Table 57. FlexSPI timings for SDR in Mode 0 (continued)

ID	Parameter	Min.	Max.	Unit
t_3	FlexSPIx[A/B]_SSy_B lead time[1, 2]	Tcss + 0.5	—	SCLK
t_4	FlexSPIx[A/B]_SSy_B lag time [1, 3]	Tcsh	—	SCLK
t_5	FlexSPIx[A/B]_DATAy output delay	See SDR output hold for Mode 0 in Table 58	See SDR output setup for Mode 0 in Table 58	ns
t_6	FlexSPIx[A/B]_DATAy setup time	See SDR input setup for Mode 0 in Table 58	—	ns
t_7	FlexSPIx[A/B]_DATAy hold time	See SDR Input Hold for Mode 0 in Table 58	—	ns

1. Timing is controlled from FLSHxCR1 register (x=A1, A2, B1, or B2).
2. Tcss: Chip select output setup time.
3. Tcsh: Chip select output hold time.

Table 58. FlexSPI AC specifications for SDR mode 0

Parameter	Max interface frequency				Unit
Frequency SDR	90 - 84	83 - 61	60-51	≤ 50	MHz
SDR input setup	7	7	8	8	ns
SDR input hold	0	0	0	0	ns
SDR output setup	3.5	4.25	4.25	8	ns
SDR output hold	- 3.5	- 4.25	- 4.25	- 8	ns

7.3.1.2 SDR timing diagrams for Mode 0

The following timing diagrams are valid for FlexSPIn_MCR0[RXCLKSRC] = 0x0.

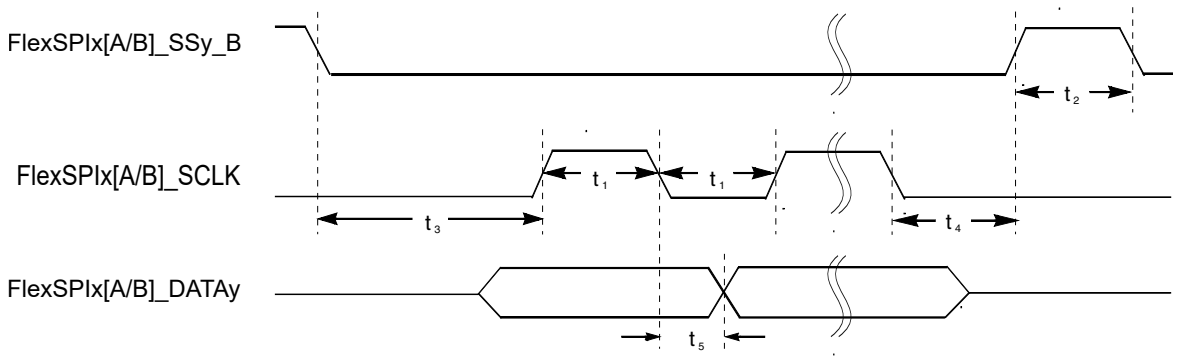


Figure 29. SDR output timing diagram for Mode 0

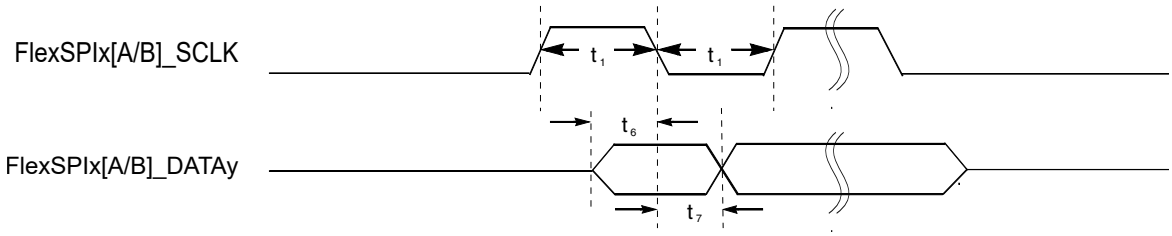


Figure 30. SDR input timing diagram with internal loopback input sample for Mode 0

7.3.1.3 FlexSPI timings for DDR with internal loopback input sample (Mode 0 - FlexSPIn_MCR0[RXCLKSRC] = 0x0)

Table 59. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x0 (DDR mode)

ID	Parameter	Min.	Max.	Unit
	FlexSPIx[A/B]_SCLK cycle frequency	—	See Mode 0 in Table 60	MHz
t_1	FlexSPIx[A/B]_SCLK high or low time	15	—	ns
t_2	FlexSPIx[A/B]_SSy_B pulse width	1	—	SCLK
t_3	FlexSPIx[A/B]_SSy_B lead time [1]	(TCSS + 0.5) / 2	—	SCLK
t_4	FlexSPIx[A/B]_SSy_B lag time [1]	TCSH / 2	—	SCLK
t_5	FlexSPIx[A/B]_DATAy output valid time	—	See DDR output setup for mode 0 in Table 60	ns
t_6	FlexSPIx[A/B]_DATAy output hold time	See DDR Output Hold for mode 0 in Table 60	—	ns
t_7	FlexSPIx[A/B]_DATAy setup time	See DDR Input Setup for Mode 0 in Table 60	—	ns
t_8	FlexSPIx[A/B]_DATAy hold time	See DDR Input Hold for Mode 0 in Table 60	—	ns

1. Timing is controlled from FLSHxCR1 register (x=A1, A2, B1, or B2).

Table 60. FlexSPI DDR AC specifications for Mode 0

Parameter	Max interface frequency		Unit
Frequency DDR	45 -40	30	MHz
DDR input setup	7	8	ns
DDR input hold	0	0	ns
DDR output setup	3	3	ns
DDR output hold	- 3	- 3	ns

7.3.1.4 DDR Timing Diagrams for Mode 0

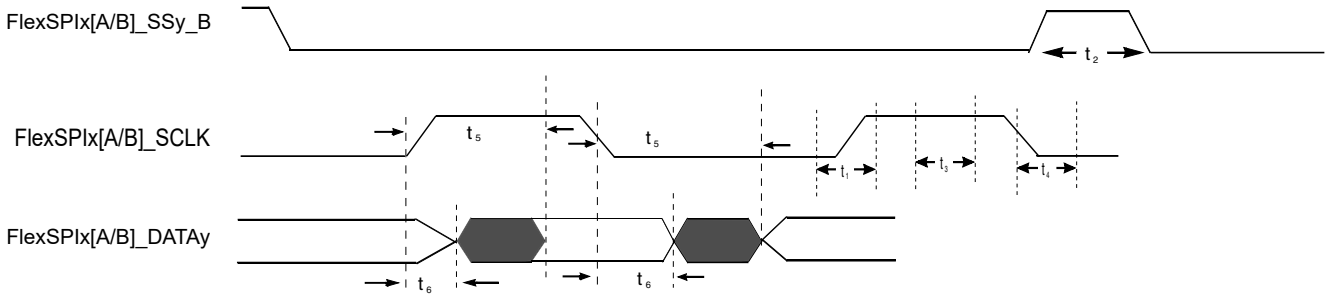


Figure 31. DDR output timing diagram for Mode 0

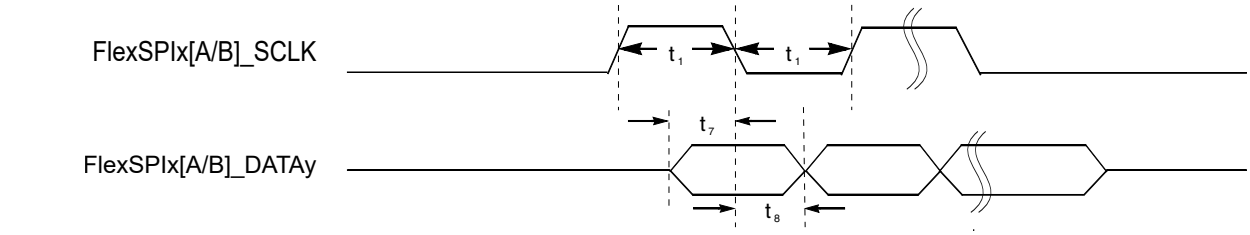


Figure 32. DDR input timing diagram with internal loopback input sample for Mode 0

7.3.1.5 FlexSPI timings for SDR with external DQS input sample (Mode 3 - FlexSPIn_MCR0[RXCLKSRC] = 0x3)

Table 61. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x3 (SDR mode)

ID	Parameter	Min.	Max.	Unit
	FlexSPIx[A/B]_SCLK cycle frequency		See values in Table 62	MHz
t_1	FlexSPIx[A/B]_SCLK high or low time	2.25	—	ns
t_2	FlexSPIx[A/B]_SSy_B pulse width[1]	CSINTERVAL	—	SCLK
t_3	FlexSPIx[A/B]_SSy_B lead time[2, 3]	Tcss + 0.5	—	SCLK
t_4	FlexSPIx[A/B]_SSy_B lag time[2, 4]	Tcsh	—	SCLK
t_5	FlexSPIx[A/B]_DATAy output delay	See SDR output hold for Mode 3 in Table 62	See SDR output setup for Mode 3 in Table 62	ns
t_6	FlexSPIx[A/B]_DATAy input setup time	See SDR input setup for Mode 3 in Table 62		ns
t_7	FlexSPIx[A/B]_DATAy input hold time	See SDR input hold for Mode 3 in Table 62		

1. Minimum is 2 SCLK cycles even if CSINTERVAL value is less than 2.
2. Timing is controlled from FLSHxCR1 register (x=A1, A2, B1, or B2).

3. Tcss: Chip select output setup time.
4. Tcsh: Chip select output hold time.

Table 62. FlexSPI AC SDR specifications for input mode 3

Parameter	Max interface frequency					Unit
Frequency SDR	180	166	100	83	50 - 42	MHz
SDR input setup	0.6	0.6	0.8	1.2	2.75	ns
SDR input hold	-0.6	-0.6	-0.8	-1.2	-2.75	ns
SDR output setup	1.5	2	3.5	4.25	8	ns
SDR output hold	-1.5	-2	-3.5	-4.25	-8	ns

7.3.1.6 SDR timing diagrams for Mode 3

The following timing diagrams are valid for FlexSPIn_MCR0[RXCLKSRC] = 0x3.

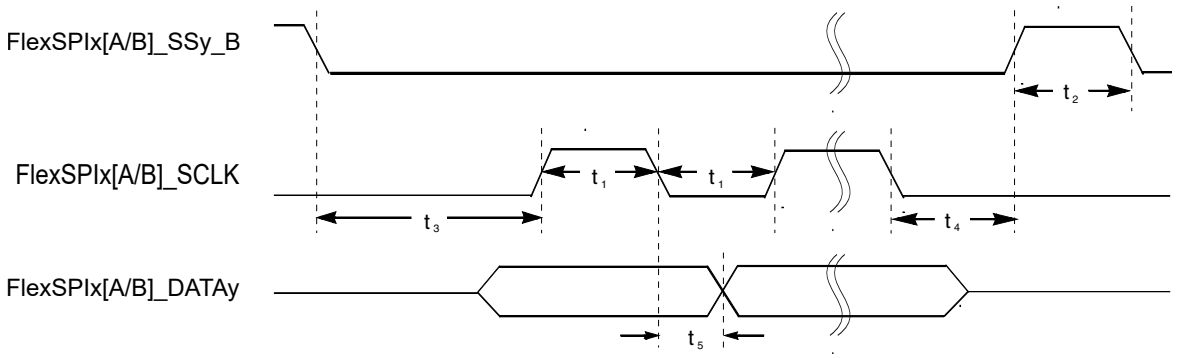


Figure 33. SDR output timing diagram for Mode 3

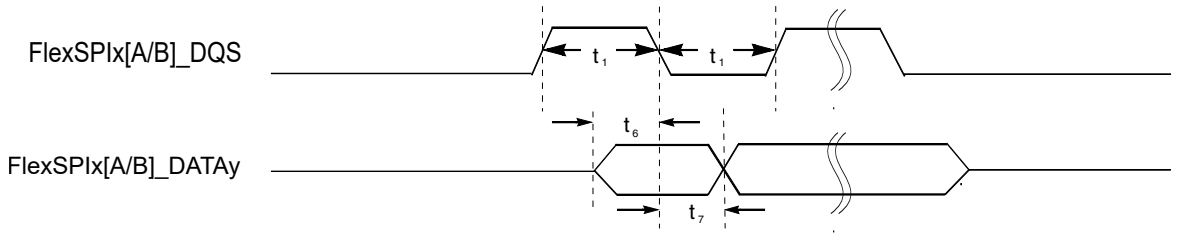


Figure 34. Input timing diagram for SDR with external DQS input sample

7.3.1.7 FlexSPI timings for DDR with external DQS input sample (Mode 3 - FlexSPIn_MCR0[RXCLKSRC] = 0x3)

Table 63. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x3 (DDR mode)

ID	Parameter	Min.	Max.	Unit
	FlexSPIx[A/B]_SCLK cycle frequency	—	See values in Table 64	MHz

Table continues on the next page...

Table 63. FlexSPI timings with FlexSPIn_MCR0[RXCLKSRC] = 0x3 (DDR mode) (continued)

ID	Parameter	Min.	Max.	Unit
t_1	FlexSPIx[A/B]_SCLK high or low time	2.25	—	ns
t_2	FlexSPIx[A/B]_SSy_B pulse width	1	—	SCLK
t_3	FlexSPIx[A/B]_SSy_B lead time[1, 2]	(Tcss + 0.5) / 2	—	SCLK
t_4	FlexSPIx[A/B]_SSy_B lag time[1, 3]	Tsch / 2	—	SCLK
t_5	FlexSPIx[A/B]_DATAy output valid time	—	See DDR output setup for Mode 3 in Table 64	ns
t_6	FlexSPIx[A/B]_DATAy output hold time	See DDR output hold for Mode 3 in Table 64	—	ns
t_9	FlexSPIx[A/B]_DATAy input setup skew	—	See DDR input setup for Mode 3 in Table 64	ns
t_{10}	FlexSPIx[A/B]_DATAy input hold skew	—	See DDR input hold for Mode 3 in Table 64	ns

1. Timing is controlled from FLSHxCR1 register (x=A1, A2, B1, or B2).
2. Tcss: Chip select output setup time
3. Tcsh: Chip select output hold time

Table 64. FlexSPI AC DDR specifications for Mode 3

Parameter	Max interface frequency					Unit
Frequency DDR	180	166	100	83	50 - 42	MHz
DDR input setup	0.6	0.6	0.8	1.2	2.75	ns
DDR input hold	-0.6	-0.6	-0.8	-1.2	-2.75	ns
DDR output setup	0.6	0.6	1	1.25	3	ns
DDR output hold	-0.6	-0.6	-1	-1.25	-3	ns

7.3.1.8 DDR timing diagrams for Mode 3

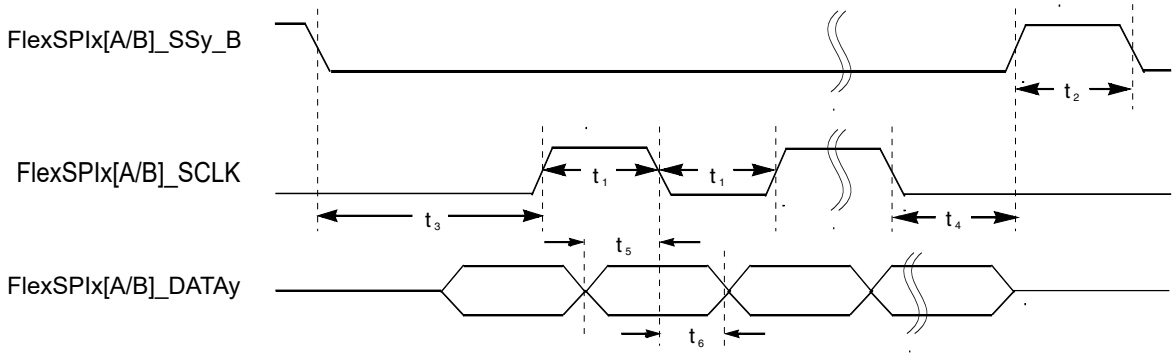


Figure 35. DDR output timing diagram for Mode 3

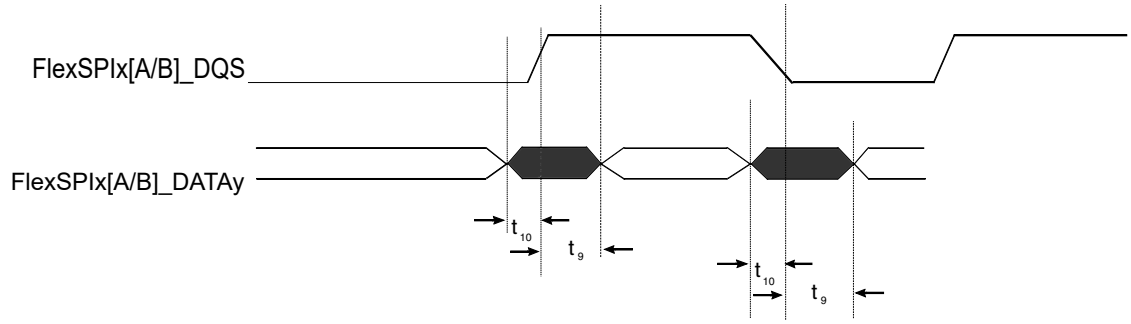


Figure 36. DDR input timing diagram with external DQS input sample for Mode 3

7.3.2 Analog modules

7.3.2.1 12-bit ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

Table 65. ADC Electrical Specifications (VREFH=VDD_ANA_18 and $VADIN_{max} \leq VREFH$)

Symbol	Description	Min	Typ	Max	Unit	Notes
VADIN	Input voltage	VREFL	—	VREFH	V	—
CADIN	Input capacitance	—	4.5	—	pF	—
RADIN	Input resistance	—	500	—	Ω	—
RAS	Analog source resistance	—	—	5	KΩ	1
fADCK	ADC Conversion clock frequency	8	—	66	MHz	
Csample	Sample cycles	3.5	—	131.5		2
Ccompare	Fixed compare cycles	—	17.5	—	cycles	
Cconversion	Conversion cycles	Cconversion= Csample + Ccompare			cycles	
TUE	Total unadjusted Error	—	-14 to -2	—	LSB	3
DNL	Differential nonlinearity	—	±1.2	—	LSB	3,4
INL	Integral nonlinearity	—	±1.2	—	LSB	3,4
ENOB	Effective number of bits					5
	Single-ended mode					
	Avg = 1	—	10.5	—		
	Avg = 2	—	10.8	—		
	Avg = 16	—	11.4	—		
	Differential mode					
	Avg = 1	—	11.4	—		

Table continues on the next page...

Table 65. ADC Electrical Specifications (VREFH=VDD_ANA_18 and $VADIN_{max}$≤VREFH) (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
	Avg = 2	—	—	—		
	Avg = 16	—	—	—		
SINAD	Signal to noise plus distortion	SINAD=6.02 x ENOB + 1.76			dB	
EFS	Full-scale error	—	-4	—	LSB	3
EZS	Zero-scale error	—	0.05	—	LSB	3
Iin_ext_leak	External channel leakage current	—	30	500	nA	
EIL	Input leakage error	RAS * Iin			mV	

1. This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS time constant should be kept to < 1 ns.
2. See Figure 37.
3. 1 LSB = (VREFH - VREFL)/2N, N=12
4. ADC conversion clock at max frequency and using linear histogram.
5. Input data used for test was 1 kHz sine wave.

Table 66. ADC electrical specifications (VREFH=1.68 V and $VADIN_{max}$≤VDD_PTA_{max})[1]

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
VADIN	Input voltage—Port A	VREFL	—	VDD_PTA_{max}	V	
	Input voltage—Port B			VDD_PTB_{max}		
CADIN	Input capacitance		4.5	—	pF	
RADIN	Input resistance		1	—	KΩ	
RAS	Analog source resistance		—	5	KΩ	3
fADCK	ADC conversion clock frequency	8	—	66	MHz	
Csample	Sample cycles	3.5	—	131.5	—	4
Ccompare	Fixed compare cycles	—	17.5	—	Cycles	
Cconversion	Conversion cycles	Cconversion= Csample + Ccompare			Cycles	
TUE	Total unadjusted error	—	-14 to -2	—	LSB	5
DNL	Differential nonlinearity	—	±1.2	—	LSB	5,6

Table continues on the next page...

Table 66. ADC electrical specifications (VREFH=1.68 V and $VADIN_{max} \leq VDD\_PTA_{max}$)[1] (continued)

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
INL	Integral nonlinearity	—	±1.2	—	LSB	[5],[6]
ENOB	Effective Number of Bits					[7]
	Single-ended mode					
	Avg = 1	—	10.3	—		
	Avg = 2	—	10.6	—		
	Avg = 16	—	11.3	—		
	Differential mode					
	Avg = 1	—	11.2	—		
	Avg = 2	—	—	—		
	Avg = 16	—	—	—		
SINAD	Signal to noise plus distortion	SINAD=6.02 x ENOB + 1.76			dB	
EFS	Full-scale error	—	-4	—	LSB	[5]
EZS	Zero-scale error	—	0.05	—	LSB	[5]
Iin_ext_leak	External channel leakage current	—	30	500	nA	
EIL	Input leakage error	RAS * Iin			mV	

1. Values in this table are based on design simulations.
2. Typical values assume VDD_ANA_18 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only, and are not tested in production.
3. This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS time constant should be kept to < 1 ns.
4. See Figure 37.
5. 1 LSB = (VREFH - VREFL)/2N, N=12
6. ADC conversion clock at max frequency and using linear histogram.
7. Input data used for test was 1 kHz sine wave.

Table 67. ADC electrical specifications ($1V \leq VREFH < VDD\_ANA18_{MIN}$ and $VADIN_{MAX} \leq VREFH$) [1]

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
VADIN	Input voltage	VREFL	—	VREFH	V	—
CADIN	Input capacitance	—	4.5	—	pF	—
RADIN	Input resistance	—	500	—	Ω	

Table continues on the next page...

Table 67. ADC electrical specifications (1V≤VREFH<VDD_ANA18_{MIN} and $VADIN_{MAX}$≤VREFH) [1] (continued)

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
RAS	Analog source resistance	—	—	5	KΩ	[3]
fADCK	ADC conversion clock frequency	8	—	44	MHz	
Csample	Sample cycles	3.5	—	131.5	—	[4]
Ccompare	Fixed compare cycles	—	17.5	—	Cycles	
Cconversion	Conversion cycles	Cconversion= Csample + Ccompare			Cycles	
TUE	Total unadjusted error	—	-14 to -2	—	LSB	[5]
DNL	Differential nonlinearity	—	±1.2	—	LSB	[5,6]
INL	Integral nonlinearity	—	±1.2	—	LSB	[5,6]
ENOB	Effective number of bits					[7]
	Single-ended mode					
	Avg = 1	—	9.8	—	—	
	Avg = 2	—	10.2	—	—	
	Avg = 16	—	11.1	—	—	
	Differential mode					
	Avg = 1	—	10.7	—	—	
	Avg = 2	—	—	—	—	
	Avg = 16	—	—	—	—	
SINAD	Signal to noise plus distortion	SINAD=6.02 x ENOB + 1.76			dB	
EFS	Full-scale error	—	-4	—	LSB	[5]
EZS	Zero-scale error	—	0.05	—	LSB	[5]
Iin_ext_leak	External channel	—	30	500	nA	—

Table continues on the next page...

Table 67. ADC electrical specifications (1V≤VREFH<VDD_ANA18_{MIN} and $VADIN_{MAX}$≤VREFH) [1] (continued)

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
	leakage current					
EIL	Input leakage error	RAS * Iin			mV	—

1. Values in this table are based on design simulations.
2. Typical values assume VDD_ANA_18 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only, and are not tested in production.
3. This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS time constant should be kept to < 1 ns.
4. See Figure 37.
5. 1 LSB = (VREFH - VREFL)/2N, N=12
6. ADC conversion clock at max frequency and using linear histogram.
7. Input data used for test was 1 kHz sine wave.

The following figure shows a plot of the ADC sample time versus RAS.

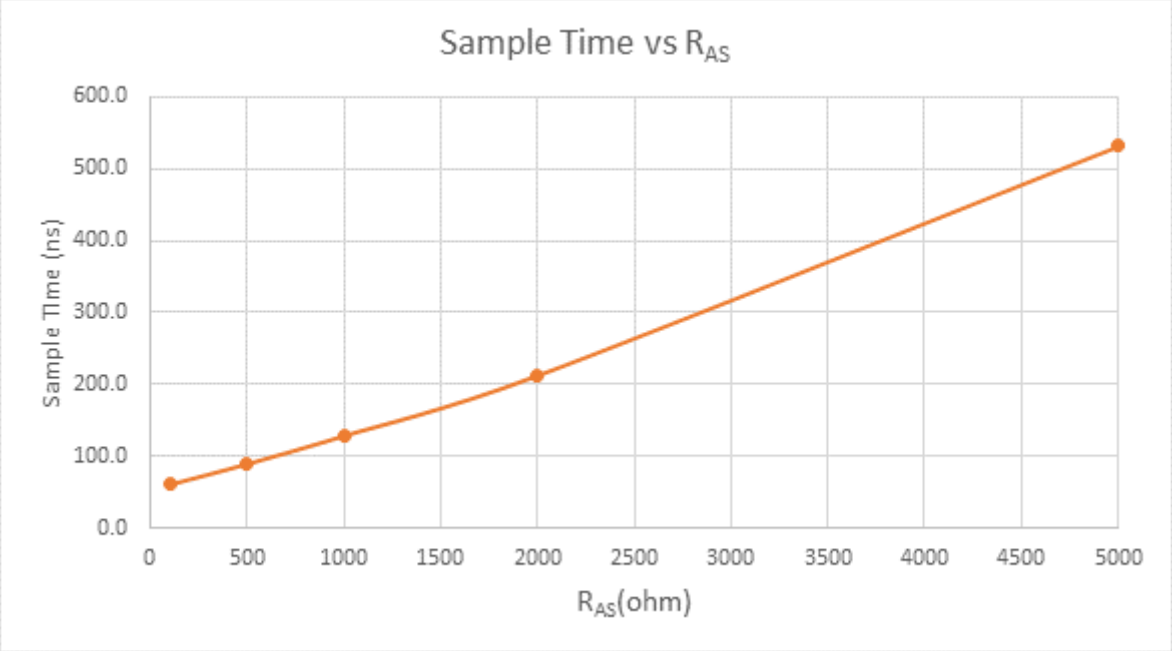


Figure 37. Sample time vs R_{AS}

7.3.2.1.1 ADC operating conditions

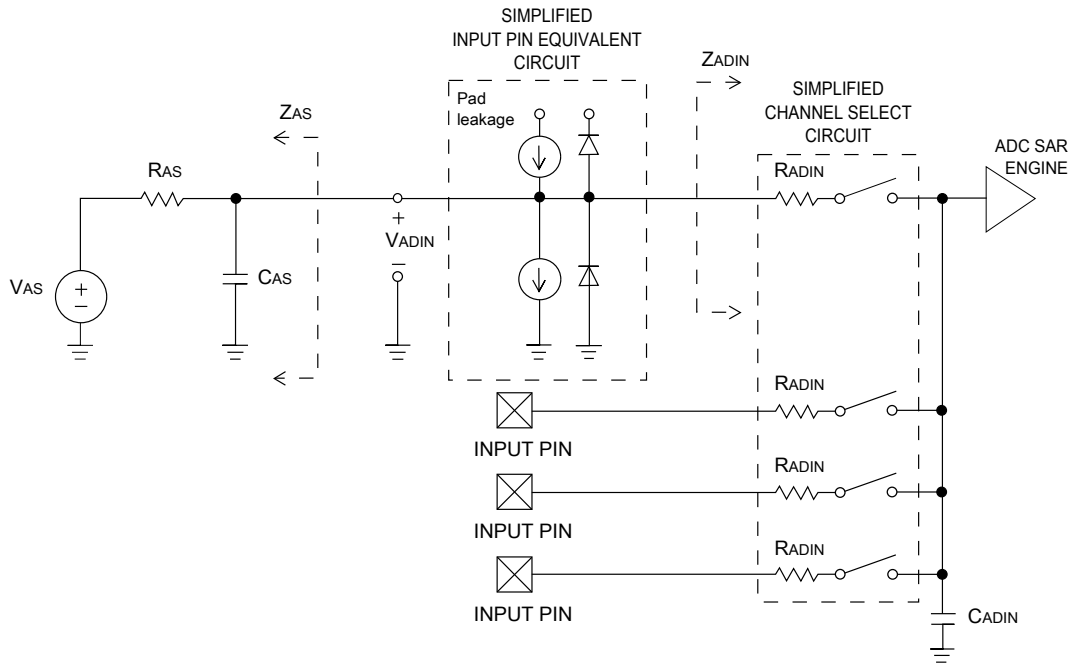


Figure 38. ADC input impedance equivalency diagram

7.3.2.2 12-bit DAC electrical characteristics

7.3.2.2.1 12-bit DAC operating requirements

Table 68. 12-bit DAC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Notes
C_L	Output load capacitance	—	50	100	pF	1
I_L	Output load current	—	—	±1	mA	2

1. The DAC output can drive R and C loading. The user should consider both DC and dynamic application requirements. 50pF CL provides the best dynamic performance, while 100pF provides the best DC performance.
2. Sink or source current ability.

Table 69. DAC characteristics

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units	Notes
IDDA_LS	Supply Current in Low Speed mode	Code 800h, VDD_ANA18 selected, no Rload	—	80	120	µA	1
			—	80	—		2
IDDA_MS	Supply Current in Middle Speed mode		—	250	450		1
			—	250	—		2
IDDA_HS	Supply Current in High Speed mode		—	500	850		1
			—	500	—		2

Table continues on the next page...

Table 69. DAC characteristics (continued)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units	Notes
VDACOUTL	DAC low level output voltage	VDD_ANA18 selected, Rload=18k, Cload=50pF	VSS	—	0.15	V	3
VDACOUTH	DAC high level output voltage		VDD_ANA18 -0.15	—	VDD_ANA18		
DNL	Differential non-linearity error	Code 100h -> F00h best fit curve	—	±0.5	±1	LSB	—
INL	Integral non-linearity error	Code 100h -> F00h best fit curve	—	±2	—		4
			—	±1	—		5
EO	Offset error	Code 100h	—	±0.6	—	%FSR	—
TEO	Offset error temperature coefficient	Code 100h	—	±30	—	uV/°C	—
EG	Gain error	Code F00h	—	±0.3	—	%FSR	—
TEG	Gain error temperature coefficient	Code F00h	—	10	—	ppm of FSR/°C	—
TFS_LS	Full scale setting time in Low Speed mode	Code 100h -> F00h or F00h -> 100h @ ZTC current	—	5	—	µs	6
		Code 100h -> F00h or F00h -> 100h @ PTAT current	—	5	—		
TFS_MS	Full scale setting time in Middle Speed mode	Code 100h -> F00h or F00h -> 100h @ ZTC current	—	1	—		
		Code 100h -> F00h or F00h -> 100h @ PTAT current	—	1	—		
TFS_HS	Full scale setting time in High Speed mode	Code 100h -> F00h or F00h -> 100h @ ZTC current	—	0.5	—		
		Code 100h -> F00h or F00h -> 100h @ PTAT current	—	0.5	—		
TCC_LS	Code to code setting time in Low Speed mode	Code 7F7h -> 807h or 807h -> 7F7h @ ZTC current	—	1	—		
		Code 7F7h -> 807h or 807h -> 7F7h @ PTAT current	—	1	—		
TCC_MS	Code to code setting time in Middle Speed mode	Code 7F7h -> 807h or 807h -> 7F7h @ ZTC current	—	0.5	—		
		Code 7F7h -> 807h or 807h -> 7F7h @ PTAT current	—	0.5	—		
TCC_HS	Code to code setting time in High Speed mode	Code 7F7h -> 807h or 807h -> 7F7h @ ZTC current	—	0.3	—		
		Code 7F7h -> 807h or 807h -> 7F7h @ PTAT current	—	0.3	—		

Table continues on the next page...

Table 69. DAC characteristics (continued)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units	Notes
SR_LS	Slew rate in Low Speed mode	Code 100h -> F00h or F00h -> 100h @ ZTC current	—	0.24	—	V/µs	7
		Code 100h -> F00h or F00h -> 100h @ PTAT current	—	0.24	—		
SR_MS	Slew rate in Middle Speed mode	Code 100h -> F00h or F00h -> 100h @ ZTC current	—	1.2	—		
		Code 100h -> F00h or F00h -> 100h @ PTAT current	—	1.2	—		
SR_HS	Slew rate in High Speed mode	Code 100h -> F00h or F00h -> 100h @ ZTC current	—	2.4	—		
		Code 100h -> F00h or F00h -> 100h @ PTAT current	—	2.4	—		
PSRR	Power supply rejection ratio	Code 800h, ΔVDD_ANA18=100mV, VREFH_ANA12 selected	—	70	—	dB	8
Glitch	Glitch energy	Code 100h -> F00h -> 100h	—	30	—	nV-s	—
		Code 7FFh -> 800h -> 7FFh	—	30	—		
CT	Channel to channel crosstalk	—	—	—	-80	dB	9
ROP	Output resistance	Code 100h -> 2A8h and D58h -> F00h	—	200	—	Ω	10
		Code 2A8h and D58h	—	30	—	Ω	

1. DAC output reference current is configured as either the PTAT current reference or the internal current reference in the DAC Status and Control Register (DAC_CR2).
2. DAC output reference current is configured as the ZTC current reference in the DAC Status and Control Register (DAC_CR2).
3. It is recommended to operate the DAC in the output voltage range between 0.15 V and

   (VDD_ANA18

   -0.15

   V) for best accuracy. Linearity of the output voltage outside this range will be affected as current load increases.
4. When VDD_ANA18 is selected as the reference (DAC_CR[DACRFS]=1b).
5. When the VREFH_ANA18 is selected as the reference (DAC_CR[DACRFS]=0b).
6. The DAC output remains within ±0.5 LSB of the final measured value for digital input code change. Noise on the power supply can cause this performance to degrade to ±1 LSB. This parameter represents both rising edge and falling edge settling time.
7. Time for the DAC output to transition from 10% to 90% signal amplitude (rising edge or falling edge).
8. PSRR=20*log{ΔVDD_ANA18 /ΔVDAC_OUT}
9. If two DACs are used and sharing the same VREFH.
10. Based on design simulation.

7.3.2.3 CMP electrical specifications

Table 70. CMP Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VREFH_EXT	External reference voltage	1	—	1.98	V
VREFH_INT[1]	Internal reference voltage	—	1.3	—	V

1. This is an internally generated voltage reference generated by PMC0.

Table 71. CMP Characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
VAIN	Analog input voltage		0		VDD_PT*x*[1]	V
VAIO	Analog input offset voltage				20	mV
VH	Analog comparator hysteresis	Hysctrl[1:0]=00		5		mV
		Hysctrl[1:0]=01		10		mV
		Hysctrl[1:0]=10		20		mV
		Hysctrl[1:0]=11		30		mV
TDHS	Propagation delay, high-speed mode	Nominal supply			50	ns
TDHS	Propagation delay, low-speed mode				5	µs
	Analog comparator initialization delay				20	µs
INL	8B DAC integral non-linearity		-1		1	LSB
DNL	8B DAC differential non-linearity		-1		1	LSB

1. The maximum input voltage for CMP analog inputs associated with Port A (PTA) is VDD_PTA. The maximum input voltage for CMP analog inputs associated with Port B (PTB) is VDD_PTB.

7.3.3 Timer specifications—real-time domain

See General switching timing specifications.

7.3.4 Connectivity and communications specifications—real-time domain

7.3.4.1 LPUART

See General switching timing specifications.

7.3.4.2 Inter-Integrated Circuit Interface (I^2C) timing—real-time domain

See Inter-Integrated Circuit Interface (I^2C) timing.

7.3.4.3 LPSPI switching specifications—real-time domain

See Low-power serial peripheral interface (LPSPI) switching specifications—application domain.

7.3.4.4 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

All timing shown is also with respect to input signal transitions of 3 ns and a 50 pF maximum load.

Table 72. I2S/SAI master mode timing

Num.	Parameter	Min	Max	Unit
S1	I2S_MCLK cycle time	20	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	40	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	17.5	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	17.5	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	19.8	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

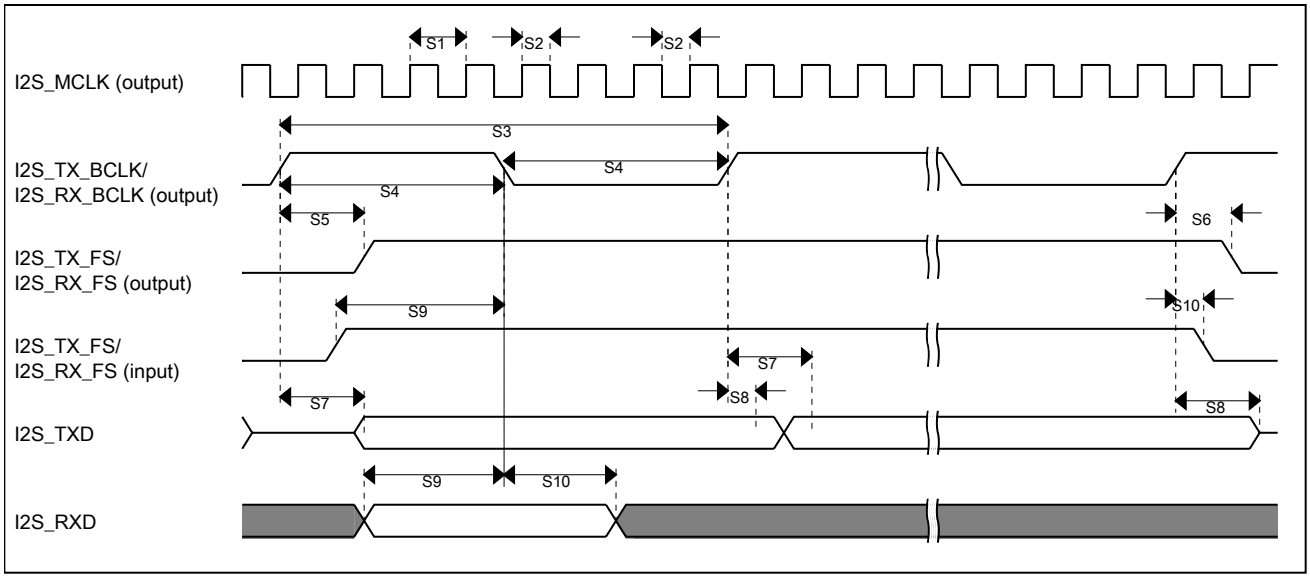


Figure 39. I2S/SAI timing — master modes

Table 73. I2S/SAI slave mode timing

Num.	Parameter	Min	Max	Unit
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	40	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/ I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/ I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	18	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	2	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	17.0	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

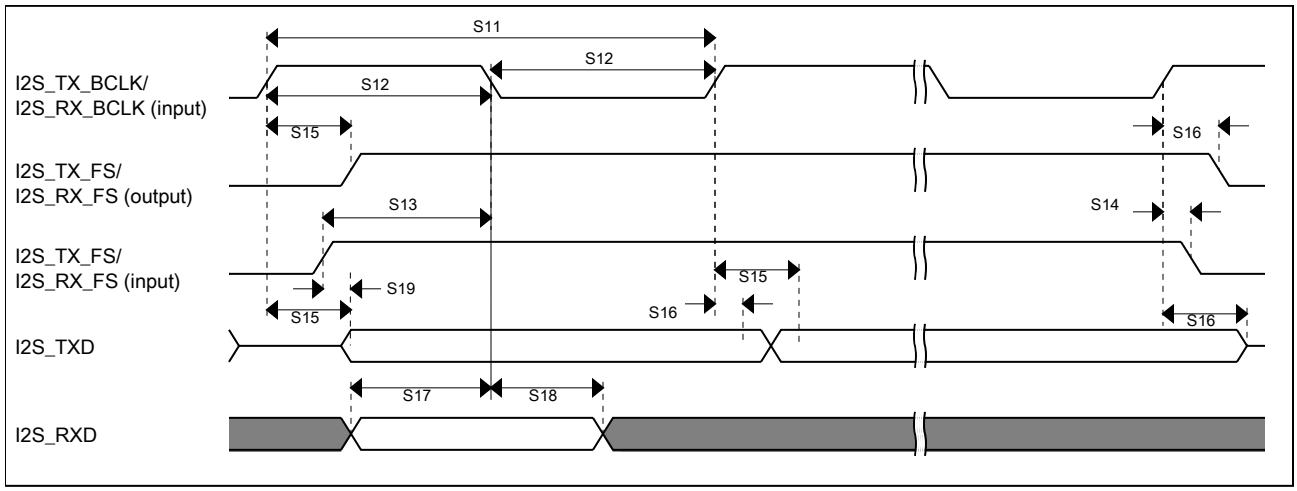


Figure 40. I2S/SAI timing — slave modes

7.3.4.5 FlexIO specifications—real-time domain

See General switching timing specifications

7.3.4.6 CAN switching specifications

See General switching timing specifications.

8 Package information

This section contains package information for the following packages:

- MAPBGA 15 x 15 mm, 0.5 mm pitch (485 MAPBGA)
- FCBGA 9.4 x 9.4 mm, 0.4 mm pitch (512 FCBGA)

8.1 MAPBGA, 15 x 15 mm, 0.5 mm pitch (485 MAPBGA)

This section includes the following information for the 15 x 15 mm, 0.5 mm pitch package:

- Case outline
- Ball map

8.1.1 15 x 15 mm package case outline

The following figure shows the top, bottom, and side views of the 15 × 15 mm MAPBGA package.

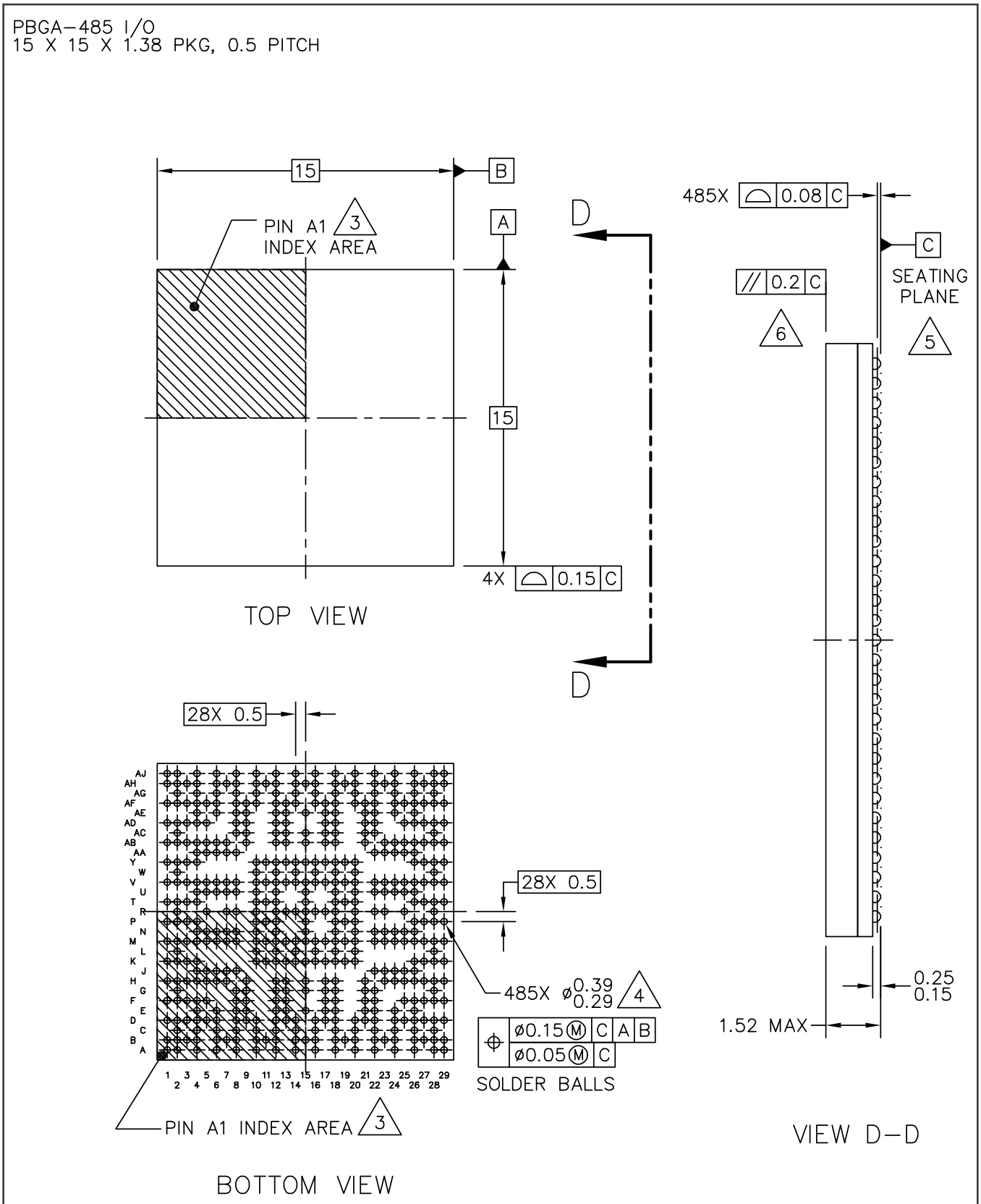


Figure 41. 15 x 15 mm case outline

PBGA–485 I/O
15 X 15 X 1.38 PKG, 0.5 PITCH

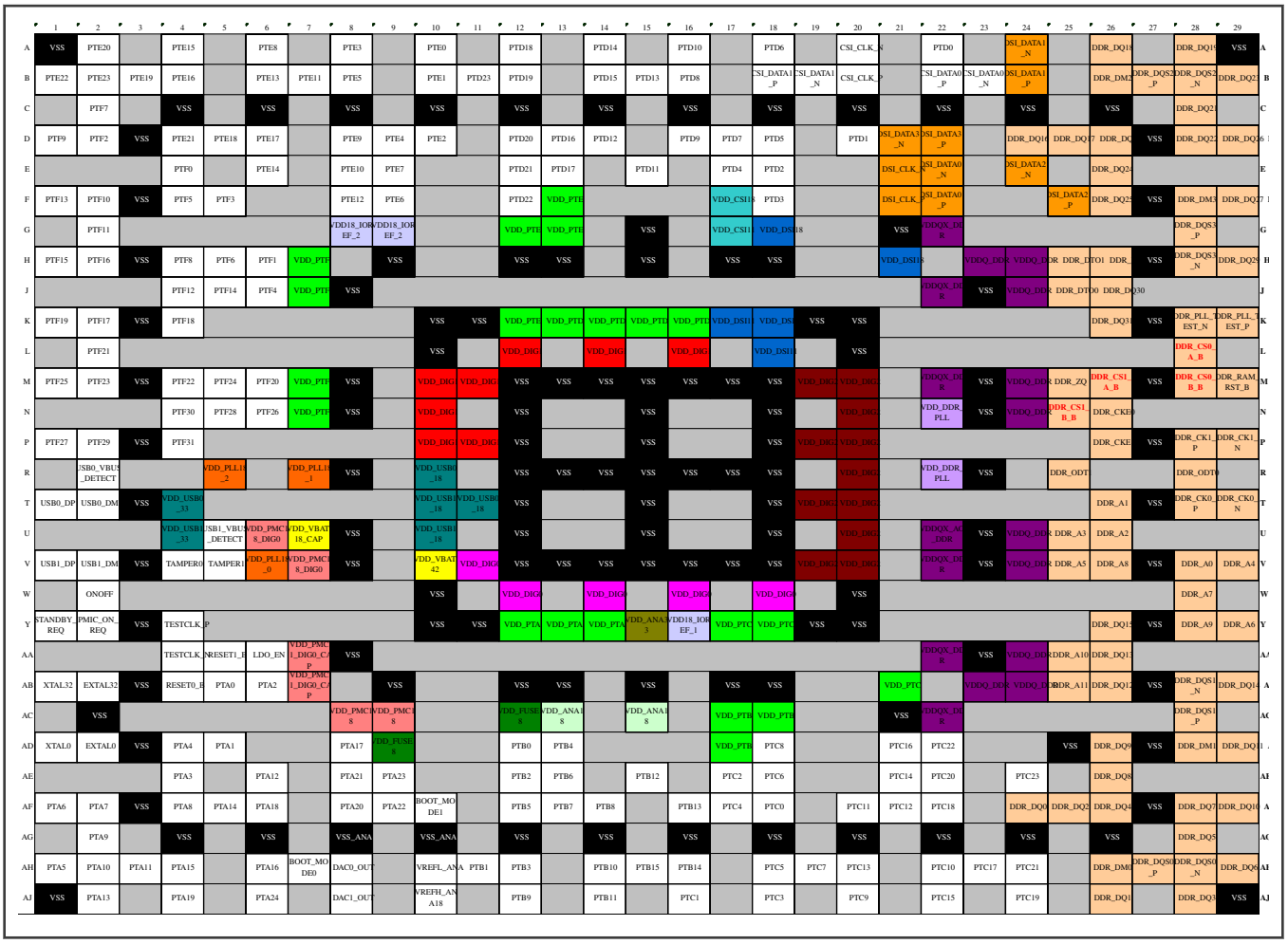
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 42. Notes on 15 x 15 mm case outline

8.1.2 15 x 15 mm, 0.5 mm pitch, ball map

The following figure shows the 15 × 15 mm, 0.5 mm pitch, ball map.



8.2 FCBGA, 9.4 x 9.4 mm, 0.4 mm pitch (512 FCBGA)

This section includes the following information for the 9.4 x 9.4 mm, 0.4 mm pitch package (512 FCBGA).

- Case outline
- Ball map

8.2.1 9.4 x 9.4 mm package case outline

The following figure shows the top, bottom, and side views of the 9.4 x 9.4 mm FCBGA package.

FC-PBGA-512 I/O
9.4 X 9.4 X 0.811 PKG, 0.4 PITCH

SOT2147-1

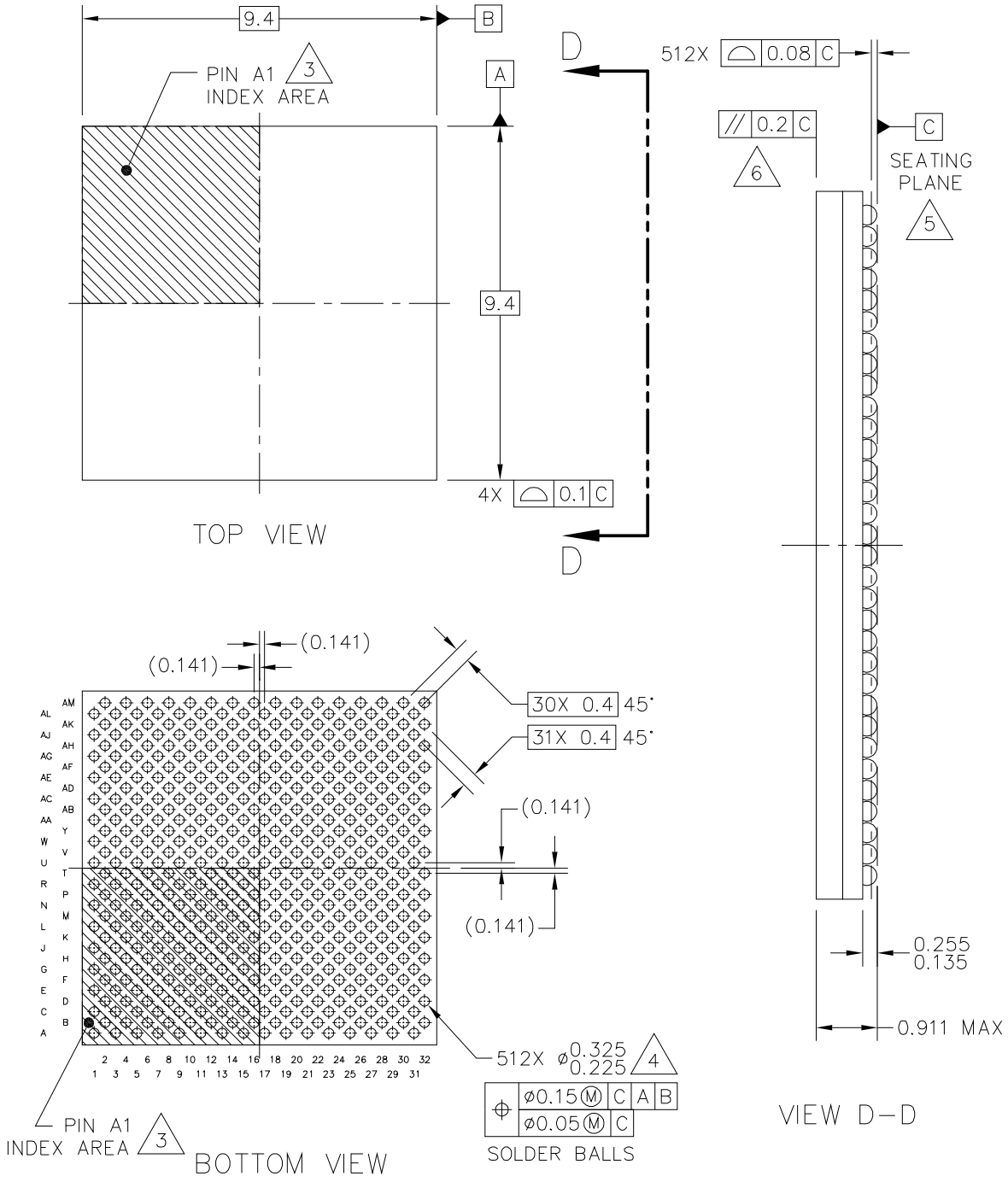


Figure 43. 9.4 x 9.4 mm case outline

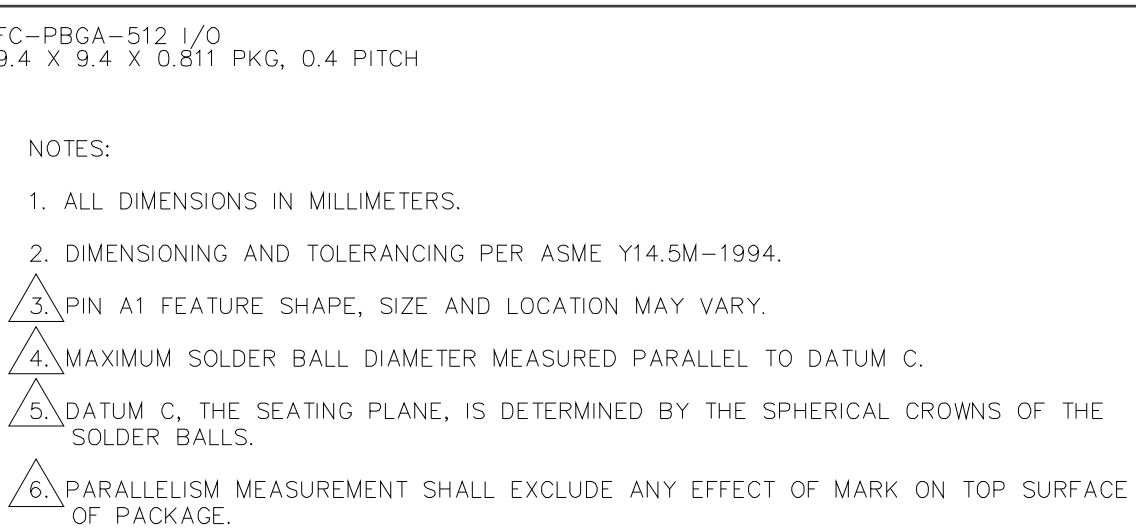


Figure 44. 9.4 x 9.4 mm case outline notes

8.2.2 9.4 x 9.4 mm, 0.4 mm pitch, ball map

The following page shows the 9.4 x 9.4 mm, 0.4 mm pitch, ball map.

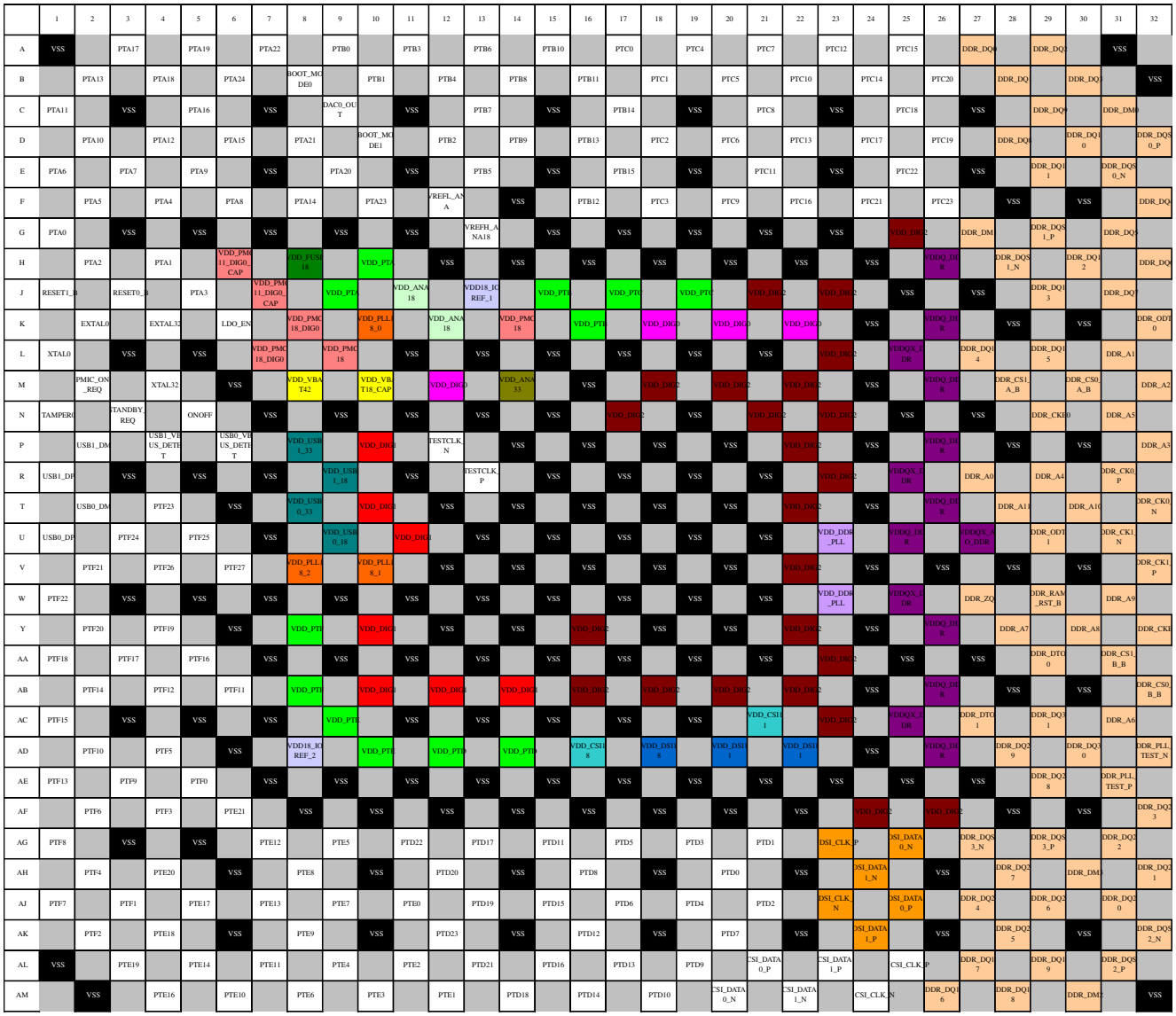


Figure 45. 9.4 x 9.4 mm ballmap

9 Pin Multiplexing

9.1 i.MX 8ULP pin multiplexing

See the attached IO Definition and Package Ballmap spreadsheet for the pinout table of 485 MAPBGA as well as 512 FCBGA package.

10 Revision History

10.1 Revision history

The following table shows the revision history of this document.

Table 74. Revision history

Revision number	Date	Substantial changes
Rev 1	09/2023	• Initial Release.

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Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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