Freescale Semiconductor
Application Note

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i.MX 6 Series HDMI Test Method for Eye Pattern and Electrical Characteristics

This document applies to the following i.MX6 series chips: i.MX 6Quad, i.MX 6Dual, i.MX 6DualLite, and i.MX 6Solo.

It describes the necessary procedures, tools, and criteria for testing the compliance of devices with the *HDMI Compliance Test Specification* (HDMI.org, 2009), version 1.4a.

Contents

1 Test equipment and method

Table 1 indicates what equipment and method were used for the test.

Table 1. Test equipment and method

Equipment/method	Name
Boards	• MCIMX6Q-SDP • MCIMX6DL-SDP
Oscilloscope	Tektronix MSO72004C
Probes	Tektronix P7313SMA (4)
HDMI fixture	Wilder-Tech TPA-P with EDID attached
Power supply	SunPower P40A-1P2J
Operating system	Linux
Test source	*HDMI Compliance Test Specification* (HDMI.org, 2009), version 1.4a

2 Software configuration and procedures

The following sequence details the software configuration and testing procedures.

1. Check the video modes that the monitor can support.
2. Command:
   cat /sys/class/graphics/fb0/mode
   The definition of the video modes in Linux kernel are as follows:

```
if (mode->flag & FB_MODE_IS_DETAILED)
            m = 'D';
 if (mode->flag & FB_MODE_IS_VESA)
        m = 'V';
 if (mode->flag & FB_MODE_IS_STANDARD)
        m = 'S';


#define FB_MODE_IS_UNKNOWN      0
 #define FB_MODE_IS_DETAILED     1
 #define FB_MODE_IS_STANDARD     2
 #define FB_MODE_IS_VESA         4
```

3. Set video resolution, for example 1920*1080p60.
4. Command:

```
echo S:1920x1080p-60 > /sys/class/graphics/fb0/mode
```

5. Run Tektronix test software.

Table 2. HDMI TX memory map

Name	Address Offset	Width	R/W	Description	Value after Reset
I²C Master PHY Registers					
PHY_I2CM_SLAVE_ADDR	0x3020	8 bits	R/W	I2C Master PHY slave address	0x00
PHY_I2CM_ADDRESS_ADDR	0x3021	8 bits	R/W	PHY Register Address	0x00
PHY_I2CM_DATAO_1_ADDR	0x3022	8 bits	R/W	Data to write in PHY register (MSB)	0x00
PHY_I2CM_DATAO_0_ADDR	0x3023	8 bits	R/W	Data to write in PHY register (LSB)	0x00
PHY_I2CM_DATAI_1_ADDR	0x3024	8 bits	R/W	Data read from PHY register (MSB)	0x00
PHY_I2CM_DATAI_0_ADDR	0x3025	8 bits	R/W	Data read from PHY register (LSB)	0x00
PHY_I2CM_OPERATION_ADDR	0x3026	8 bits	W	Read or Write operation request	0x00
PHY_I2CM_INT_ADDR	0x3027	8 bits	R/W	PHY “done” interrupt	0x08

The driver voltage level configuration depends on the source termination value, the driver pre-emphasis settings, and the target signal voltage level swing.

A correct configuration must be set to meet both eye diagram mask and the specified high and low signal voltage levels.

To correctly configure the driver voltage level, the following parameters and signals (represented by their symbol) must be taken into consideration:

VPHRXTERM = 3.3 V→ 3.3-V supply rail connected to HDMI PHY sink termination resistors

RXTERM = 50 Ω → HDMI PHY sink termination resistors

Table 3. Register definitions

Control Register	Register field	Access type	Address	Value at reset
TXTERM	d_tx_term[2:0]	R/W	0x19	0x0007
VLEVCTRL	sup_tx_lvl[4:0]	R/W	0x0E	0x0000
VLEVCTRL	sup_ck_lvl[4:0]	R/W/O	0x09	0x0009
CKSYMTXCTRL	tx_symon	R/W	0x0E	0x0000
CKSYMTXCTRL	tx_traon	R/W	0x0E	0x0000
CKSYMTXCTRL	tx_trbon	R/W	0x0E	0x0000

Table 4. TXTERM

Field	Description
d_tx_term[2:0]	Digital Transmission Termination This bus defines the transmission termination (resistance) value, which is set by the HDMI controller. The formula for the resistance value is: $R = \frac{50}{1 - 0.125 \times d\_tx\_term}$ This equation is only valid when d_tx_term equals 0-6. 000: 50 Ω 001: 57.14 Ω 010: 66.67 Ω 011: 80 Ω 100: 100 Ω 101: 133.33 Ω 110: 200 Ω 111: Open circuit

Table 5. VLEVCTRL

Field	Description
sup_ck_lvl[4:0]	Support Clock Level This bus controls the reference voltage level of the Clock Channel module. This voltage reference has a direct relationship with the output signal voltage level.
sup_tx_lvl[4:0]	Support Transmitter Level This bus controls the reference voltage level of the three transmitter channel modules. This voltage reference has a direct relationship with the output signal voltage level.

Table 6. CKSYMTXCRTL

Field	Description
ck_symon	Clock Symbol On This bit enables the clock symbol driver. To enable the clock driver, the ck_powon bit must be high. In addition, there is no pre-emphasis enable for the clock driver. 0: Disable the clock symbol driver, if the Override bit is 0. 1: Enable the clock symbol driver, if the Override bit is 0.
tx_trbon	Transmitter Trailer B On This bit enables the transmitter trailer B driver(s). To enable the transmitter trailer B driver(s) and to enable pre-emphasis, the tx_pwron bit for each channel must be high. 0: Disable the transmitter trailer B driver(s), if the Override bit is 0. 1: Enable the transmitter trailer B driver(s), if the Override bit is 0.

Table 6. CKSYMTXCRTL (continued)

Field	Description
tx_traon	Transmitter Trailer A On This bit enables the transmitter trailer A driver(s). To enable the transmitter trailer A driver(s) and to enable pre-emphasis, the tx_pwron bit for each channel must be high. 0: Disable the transmitter A driver(s), if the Override bit is 0. 1: Enable the transmitter A driver(s), if the Override bit is 0.
tx_symon	Transmitter Symbol On This bit enables the transmitter symbol driver(s). To enable the transmitter driver(s), the tx_pwron bit for each channel must be high. 0: Disable the transmitter symbol driver(s), if the Override bit is 0. 1: Enable the transmitter symbol driver(s), if the Override bit is 0.

Table 7 defines the pre-emphasis factor (PREEMPH).

Table 7. PREEMPH definition

SYMON	TRAON	TRBON	PREEMPH
0	0	0	—
1	0	0	0.00
1	0	1	0.08
1	1	0	0.17
1	1	1	0.25

The following equations can be used to calculate—for a certain signal voltage swing (VSWING) and PHY configuration (PREEMPH, RTERM)—the signal's high and low voltage levels (VHI, VLO).

$$VLO = VPH_{RXTERM} - \frac{VSWING}{1 - PREEMPH} - \frac{VSWING \times RXTERM(1 + PREEMPH)}{2 \times RTERM \times (1 - PREEMPH)} \quad \textit{Eqn. 1}$$

$$VHI = VLO + VSWING \quad \textit{Eqn. 2}$$

$$TXLVL = CKLVL = \frac{0.772 - VPH_{RXTERM} - VLO}{0.01405} \quad \textit{Eqn. 3}$$

For a certain termination value and pre-emphasis configuration (factor), users input only the VSWING value. With this data, users can obtain the respective VHI and VLO DC levels and the TXLVL and CKLVL configuration to apply to the PHY.

Lower TXLVL/CKLVL values result in higher signal amplitudes, while higher TXLVL/CKLVL values result in lower signal amplitudes.

Values for VSWING, VHI, and VLO must be within HDMI 1.4a specification limits. Table 8 provides driver voltage level settings for some example scenarios.

NOTE

VSWING should be set at 400–600 mV.

Table 8. Example driver voltage level settings

RTERM	SYMON	TRAON	TRBON	VHI (V)	VLO (V)	VSWING (V)	TXLVL	TXLVL (BIN)	CKLVL	CKLVL (BIN)
100	1'b1	1'b0	1'b0	3.200	2.800	0.400	19	10011	19	10011
100	1'b1	1'b0	1'b0	3.175	2.675	0.500	10	01010	10	01010
100	1'b1	1'b0	1'b1	3.107	2.607	0.500	6	00110	6	00110
133	1'b1	1'b0	1'b0	3.225	2.825	0.400	21	10101	21	10101
133	1'b1	1'b0	1'b0	3.206	2.706	0.500	13	01101	13	01101
133	1'b1	1'b0	1'b1	3.143	2.643	0.500	8	01000	8	01000

6. The following are PHY register settings that produce a passing result:
   a) HDMI write Reg 0xe=0x01ad; 0x09=0x800d; command
      /unit_tests/memtool -8 0x00123021=0x0e
      /unit_tests/memtool -8 0x00123022=0x01
      /unit_tests/memtool -8 0x00123023=0xad
      /unit_tests/memtool -8 0x00123026=0x10
      /unit_tests/memtool -8 0x00123021=0x09
      /unit_tests/memtool -8 0x00123022=0x80
      /unit_tests/memtool -8 0x00123023=0x0d
      /unit_tests/memtool -8 0x00123026=0x10
   b) HDMI read Reg 0x0e and 0x09 command
      /unit_tests/memtool -8 0x00123021=0x0e
      /unit_tests/memtool -8 0x00123026=0x1
      /unit_tests/memtool -8 0x00123024 2
      /unit_tests/memtool -8 0x00123021=0x09
      /unit_tests/memtool -8 0x00123026=0x1
      /unit_tests/memtool -8 0x00123024 2

3 Test results

3.1 Test data summary

i.MX 6 series silicon passes CTS 7-6, 7-7, 7-8, 7-9, 7-10 at 1080p 24bit, and CTS 7-2, 7-7 at 480p. Measurements shown in Table 9 through Table 11 have a PASS/NO PASS for final performance criteria.

Table 9. CTS7-2, 7-7 at 480p 60 Hz

Index	Test Name	Lanes	Spec Range	Measured Value	Result
1	7-2: Source Low Amplitude +(Supported Sink <= 165MHz)	CK+	2.700V < VL < 2.900V;	2.7475V	Pass
2	7-2: Source Low Amplitude +(Supported Sink <= 165MHz)	D0+	2.700V < VL < 2.900V;	2.7475V	Pass
3	7-2: Source Low Amplitude -(Supported Sink <= 165MHz)	CK-	2.700V < VL < 2.900V;	2.7600V	Pass
4	7-2: Source Low Amplitude -(Supported Sink <= 165MHz)	D0-	2.700V < VL < 2.900V;	2.7325V	Pass
5	7-2: Source Low Amplitude +(Supported Sink <= 165MHz)	D1+	2.700V < VL < 2.900V;	2.7375V	Pass
6	7-2: Source Low Amplitude -(Supported Sink <= 165MHz)	D1-	2.700V < VL < 2.900V;	2.7225V	Pass
7	7-2: Source Low Amplitude +(Supported Sink <= 165MHz)	D2+	2.700V < VL < 2.900V;	2.7450V	Pass
8	7-2: Source Low Amplitude -(Supported Sink <= 165MHz)	D2-	2.700V < VL < 2.900V;	2.7325V	Pass
9	7-7: Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.011*Tbit	Pass
10	7-7: Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.005*Tbit	Pass
11	7-7: Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.011*Tbit	Pass
12	7-7: Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.008*Tbit	Pass

Table 10. CTS7-4, 7-6, 7-8 at 1080p 60 Hz

Index	Test Name	Lanes	Spec Range	Measured Value	Result
1	7-6: Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.01*TPixel	Pass
2	7-6: Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0.012*TPixel	Pass
3	7-6: Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0.002*TPixel	Pass
4	7-4: Source Rise Time	CK	75.00ps < TRISE;	321.78ps	Pass
5	7-4: Source Rise Time	D0	75.00ps < TRISE;	215.70ps	Pass
6	7-4: Source Rise Time	D1	75.00ps < TRISE;	237.55ps	Pass
7	7-4: Source Rise Time	D2	75.00ps < TRISE;	224.37ps	Pass
8	7-4: Source Fall Time	CK	75.00ps < TFALL;	321.58ps	Pass
9	7-4: Source Fall Time	D0	75.00ps < TFALL;	237.85ps	Pass
10	7-4: Source Fall Time	D1	75.00ps < TFALL;	236.09ps	Pass
11	7-4: Source Fall Time	D2	75.00ps < TFALL;	180.79ps	Pass
12	7-8: Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.49%	Pass
13	7-8: Min Duty Cycle	CK	40.0% < Min Duty Cycle;	48.7%	Pass

Table 11. CTS7-9, 7-10 at 1080p 60 Hz

Index	Test Name	Lanes	Spec Range	Measured Value	Result
1	7-9: Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.087*Tbit	Pass
2	7-10: Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.09*Tbit	Pass
3	7-10: Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.08*Tbit	Pass
4	7-10: Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.1*Tbit	Pass

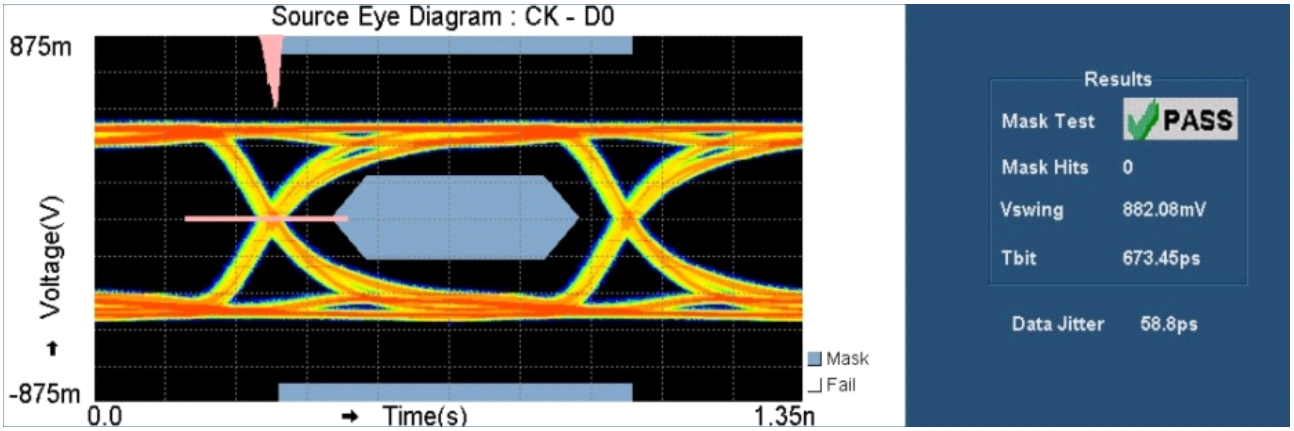

Figure 1. Source eye diagram: CK - D0 1080p 24-bit 60 Hz

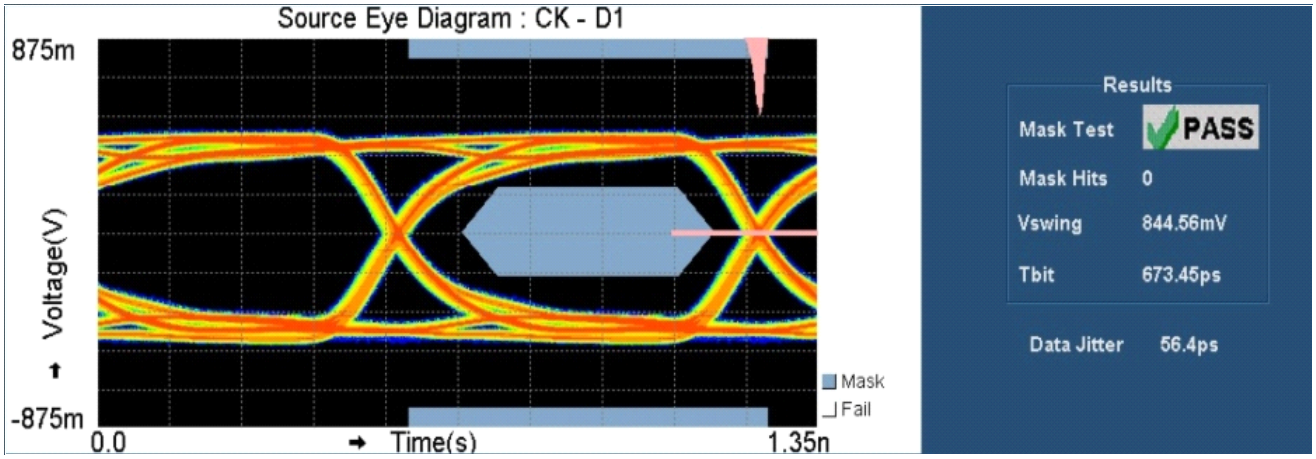

Figure 2. Source eye diagram: CK – D1 1080p 24-bit 60 Hz

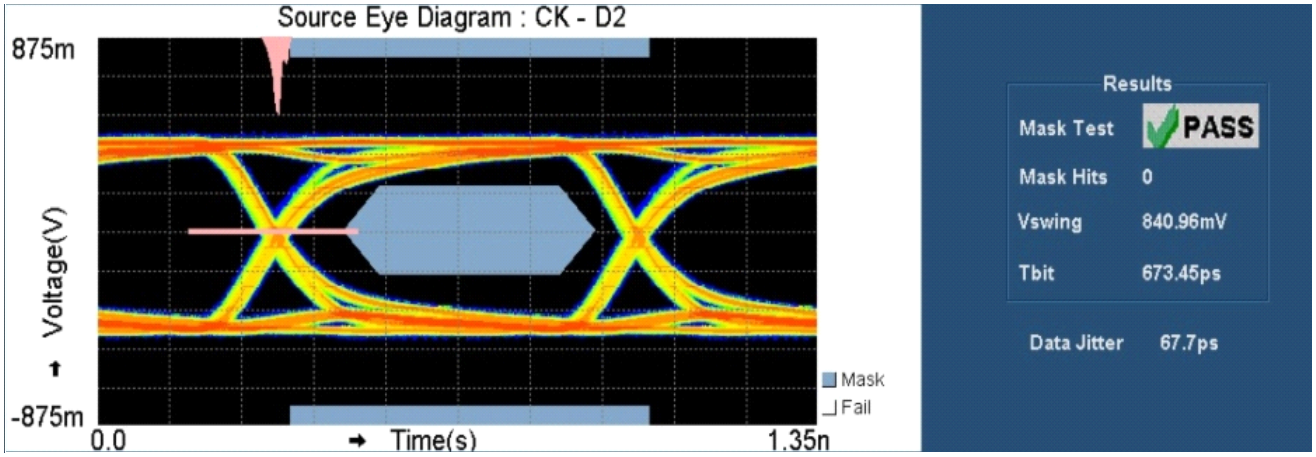

Figure 3. Source eye diagram: CK – D2 1080p 24-bit 60 Hz

4 Revision history

The following table provides a revision history for this application note.

Table 12. Revision history

Rev. Number	Date	Substantive Change
0	04/02/2013	Initial release.

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